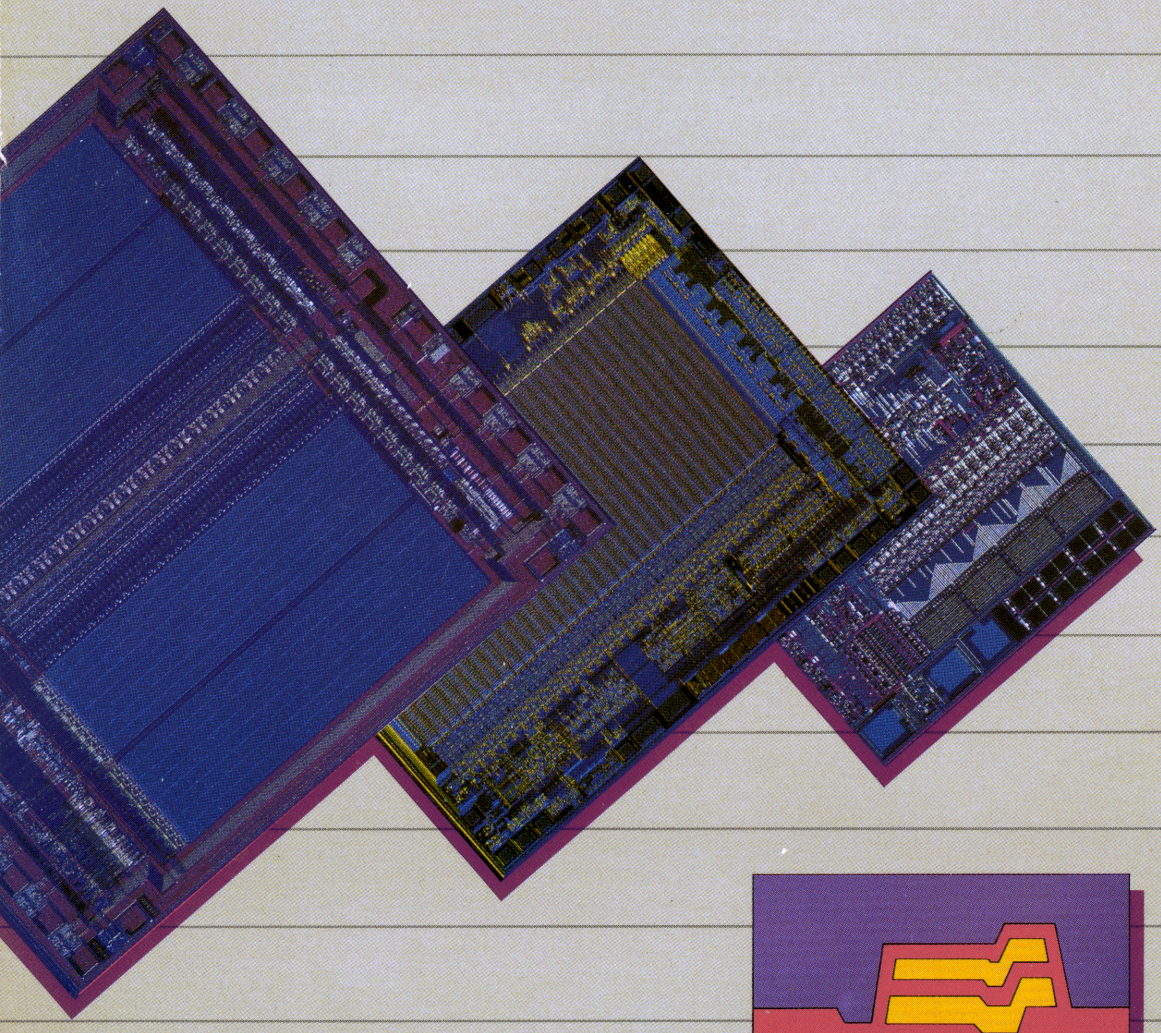
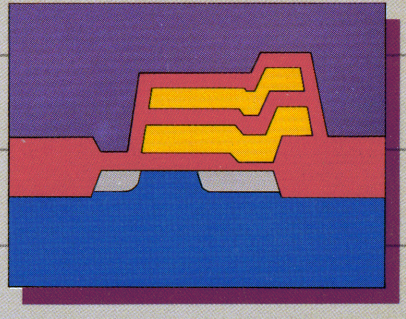
E^2 PROMs





EXEL MICROELECTRONICS

Excellence in E^2

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EXEL E²PROMs DATABOOK

EXEL Microelectronics
A Division of ROHM Corporation
2150 Commerce Drive • P.O. Box 49038
San Jose, CA 95161-9038
Phone 408 432-0500 • FAX 408 432-8710

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Excellence in E²

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President's Message

To Our Valued Customer:

EXEL Microelectronics has pursued its original charter to design, manufacture and market high performance E^2 products. Since 1983, EXEL has continued to follow that charter, serving both the commercial and industrial semiconductor markets.

EXEL Microelectronics with the aid of its parent company, ROHM Corporation of Japan, has invested millions of dollars in state-of-the-art manufacturing at our San Jose, California facility. This facility houses all of our design, manufacturing and marketing for E^2PROMs, ASEC Microcontrollers and E^2PLDs . ROHM has provided EXEL access to its expertise in the area of high-volume, low-cost manufacturing and quality. Additionally, EXEL Microelectronics products are marketed and distributed through an enhanced worldwide network of sales representatives.

EXEL's product line is unique in that it provides world-class reliability and quality with the convenience of U.S. design and manufacturing.

EXEL will continue to extend its leadership in the field of high-performance E^2 semiconductors. Your investment in EXEL memory products is also an investment in a long-term partnership with a growing, innovative company. This is our commitment to you, our valued customer.

Takashi Kobayashi
President

Section 3. Parallel E^2 Memory Products

Section 4. E^2 Application Notes

Section 5. Programmable Logic Devices

Section 6. Application Specific Embedded Controller

APPENDIX A. Packaging Information

GEN'L 1 INFO

SECTION 1 Table of Contents

Serial E², Parallel E², PLD E² and ASECs

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Max. Clock	Package Type	Number of Pins	Features	Section
Serial E²PROMs — I²C™ Bus Devices								
Serial 1K CMOS E²PROMs								
5V							5V Operation	
XL 24C01A	1K (128x8)	S,E	1mA/15µA	100 KHz	PDIP	8	Auto Increment, Vcc Lockout	2
XL 24C01A	1K (128x8)	S,E	1mA/15µA	100 KHz	SOIC JR	8	Xicor Compatible	
							Advance Information	
3V-5V							3V-5V Operation	
XL 24C01A-3	1K (128x8)	S,E	1mA/15µA	100 KHz	PDIP	8	Auto Increment	2
XL 24C01A-3	1K (128x8)	S,E	1mA/15µA	100 KHz	SOIC JR	8	Xicor Compatible	
							Advance Information	
Serial 2K CMOS E²PROMs								
5V							5V Operation	
XL 24C02	2K (256x8)	S,E	1mA/15µA	100KHz	PDIP	8	Auto Increment	2
XL 24C02	2K (256x8)	S,E	1mA/15µA	100KHz	SOIC JR	8	Vcc Lockout	
							Xicor Compatible	
							Advance Information	
3V-5V							3V-5V Operation	
XL 24C02-3	2K (256x8)	S,E	1mA/15µA	100 KHz	PDIP	8	Auto Increment	2
XL 24C02-3	2K (256x8)	S,E	1mA/15µA	100 KHz	SOIC JR	8	Xicor Compatible	
							Advance Information	
Serial 4K CMOS E²PROMs								
5V							5V Operation	
XL 24C04	4K (512x8)	S,E	1mA/15µA	100KHz	PDIP	8	Auto Increment	2
XL 24C04	4K (512x8)	S,E	1mA/15µA	100KHz	SOIC JR	8	Vcc Lockout	
XL 24C04	4K (512x8)	S,E	1mA/15µA	100KHz	DIE	8	Xicor Compatible	
							Preliminary Information	
3V-5V							3V-5V Operation	
XL 24C04-3	4K (512x8)	S,E	1mA/15µA	100 KHz	PDIP	8	Auto Increment	2
XL 24C04-3	4K (512x8)	S,E	1mA/15µA	100 KHz	SOIC JR	8	Xicor Compatible	
							Preliminary Information	
Serial 16K CMOS E²PROMs								
5V							5V Operation	
XL 24C16	16K (2Kx8)	S,E	3mA/15µA	100KHz	PDIP	8	Auto Increment	2
XL 24C16	16K (2Kx8)	S,E	3mA/15µA	100KHz	SOIC JR	8	Vcc Lockout	
							Xicor Compatible	
							Advance Information	
Serial E²PROMs — Microwire™ Bus Devices								
Serial 256 bit CMOS E²PROMs								
5V — with Advanced Features							5V Operation	
XL 93LC06	256 bit (16x16)	S,E	2mA/2µA	1 MHz	PDIP	8	Auto Increment	2
XL 93LC06	256 bit (16x16)	S,E	2mA/2µA	1 MHz	SOIC J	8	Vcc Lockout	
XL 93LC06	256 bit (16x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8	Microwire Serial Interface	
							Low Power Consumption	
Serial 1K CMOS E²PROMs								
5V — with Advanced Features							5V Operation	
XL 93LC46	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	Auto Increment	2
XL 93LC46	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8	Vcc Lockout	
XL 93LC46	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8	Microwire Serial Interface	
XL 93LC46	1K (64x16)	S,E	2mA/2µA	1 MHz	DIE	8	Low Power Consumption	

Serial E²PROMs — Microwire™ Bus Devices, continued

Serial 1K CMOS E²PROMs, continued

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Max. Clock	Package Type	Number of Pins	Features	Section
3V-5V - With Advanced Features								
XL 93LC46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	3V-5V Operation Auto Increment Microwire Serial Interface Low Power Consumption	2
XL 93LC46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
XL 93LC46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8		
XL 93LC46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	DIE	8		

Serial 1K CMOS E²PROMs

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Max. Clock	Package Type	Number of Pins	Features	Section
5V								
XL 93C46	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	5V Operation Auto Increment Microwire Serial Interface	2
XL 93C46	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
3V-5V								
XL 93C46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	3V-5V Operation Auto Increment Microwire Serial Interface	2
XL 93C46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
5V — with Security								
XL 93CS46	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	5V Operation Auto Increment Hard Security National Compatible	2
XL 93CS46	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
3V-5V — with Security								
XL 93CS46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	PDIP	8	3V-5V Operation Auto Increment Hard Security National Compatible	2
XL 93CS46-3	1K (64x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		

Serial 2K CMOS E²PROMs

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Max. Clock	Package Type	Number of Pins	Features	Section
5V — With Advanced Features								
XL 93LC56	2K (128x16)	S,E	2mA/2µA	1 MHz	PDIP	8	5V Operation Auto Increment V_{CC} Lockout Microwire Serial Interface Low Power Consumption	2
XL 93LC56	2K (128x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
XL 93LC56	2K (128x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8		
XL 93LC56	2K (128x16)	S,E	2mA/2µA	1 MHz	DIE	8		
3V-5V — With Advanced Features								
XL 93LC56-3	2K (128x16)	S,E	2mA/2µA	1 MHz	PDIP	8	3V to 5V Operation Auto Increment Microwire Serial Interface Low Power Consumption	2
XL 93LC56-3	2K (128x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
XL 93LC56-3	2K (128x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8		
XL 93LC56-3	2K (128x16)	S,E	2mA/2µA	1 MHz	DIE	8		
5V								
XL 93C56	2K (128x16)	S,E	3mA/3µA	1 MHz	PDIP	8	5V Operation V_{CC} Lockout Microwire Serial Interface Low Power Consumption	2
XL 93C56	2K (128x16)	S,E	3mA/3µA	1 MHz	SOIC J	8		
XL 93C56	2K (128x16)	S,E	3mA/3µA	1 MHz	SOIC JR	8		
5V — Mitsubishi Compatible								
XL 90C21	2K (128x16)	S,E	3mA/3µA	1 MHz	PDIP	8	5V Operation Mitsubishi Compatible Interface Protocol	2
XL 90C21	2K (128x16)	S,E	3mA/3µA	1 MHz	SOIC J	8		

Serial E²PROMs — Microwire™ Bus Devices, continued

Serial 4K CMOS E²PROMs

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Max. Clock	Package Type	Number of Pins	Features	Section
5V — With Advanced Features								
XL 93LC66	4K (256x16)	S,E	2mA/2µA	1 MHz	PDIP	8	5V Operation Auto Increment Vcc Lockout Microwire Serial Interface Low Power Consumption	2
XL 93LC66	4K (256x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
XL 93LC66	4K (256x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8		
XL 93LC66	4K (256x16)	S,E	2mA/2µA	1 MHz	DIE	8		
3V-5V — With Advanced Features								
XL 93LC66-3	4K (256x16)	S,E	2mA/2µA	1 MHz	PDIP	8	3V to 5V Operation Auto Increment Microwire Serial Interface Low Power Consumption	2
XL 93LC66-3	4K (256x16)	S,E	2mA/2µA	1 MHz	SOIC J	8		
XL 93LC66-3	4K (256x16)	S,E	2mA/2µA	1 MHz	SOIC JR	8		
XL 93LC66-3	4K (256x16)	S,E	2mA/2µA	1 MHz	DIE	8		
5V								
XL 93C66	4K (256x16)	S,E	4mA/4µA	1 MHz	PDIP	8	5V Operation Microwire Serial Interface	2
XL 93C66	4K (256x16)	S,E	4mA/4µA	1 MHz	SOIC J	8		
5V — Mitsubishi Compatible								
XL 90C41	4K (256x16)	S,E	4mA/4µA	1 MHz	PDIP	8	5V Operation Mitsubishi Compatible Interface Protocol	2
XL 90C41	4K (256x16)	S,E	4mA/4µA	1 MHz	SOIC J	8		

Parallel E²PROMs-Byte-Wide Devices

4K NMOS Parallel E²PROMs

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Access Time (ns)	Package Type	Number of Pins	Features	Section
XL 2804A	4K (512x8)	S	80mA/40mA	250	PDIP	24		3

16K NMOS Parallel E²PROMs

XL 2816A	16K (2Kx8)	S,E	110mA/40mA	250	PDIP	24		3
XL 2816A	16K (2Kx8)	S,E	110mA/40mA	250	PLCC	32		
XL 2816A	16K (2Kx8)	S,E	110mA/40mA	250	CERDIP	24		
XL 28C16A	16K (2Kx8)	S,E	30mA/100µA	100	PDIP	24	$\overline{\text{DATA}}$ Polling	3
XL 28C16A	16K (2Kx8)	S,E	30mA/100µA	100	PDIP (P3)	24		
XL 28C16A	16K (2Kx8)	S,E	30mA/100µA	100	PLCC	32		
XL 28C16A	16K (2Kx8)	S,E	30mA/100µA	100	SOIC J	24		
XL 28C16A	16K (2Kx8)	S,E	30mA/100µA	100	CERDIP	24		
XL 28C16B	16K (2Kx8)	S,E	30mA/100µA	100	PDIP	24	$\overline{\text{DATA}}$ Polling 16 Byte Page Mode	3
XL 28C16B	16K (2Kx8)	S,E	30mA/100µA	100	PDIP (P3)	24		
XL 28C16B	16K (2Kx8)	S,E	30mA/100µA	100	PLCC	32		
XL 28C16B	16K (2Kx8)	S,E	30mA/100µA	100	SOIC J	24		
XL 28C16B	16K (2Kx8)	S,E	30mA/100µA	100	CERDIP	24		

16K High Speed CMOS Parallel E²PROMs

XL 46C15	16K (2Kx8)	S,E	90mA/35mA	55	PDIP	24	Bipolar PROM Replacement Pin for Pin	3
XL 46C15	16K (2Kx8)	S,E	90mA/35mA	55	PDIP (P3)	24		
XL 46C15	16K (2Kx8)	S,E	90mA/35mA	55	CERDIP	24		

XL Product	Size (organization)	Temp. Range	Icc (max/stby)	Access Time (ns)	Package Type	Number of Pins	Features	Section

Parallel E²PROMs-Byte-Wide Devices, continued

64K NMOS Parallel E²PROMs

XL 2864A	64K (8Kx8)	S,E	100mA/50mA	250	PDIP	28	$\overline{\text{DATA}}$ Polling 32 Byte Page Mode	3
XL 2864A	64K (8Kx8)	S,E	100mA/50mA	250	PLCC	32		
XL 2864A	64K (8Kx8)	S,E	100mA/50mA	250	SOIC J	28		
XL 2864A	64K (8Kx8)	S,E	100mA/50mA	250	CERDIP	28		
XL 2865A	64K (8Kx8)	S,E	100mA/50mA	250	PDIP	28	$\overline{\text{DATA}}$ Polling Ready/$\overline{\text{Busy}}$ 32 Byte Page Mode	3
XL 2865A	64K (8Kx8)	S,E	100mA/50mA	250	PLCC	32		
XL 2865A	64K (8Kx8)	S,E	100mA/50mA	250	SOIC J	28		
XL 2865A	64K (8Kx8)	S,E	100mA/50mA	250	CERDIP	28		

64K CMOS Parallel E²PROMs

XL 28C64	64K (8Kx8)	S,E	60mA/150µA	120	PDIP	28	$\overline{\text{DATA}}$ Polling 64 Byte Page Mode	3
XL 28C64	64K (8Kx8)	S,E	60mA/150µA	120	PLCC	32		
XL 28C64	64K (8Kx8)	S,E	60mA/150µA	120	SOIC J	28		
XL 28C64	64K (8Kx8)	S,E	30mA/150µA	120	CERDIP	28		
XL 28C64B	64K (8Kx8)	S,E	60mA/150µA	120	PDIP	28	$\overline{\text{DATA}}$ Polling Software Mode Control 64 Byte Page Mode	3
XL 28C64B	64K (8Kx8)	S,E	60mA/150µA	120	PDIP (P3)	28		
XL 28C64B	64K (8Kx8)	S,E	60mA/150µA	120	PLCC	32		
XL 28C64B	64K (8Kx8)	S,E	60mA/150µA	120	SOIC J	28		
XL 28C64B	64K (8Kx8)	S,E	60mA/150µA	120	CERDIP	28		

256K CMOS Parallel E²PROMs

XL 28C256	256K (32Kx8)	S,E	60mA/150µA	150	PDIP	28	Software Mode Control 64 Byte Page Mode Industry Standard Interface	3
XL 28C256	256K (32Kx8)	S,E	60mA/150µA	150	PLCC	32		
XL 28C256	256K (32Kx8)	S,E	60mA/150µA	150	CERDIP	28		

ERASIC - Multi-Level Programmable Logic

XL 78C800	800 Gate Equiv.	S,E	35mA	35	PDIP (P3)	24	ERASIC	5
XL 78C800	800 Gate Equiv.	S,E	35mA	35	PLCC	28		
AdET 1.0	Complete Software for E²PLD Design						Multi-Level Logic	

XL Product	Pgm Stor. ROM/E² (bytes)	RAM (Nibbles)	STOP Icc Stby. (Max)	HALT Icc Standby (Typ.) LCD On	Icc Operating (Typ.) 455KHz 1K Series R	Package Type	Number of Pins	Section
ASECs Application Specific Embedded Controllers								
XL2403	640	16	1µA at 3V	X	150µA at 3V	SOIC, SDIP	18	6
XL2418	1K	32	1µA at 3V	X	150µA at 3V	SOIC,SDIP	22	6
XL2421	1K	64	10µA at 5V	X	800µA at 5V	QFP, SDIP	32	6
XL24204 XL48E04	2K 8K E²	128 256	1µA at 3V	15µA at 3V	100µA at 3V	QFP	64	6
XL4407 XL48E07	4K 8K E²	128 256	1µA at 3V	15µA at 3V	100µA at 3V	QFP	64	6
XL4410 XL48E10	4K 8K E²	256 256	1µA at 3V	15µA at 3V	100µA at 3V	QFP	80	6
XL4805 XL48EO5	8K 8K E²	256 256	1µA at 3V	15µA at 3V	150µA at 3V	QFP	80	6

Ordering Information

XL S 93C46 P -3 *or* -150

Prefix
EXEL Product

Temperature Range*
S = Commercial
E = Industrial
M = Military
* Special ranges available by request.

Part Number

Serial:	24Cxx, 90C21, 90C41, 93Cxx, 93CSxx, 93LCxx
Parallel:	2804, 28C16x, 46C15, 2864A, 2865A, 28C64x, 28C256

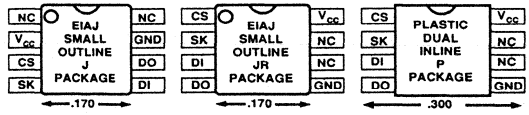
Voltage Designator
(Serial Only)
-3 = 3 to 5 Volts
Blank = 5 Volts

Package Type

Serial	***Parallel***
J = SOIC (EIAJ) 170 mil	C = CERDIP
JR = SOIC (EIAJ) 170 mil	D = PLCC
P = PDIP 300 mil	J = SOIC J
U = Die	P = PDIP 600 mil
	P3 = Plastic Skinny DIP 300 mil

Speed Grade
(Parallel Only)
-100 = 100ns
-120 = 120ns
-150 = 150ns
-200 = 200ns
-250 = 250ns
-300 = 300ns
-350 = 350ns

XL93xxxx Package/Pinout Family



Note: Slower versions of most devices are also available. Contact EXEL for details.
I²C™ is a trademark of Philips Corporation. Microwire™ is a trademark of National Semiconductor.

Dear Customer,

We are proud to present you with our 1993 *EXEL Microelectronics* databook. As we approach our tenth anniversary, *EXEL Microelectronics*, a subsidiary of ROHM Corporation, is dedicated to the design, manufacture and marketing of high-performance E^2 products. We have thrived under this charter and our databook reflects the result.

EXEL's technical staff has worked together to ensure that information contained in this reference guide is accurate and up-to-date. Inside, you'll find data sheets reflecting the latest technology in nonvolatile memories. We've expanded our commitment to serial E^2PROMs with the addition of I^2C devices, while continuing to supply our innovative XL93LCXX family. Our serial E^2PROMs provide the lowest possible operating voltage range and smallest current consumption, with stand-by current approaching zero, all housed in a space-saving surface mount package.

EXEL's product line continues to be exemplified by the XL28C64B and XL28C256 E^2PROMs. Key among user benefits of these devices is their *in-system* electrical (re-)programmability, low-power consumption, high reliability standards and wide-ranging packaging options. The innovative ASEC products combine advanced microcontroller technology and nonvolatile memory into a cost-effective application specific solution to your design problems.

When you purchase our products, you are engaging in a partnership with a company dedicated to delivering you the highest quality semiconductor devices at the lowest competitive price. We have invested many years and millions of dollars in our San Jose based E^2 fabrication facility. Consequently, we have the capacity to produce large volumes of high performance E^2 products. Our American-manufactured devices come with the *EXEL Microelectronics* quality guarantee. Our worldwide sales network is there to ensure your 100% satisfaction.

We anticipate that you'll find the answers to your E^2 application challenges within this book. If you have any questions, comments or technical service requirements, please call us directly.

The EXEL Microelectronics Technical Staff

SECTION 2 Table of Contents

I²C Family

Microwire Serial Family

Advance Information

1,024-Bit Serial Electrically Erasable PROM
3 Volt and 5 Volt Operation

FEATURES

- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2µA**
- **Two Voltage Ranges**
  - **— 2.7 to 5.5V**
  - **— 4.5 to 5.5V**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low Vcc lockout write protection (5V only)**
- **Internally Organized as 128 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **— Bidirectional data transfer protocol**
- **Four-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

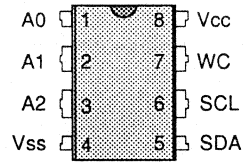
OVERVIEW

The XL24C01A is a low-cost 1,024-bit serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology and operates from a single 3 volt or 5 volt supply.

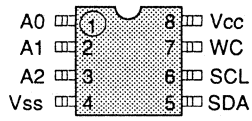
The XL24C01A is internally organized as a 128 x 8 memory bank. The XL24C01A features a serial interface and software protocol allowing operation on a simple two-wire bus (I^2C™). Up to eight XL24C01As may be connected to the 2-wire bus, by programming the A0, A1 and A2 inputs.

PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"JR" Package

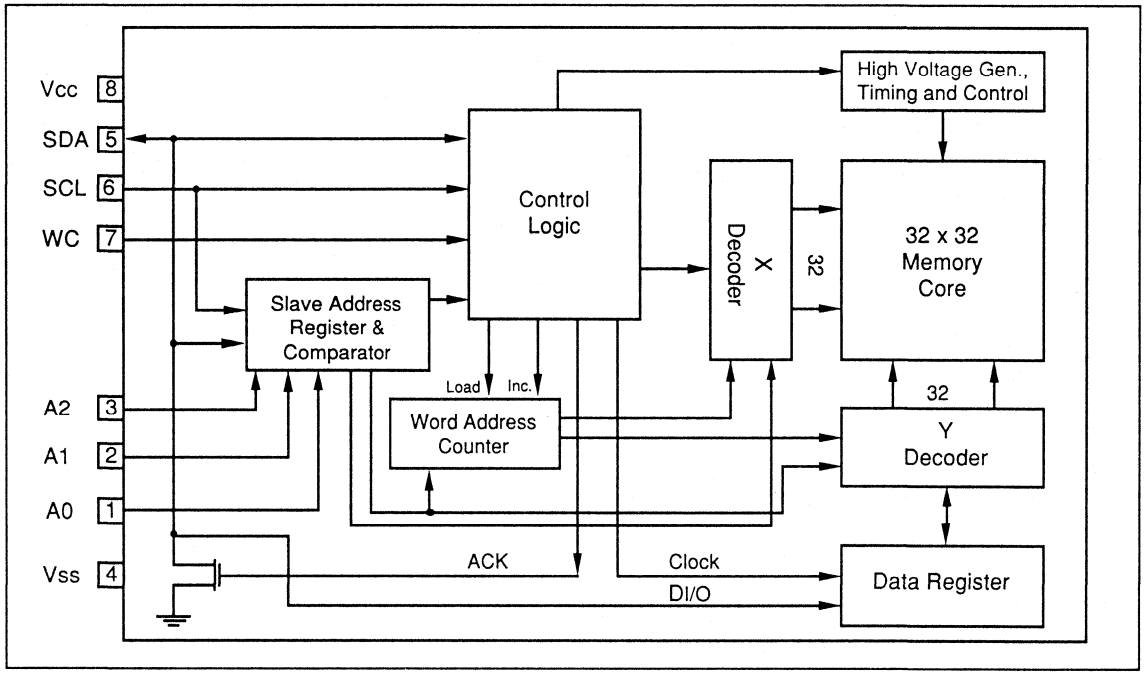


PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

Advance Information

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

A0, A1 and A2 - The address inputs are used to set the least significant three bits of the slave address. These inputs may be tied HIGH or LOW, or they may be actively driven. These inputs allow up to eight XL24C01A devices to be connected together on the bus.

Write Control (WC) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the memory is protected; when LOW, the write function is normal.

ENDURANCE AND DATA RETENTION

The XL24C01A is designed for applications requiring up to 100,000 write cycles and unlimited read cycles. It provides ten years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C01A is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

Vcc Lockout — Inadvertent WRITE Protection (5V parts only)

To insure against inadvertent WRITE operations, the XL24C01A has been equipped with an internal Vcc sensor circuit, which inhibits data alteration when the supply voltage falls below V_{WI}. If the applied Vcc is below 3.0V (typical), the XL24C01A is inhibited from executing WRITE operations, thereby protecting the nonvolatile data from being altered inadvertently.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for 2-way, 2-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. Refer to Figure 1 below, "Typical System Configuration." Data transfer may be initiated only when the bus is "not busy," which is defined as both SCL and SDA inputs being HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line at this time will be interpreted as control signals. Refer to Figure 2 below.

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. Refer to Figure 3 below.

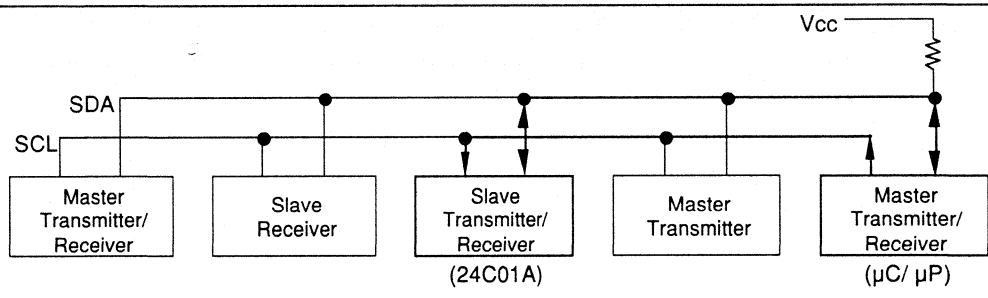


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

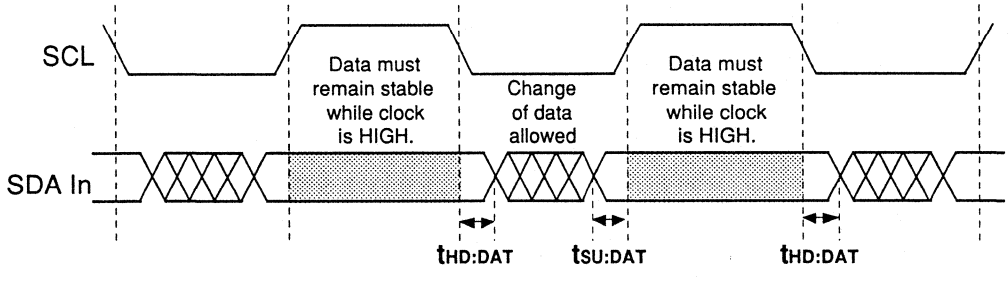


FIGURE 2. INPUT DATA PROTOCOL

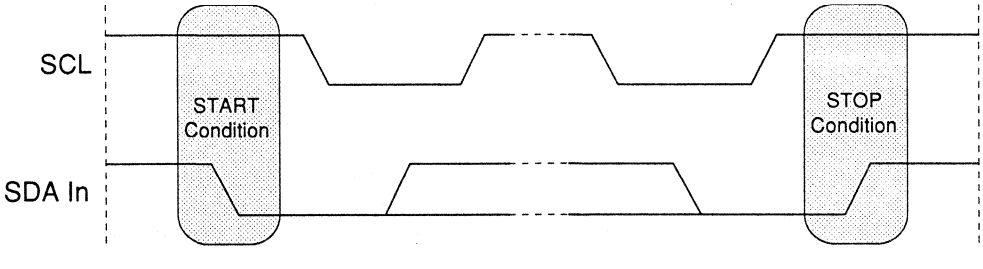


FIGURE 3. START AND STOP CONDITIONS

Advance Information

DEVICE OPERATION

The XL24C01A is a 1,024-bit serial E^2PROM. The device supports a bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter," and the receiving device as the "receiver." The device controlling the data transmission is the "master," and the controlled device is the "slave." In all cases, the XL24C01A will be a "slave" device, since it never initiates any data transfers.

Up to eight XL24C01As can be connected to the bus, selected by the A0, A1 and A2 device inputs. A0, A1 and A2 must be connected to either Vcc or Vss. A0, A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C01A will respond with an ACKnowledge after recognition of a START condition and its slave address. If both the device and a WRITE operation have been selected, the XL24C01A will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C01A will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C01A will continue to transmit data. If an ACKnowledge is not detected, the XL24C01A will terminate further data transmissions. The master must then issue a STOP condition to return the XL24C01A to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the address of the slave that it is accessing. The most significant four bits of the slave address are the "device type identifier." For an I^2C™ memory device, this is fixed as 1010. Refer to Figure 5 below.

The next three significant address bits address a particular device. A system may have up to eight XL24C01A devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to "1," a READ operation is selected; when set to "0," a WRITE operation is selected.

Device Type Identifier				Device Address			Read/ Write
1	0	1	0	A2	A1	A0	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

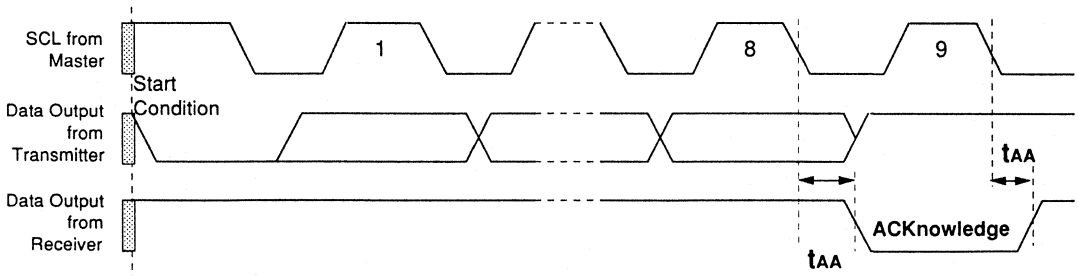


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

Byte WRITE

For a WRITE operation, the XL24C01A requires a second address field. This address field is the word address, comprised of eight bits, which provides access to any one of the 128 words of memory.

Upon receipt of the word address, the XL24C01A responds with an ACKnowledge, and waits for the next eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C01A begins the internal WRITE cycle to the nonvolatile array.

While the internal WRITE cycle is in progress, the XL24C01A inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

Page WRITE

The XL24C01A is capable of a 4-byte page-WRITE operation. It is initiated in the same manner as the byte-WRITE operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the XL24C01A will respond with an ACKnowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than four words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-WRITE operation, all inputs are disabled until completion of the internal WRITE cycle. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

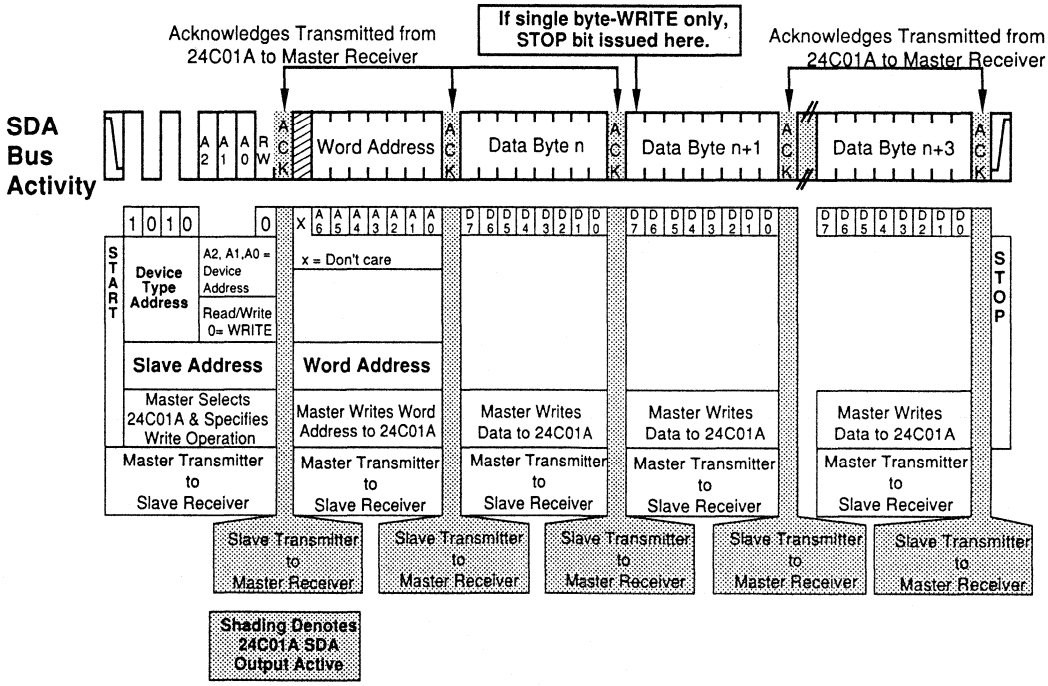


FIGURE 6. PAGE WRITE MODE

Advance Information

Acknowledge Polling

When the XL24C01A is performing an internal WRITE operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation. Refer to Figure 7 below.

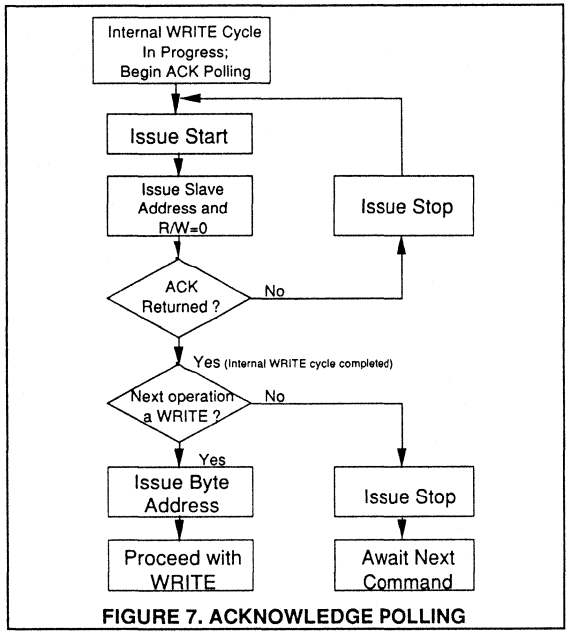


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

READ operations are initiated in the same manner as WRITE operations, except that the R/W bit of the slave address byte is set to "1." There are four different READ operation options:

1. Current Address Byte READ
2. Random Address Byte READ
3. Current Address Sequential READ
4. Random Address Sequential READ

Current Address Byte READ

The XL24C01A contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a READ or a WRITE) was to address n, the next READ operation would access data from address n+1, and update the current address pointer. When the XL24C01A receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address READ operation only accesses a single byte of data, the master does not acknowledge the transfer, but does generate a STOP condition. At this point, the XL24C01A discontinues transmission. See Figure 8 below for the address, acknowledge, and data transfer sequence.

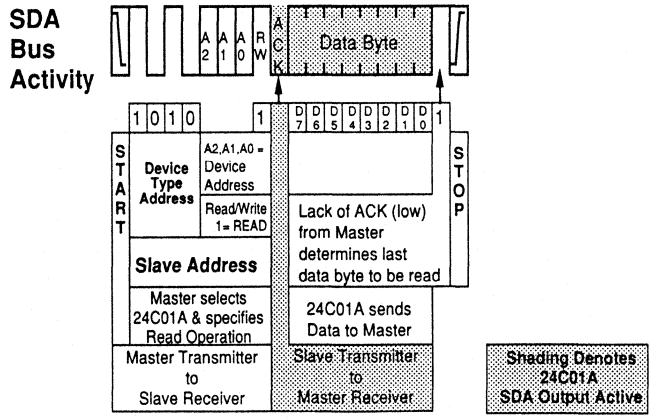


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

SERIAL 2 P'DCTS

READ OPERATIONS (continued)

Random Address Byte READ

Random address READ operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a WRITE command which includes the START condition and the slave address field (with the R/W bit set to "0"), followed by the address of the word it is to READ. This procedure sets the internal address counter of the XL24C01A to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to "1." The XL24C01A will respond with an acknowledge and transmit the eight data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the STOP condition. The XL24C01A discontinues transmission and reverts to its standby power mode. See Figure 9 below for the address, acknowledge, and data transfer sequence.

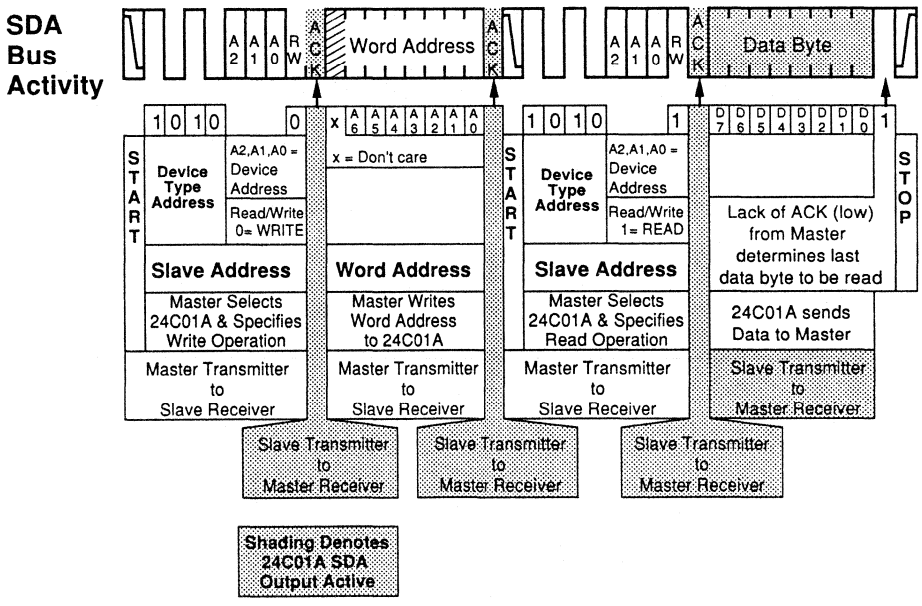


FIGURE 9. RANDOM ACCESS BYTE READ MODE

READ OPERATIONS (continued)

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes; however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C01A. The XL24C01A continues to output data for each ACKnowledge received. The sequential READ operation is terminated by the master, by not responding with an ACKnowledge, and by issuing a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for READ operations increments automatically, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 127), the counter "rolls over" to address 0, and the XL24C01A continues to output data for each ACKnowledge received.

Refer to Figure 10 below for the address, ACKnowledge, and data transfer sequence. Figure 10 shows a sequential READ starting with a random address. A sequential READ may also begin with a current address READ.

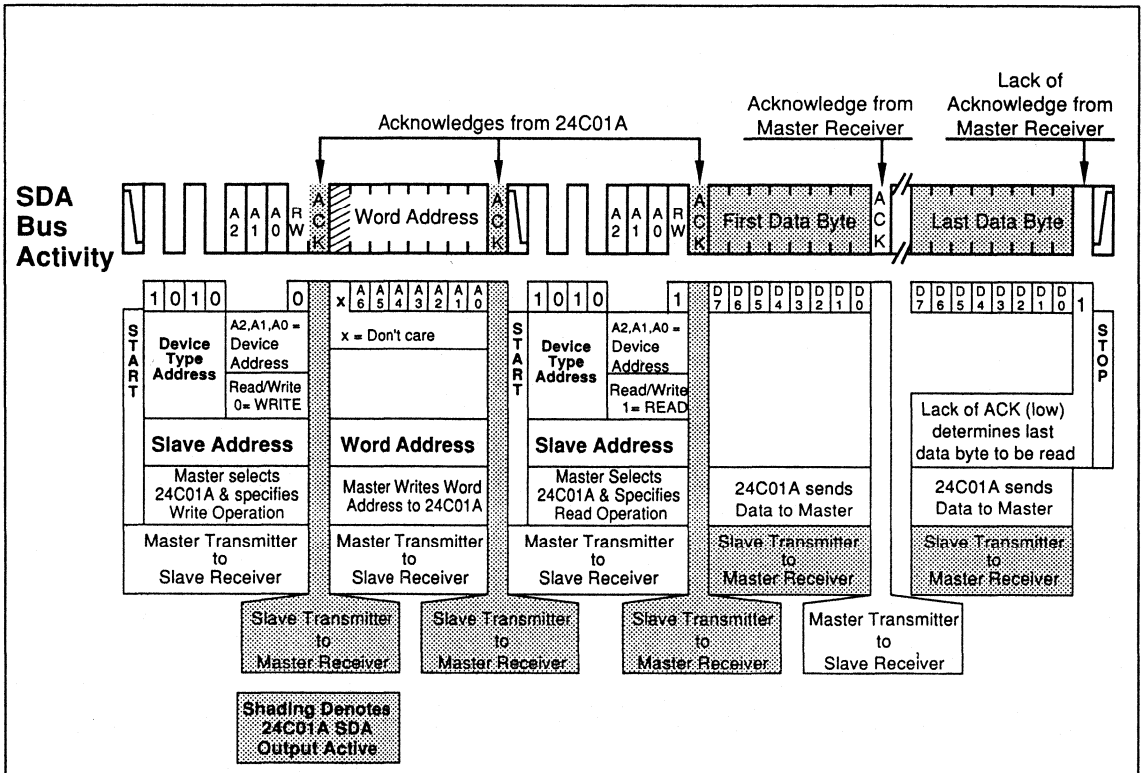


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds).....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
ESD Voltage (JEDEC method) 2,000V
Output Current .....+5mA

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C01A or -40°C to +85°C for the XLE24C01A, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = Vcc All other inputs = GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0 to Vcc			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 to Vcc			10	µA
V_{IL}	Input Low Voltage	A0-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A0-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V
V_{WI}	Write Inhibit Voltage	(5 volt part only)	2.5	3.4	4.5	V

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

Advance Information

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C01A or -40°C to +85°C for the XLE24C01A, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1000	ns
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time Constant @ SCL, SDA Inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

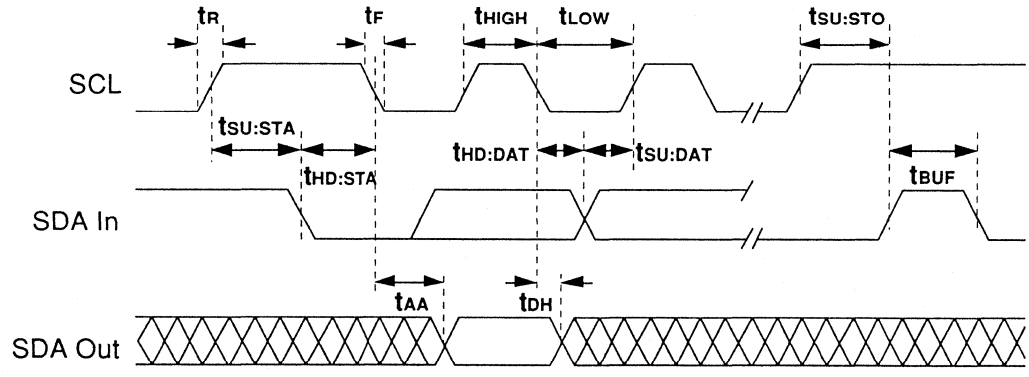


FIGURE 11. BUS TIMING

Advance Information

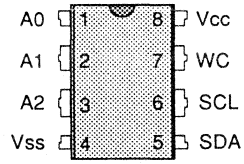
2,048-Bit Serial Electrically Erasable PROM
3 Volt and 5 Volt Operation

FEATURES

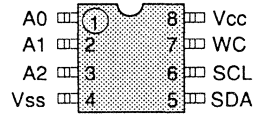
- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2μA**
- **Two Voltage Ranges**
  - **— 2.7 to 5.5V**
  - **— 4.5 to 5.5V**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low Vcc lockout write protection (5V only)**
- **Internally Organized as 256 x 8**
- **Two Wire Serial Interface (I^2C^{TM})**
  - **— Bidirectional data transfer protocol**
- **Four-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



EIAJ Small Outline "JR" Package



OVERVIEW

The XL24C02 is a low-cost 2,048-bit serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology and operates from a single 3 volt or 5 volt supply.

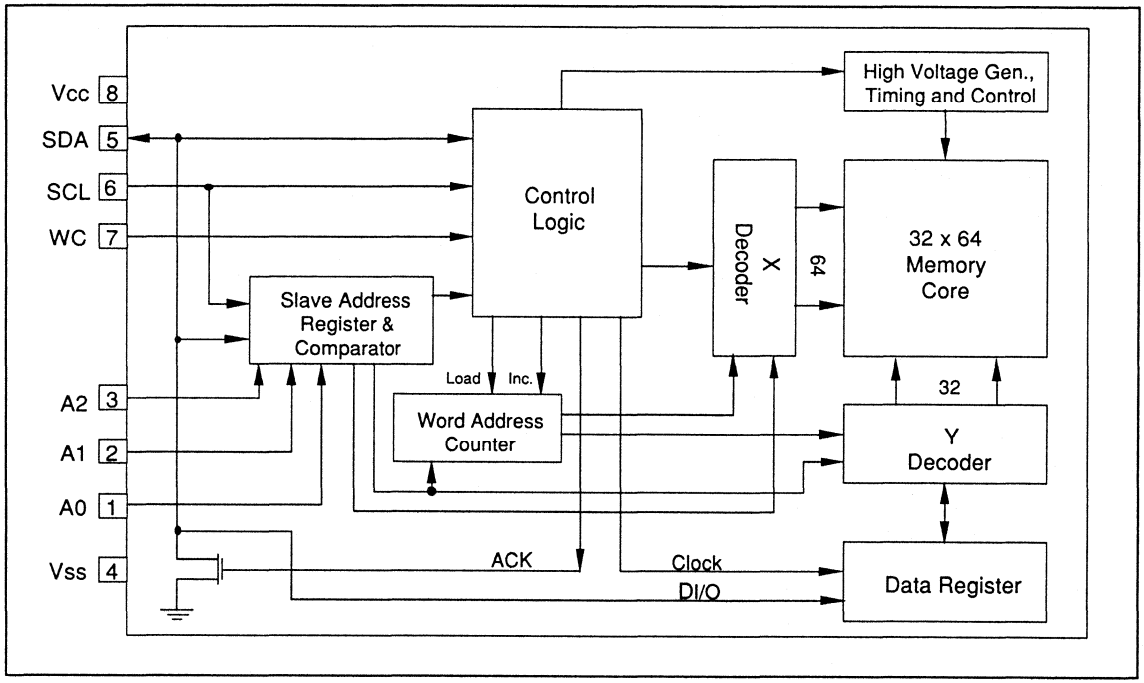
The XL24C02 is internally organized as a 256 x 8 memory bank. The XL24C02 features a serial interface and software protocol allowing operation on a simple two-wire bus (I^2C^{TM}). Up to eight XL24C02s may be connected to the 2-wire bus, by programming the A0, A1 and A2 inputs.

PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

Advance Information

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

A0, A1 and A2 - The address inputs are used to set the least significant three bits of the slave address. These inputs may be tied HIGH or LOW, or they may be actively driven. These inputs allow up to eight XL24C02 devices to be connected together on the bus.

Write Control (WC) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the memory is protected; when LOW, the write function is normal.

ENDURANCE AND DATA RETENTION

The XL24C02 is designed for applications requiring up to 100,000 write cycles and unlimited read cycles. It provides ten years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C02 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

Vcc Lockout — Inadvertent WRITE Protection (5V parts only)

To insure against inadvertent WRITE operations, the XL24C02 has been equipped with an internal Vcc sensor circuit, which inhibits data alteration when the supply voltage falls below V_{WI}. If the applied Vcc is below 3.0V (typical), the XL24C02 is inhibited from executing WRITE operations, thereby protecting the nonvolatile data from being altered inadvertently.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for 2-way, 2-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. Refer to Figure 1 below, "Typical System Configuration." Data transfer may be initiated only when the bus is "not busy," which is defined as both SCL and SDA inputs being HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line at this time will be interpreted as control signals. Refer to Figure 2 below.

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. Refer to Figure 3 below.

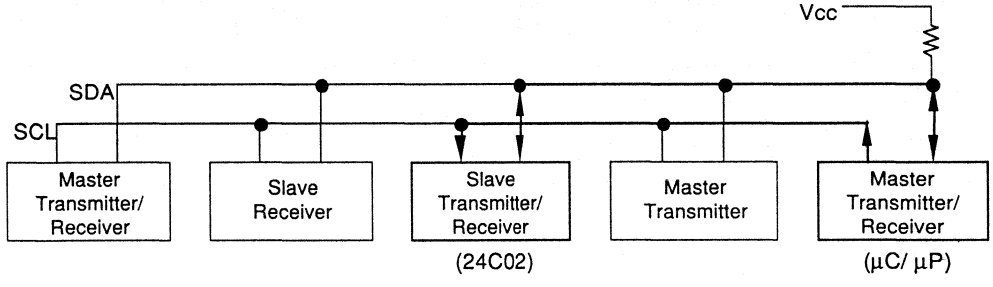


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

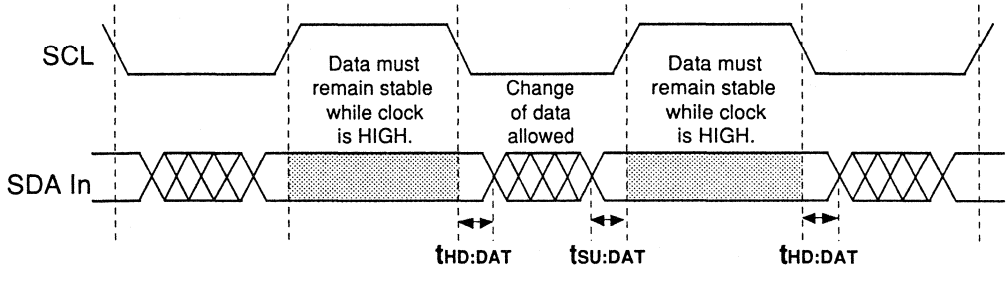


FIGURE 2. INPUT DATA PROTOCOL

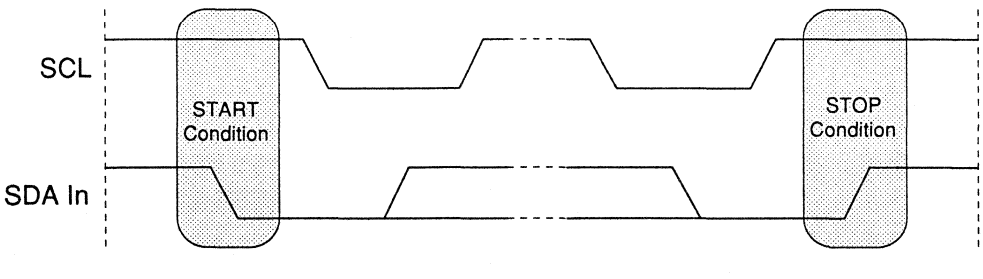


FIGURE 3. START AND STOP CONDITIONS

Advance Information

DEVICE OPERATION

The XL24C02 is a 2,048-bit serial E²PROM. The device supports a bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter," and the receiving device as the "receiver." The device controlling the data transmission is the "master," and the controlled device is the "slave." In all cases, the XL24C02 will be a "slave" device, since it never initiates any data transfers.

Up to eight XL24C02s can be connected to the bus, selected by the A0, A1 and A2 device inputs. A0, A1 and A2 must be connected to either Vcc or Vss. A0, A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C02 will respond with an ACKnowledge after recognition of a START condition and its slave address. If both the device and a WRITE operation have been selected, the XL24C02 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C02 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C02 will continue to transmit data. If an ACKnowledge is not detected, the XL24C02 will terminate further data transmissions. The master must then issue a STOP condition to return the XL24C02 to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the address of the slave that it is accessing. The most significant four bits of the slave address are the "device type identifier." For an I²C™ memory device, this is fixed as 1010. Refer to Figure 5 below.

The next three significant address bits address a particular device. A system may have up to eight XL24C02 devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to "1," a READ operation is selected; when set to "0," a WRITE operation is selected.

Device Type Identifier				Device Address			Read/ Write
1	0	1	0	A2	A1	A0	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

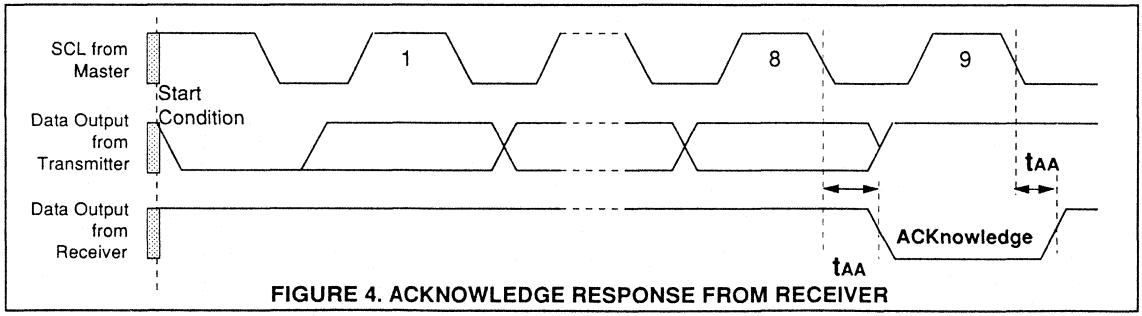


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

Byte WRITE

For a WRITE operation, the XL24C02 requires a second address field. This address field is the word address, comprised of eight bits, which provides access to any one of the 256 words of memory.

Upon receipt of the word address, the XL24C02 responds with an ACKnowledge, and waits for the next eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C02 begins the internal WRITE cycle to the nonvolatile array.

While the internal WRITE cycle is in progress, the XL24C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

Page WRITE

The XL24C02 is capable of a 4-byte page-WRITE operation. It is initiated in the same manner as the byte-WRITE operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the XL24C02 will respond with an ACKnowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order six bits of the address remain constant. If the master should transmit more than four words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-WRITE operation, all inputs are disabled until completion of the internal WRITE cycle. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

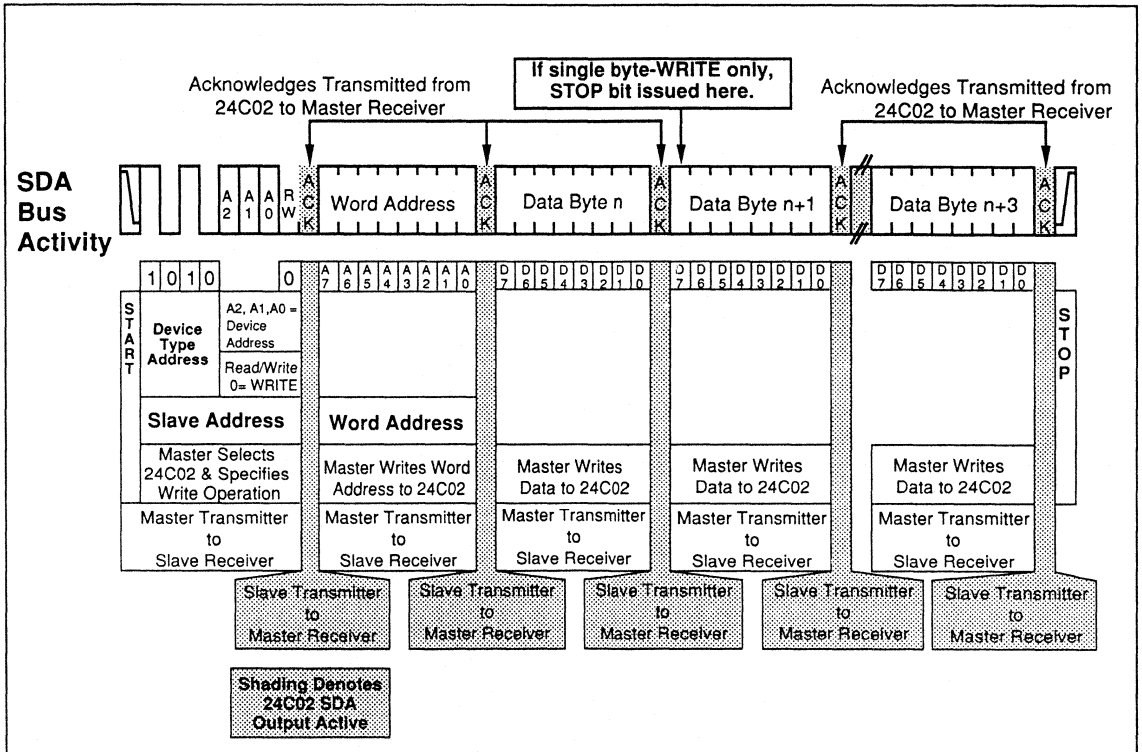


FIGURE 6. PAGE WRITE MODE

Acknowledge Polling

When the XL24C02 is performing an internal WRITE operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation. Refer to Figure 7 below.

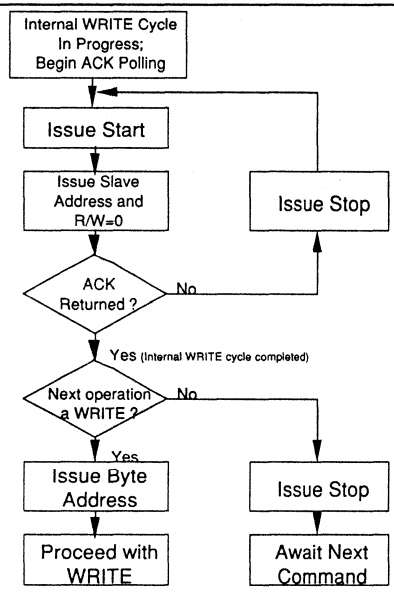


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

READ operations are initiated in the same manner as WRITE operations, except that the R/W bit of the slave address byte is set to "1." There are four different READ operation options:

1. Current Address Byte READ
2. Random Address Byte READ
3. Current Address Sequential READ
4. Random Address Sequential READ

Current Address Byte READ

The XL24C02 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a READ or a WRITE) was to address n, the next READ operation would access data from address n+1, and update the current address pointer. When the XL24C02 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address READ operation only accesses a single byte of data, the master does not acknowledge the transfer, but does generate a STOP condition. At this point, the XL24C02 discontinues transmission. See Figure 8 below for the address, acknowledge, and data transfer sequence.

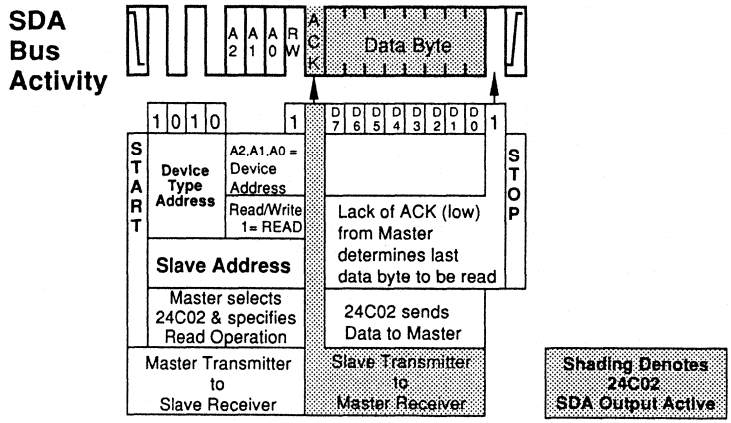


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

READ OPERATIONS (continued)

Random Address Byte READ

Random address READ operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a WRITE command which includes the START condition and the slave address field (with the R/W bit set to "0"), followed by the address of the word it is to READ. This procedure sets the internal address counter of the XL24C02 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to "1." The XL24C02 will respond with an acknowledge and transmit the eight data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the STOP condition. The XL24C02 discontinues transmission and reverts to its standby power mode. See Figure 9 below for the address, acknowledge, and data transfer sequence.

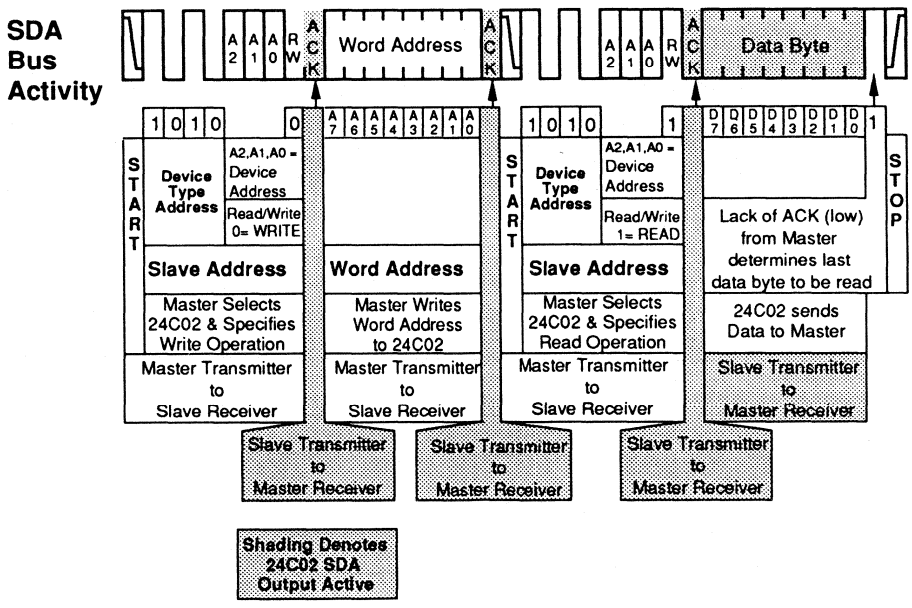


FIGURE 9. RANDOM ACCESS BYTE READ MODE

READ OPERATIONS (continued)

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes; however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C02. The XL24C02 continues to output data for each ACKnowledge received. The sequential READ operation is terminated by the master, by not responding with an ACKnowledge, and by issuing a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for READ operations increments automatically, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter "rolls over" to address 0, and the XL24C02 continues to output data for each ACKnowledge received.

Refer to Figure 10 below for the address, ACKnowledge, and data transfer sequence. Figure 10 shows a sequential READ starting with a random address. A sequential READ may also begin with a current address READ.

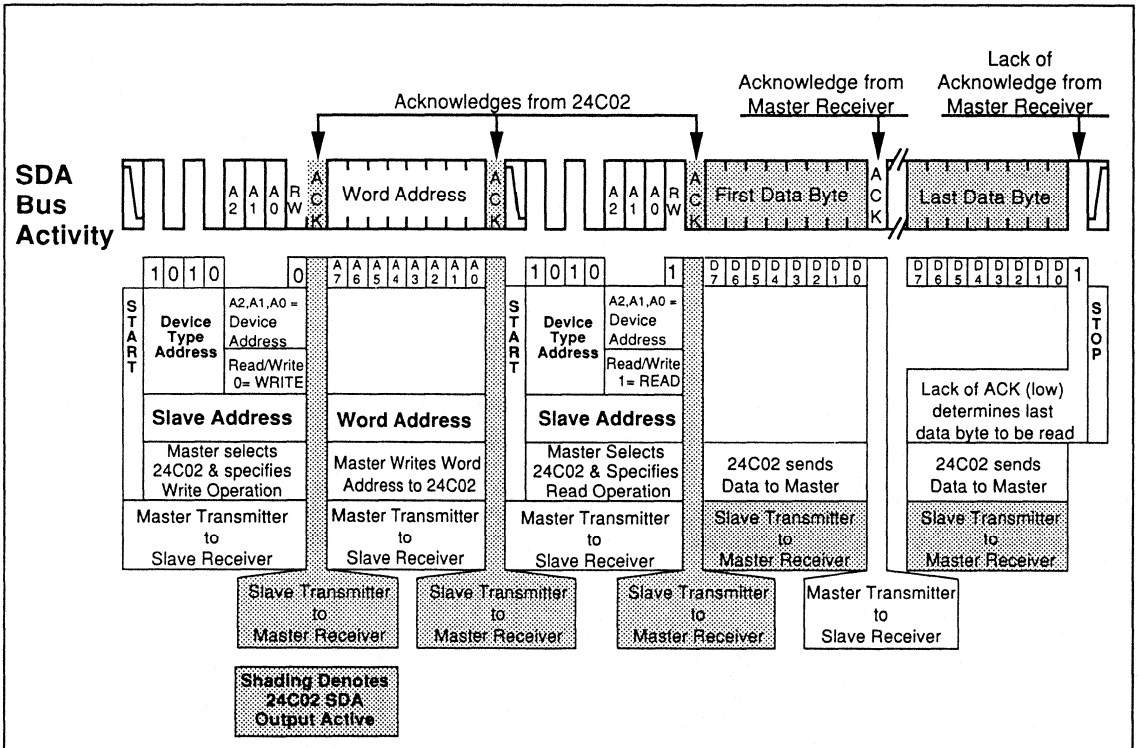


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds) .....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
ESD Voltage (JEDEC method) 2,000V
Output Current .....+5mA

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C02 or -40°C to +85°C for the XLE24C02, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = Vcc All other inputs = GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0 to Vcc			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 to Vcc			10	µA
V_{IL}	Input Low Voltage	A0-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A0-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V
V_{WI}	Write Inhibit Voltage	(5 volt part only)	2.5	3.4	4.5	V

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

Advance Information

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C02 or -40°C to +85°C for the XLE24C02, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1000	ns
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time Constant @ SCL, SDA Inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

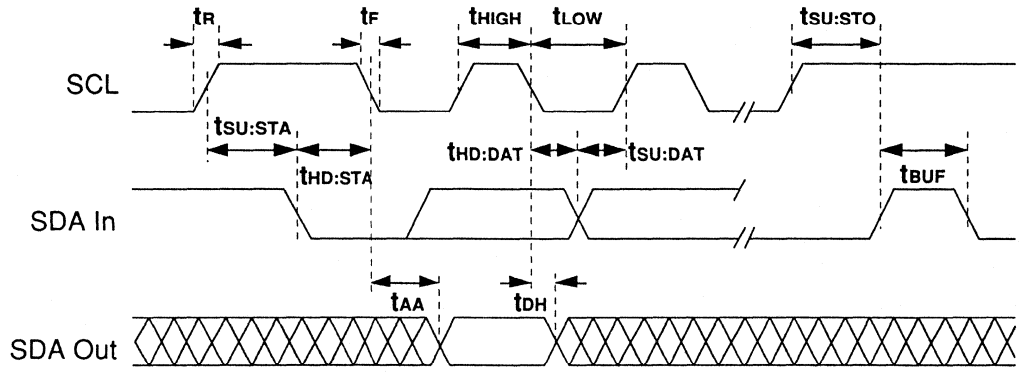


FIGURE 11. BUS TIMING

Preliminary

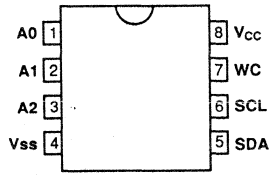
4,096-Bit Serial Electrically Erasable PROM
5 Volt Only Operation

FEATURES

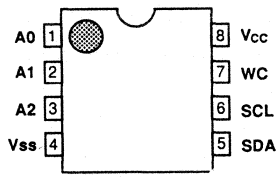
- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2µA**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low V_{CC} lockout write protection**
- **Internally Organized as Two Banks**
  - **— Each 256 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **—Bidirectional data transfer protocol**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 write cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"JR" Package



PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

OVERVIEW

The XL24C04 is a low-cost, 4,096-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The part operates from a single 5 volt supply.

The XL24C04 is internally organized as two 256 x 8 memory banks. The XL24C04 features the I^2C™serial interface and software protocol allowing operation on a simple two-wire bus. Up to four XL24C04s may be individually addressed on the two-wire bus by establishing their device address using the address input pins (A1 and A2).

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

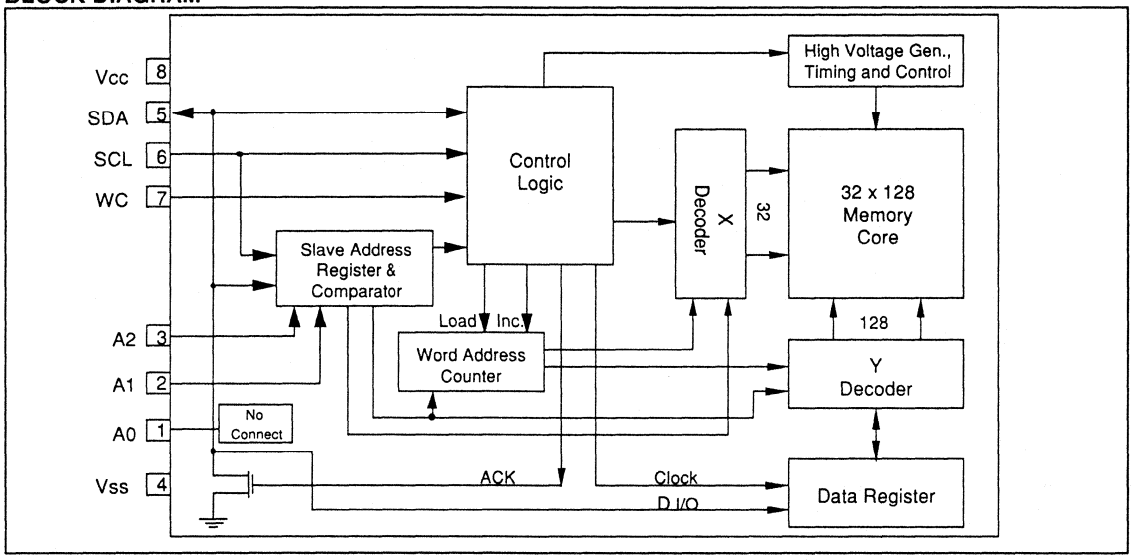
Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address (A0) - The A0 pin is not electrically connected to the XL24C04 device.

Address (A1, A2) - The address input pins are used to set the two-bit device address of the XL24C04 which will identify it on the two-wire bus. These inputs may be tied HIGH, LOW, or they may be actively driven. These inputs allow up to four XL24C04 devices to be distinguished on the bus.

Write Control (WC) - The Write Control input pin is used to disable the write circuitry to the memory. When HIGH, the write function is disabled, protecting data; when LOW, the write function is enabled.

BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL24C04 is designed for applications requiring up to 100,000 write cycles per bit and unlimited read cycles. It provides 10 years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C04 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving, 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. (See Figure 1.) Data transfer between devices may be initiated only when SCL and SDA are HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line when SCL is HIGH will be interpreted as control signals. (See Figure 2.)

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. (See Figure 3.)

DEVICE OPERATION

The XL24C04 is a 4,096-bit serial E²PROM. The device supports the I²C™ bidirectional data transmission protocol. The protocol defines any device sending data onto the bus as a "transmitter," and any device which is receiving data as a "receiver." The device controlling the data transmission is defined as the "master," and the controlled device is called the "slave." In all cases, the XL24C04 will be a "slave" device, since it never initiates any data transfers.

Up to four XL24C04s can be connected to the bus, selected by the A1 and A2 device addresses. A0 is not electrically connected. A1 and A2 must be connected to either V_{CC} or V_{SS}. A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

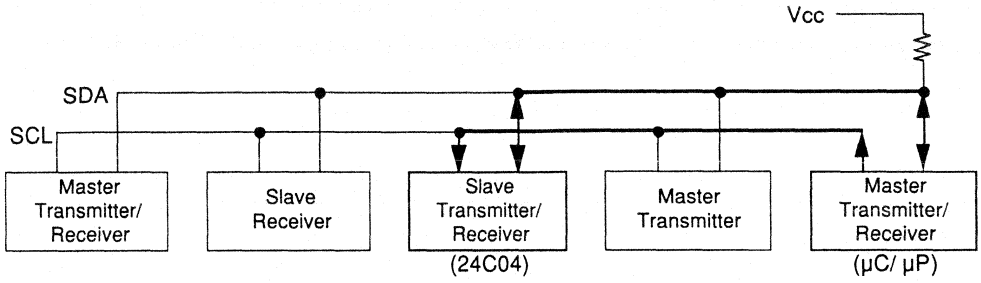


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

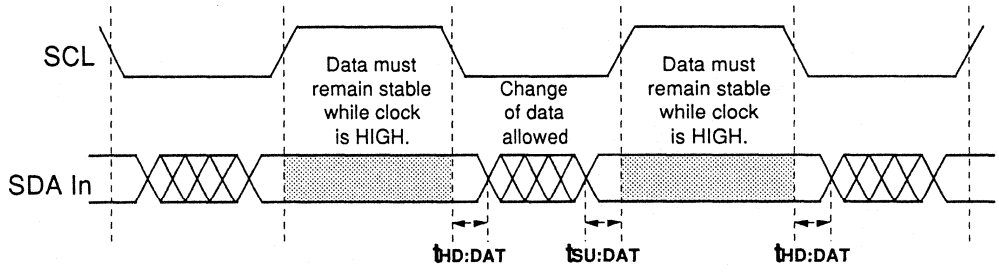


FIGURE 2. INPUT DATA PROTOCOL

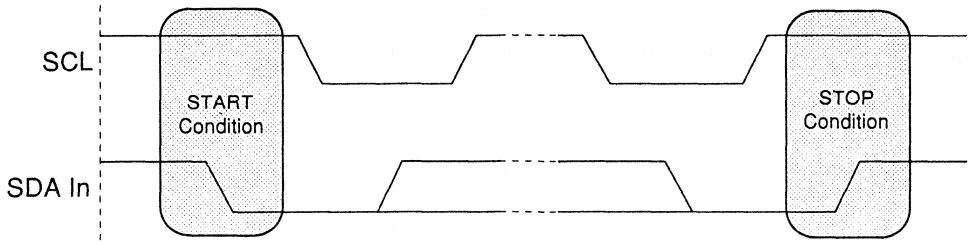


FIGURE 3. START AND STOP CONDITIONS

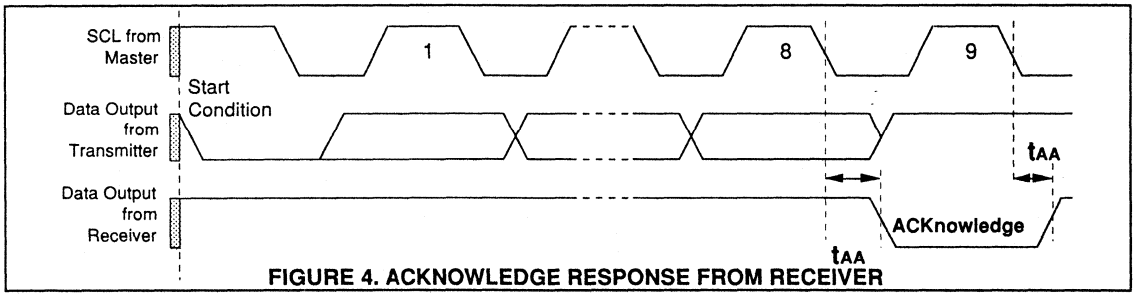


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Acknowledge (ACK)
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C04 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation have been selected, the XL24C04 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C04 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C04 will continue to transmit data. If an ACKnowledge is not detected, the XL24C04 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Slave Address Byte
Following a START condition, the master must output the device address of the slave to be accessed. The most significant four bits of the slave address are the "device type identifier." For the XL24C04 this is fixed as 1010. (See Figure 5.)

The next two bits (device address), address a particular device. Using this addressing scheme, a system may have up to four XL24C04 devices on the bus. The device address is defined by the state of the A1 and A2 input pins.

Bank Select Bit
The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Op Code
The last bit of the stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The XL24C04 allows two types of write operations: byte write and page write. The first writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows for a full 16-byte page to be stored during t_{WR}.

Byte Write
After the slave address is sent (to identify the slave device, select the bank and specify a read or write instruction), a second field is sent from the master to the slave. This field contains the word address and is comprised of eight bits providing access to any one of the 256 words in the bank.

Upon receipt of the word address, the XL24C04 responds with an ACKnowledge, and waits for the eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C04 begins the internal write cycle to the nonvolatile array.

While the internal write cycle is in progress, the XL24C04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Device Type Identifier				Device Address		Bank Select	Read/ Write
Slave Address							
1	0	1	0	A2	A1	BS (A8)	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

Page Write

The XL24C04 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words of data. After the receipt of each word, the XL24C04 will respond with an ACKnowledge.

The XL24C04 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

V_{CC} Lockout – Inadvertent Write Protection

To ensure against inadvertent write operations, the XL24C04 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below V_{WI}, the XL24C04 is inhibited from executing write operations, thereby protecting the nonvolatile data from inadvertent write operations.

READ OPERATIONS

Read operations are initiated in the same manner as write operations except that the R/W bit of the identification field is set to "1." There are four different read operation options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The XL24C04 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address n, the next read operation would access data from address n+1 and update the current address pointer. When the XL24C04 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address read operation only accesses a single byte of data, the master does not acknowledge the transfer but does generate a stop condition. At this point, the XL24C04 discontinues transmission. See Figure 7 for the address acknowledge and data transfer sequence.

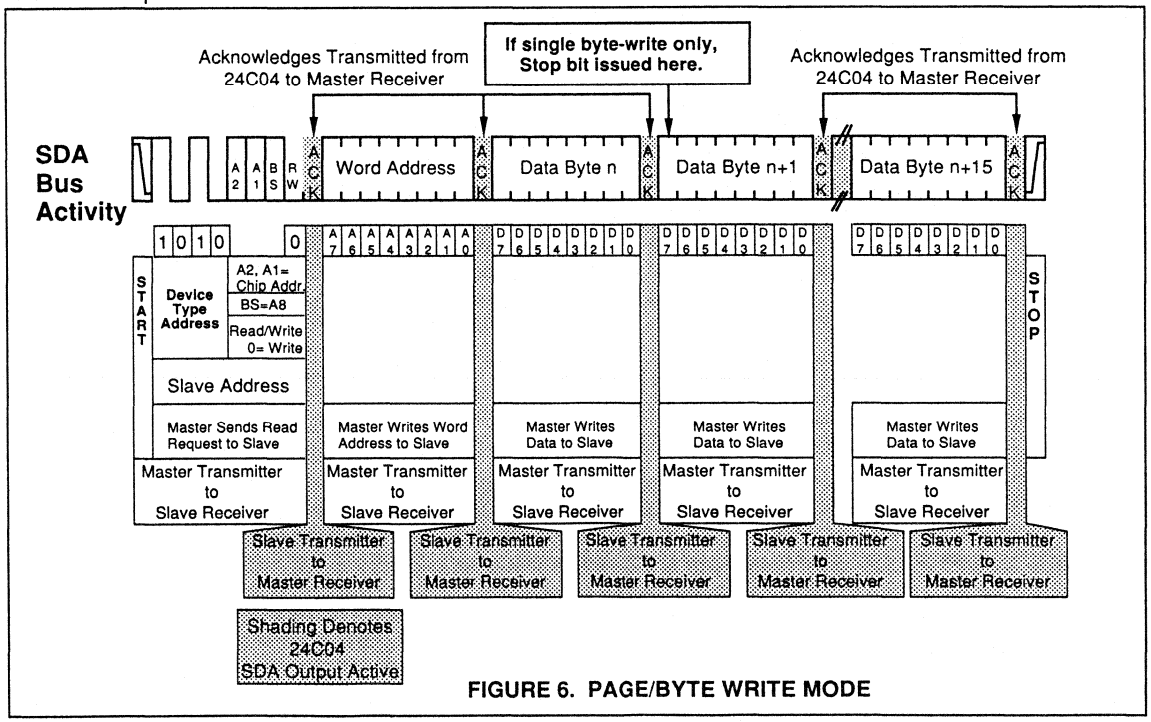


FIGURE 6. PAGE/BYTE WRITE MODE

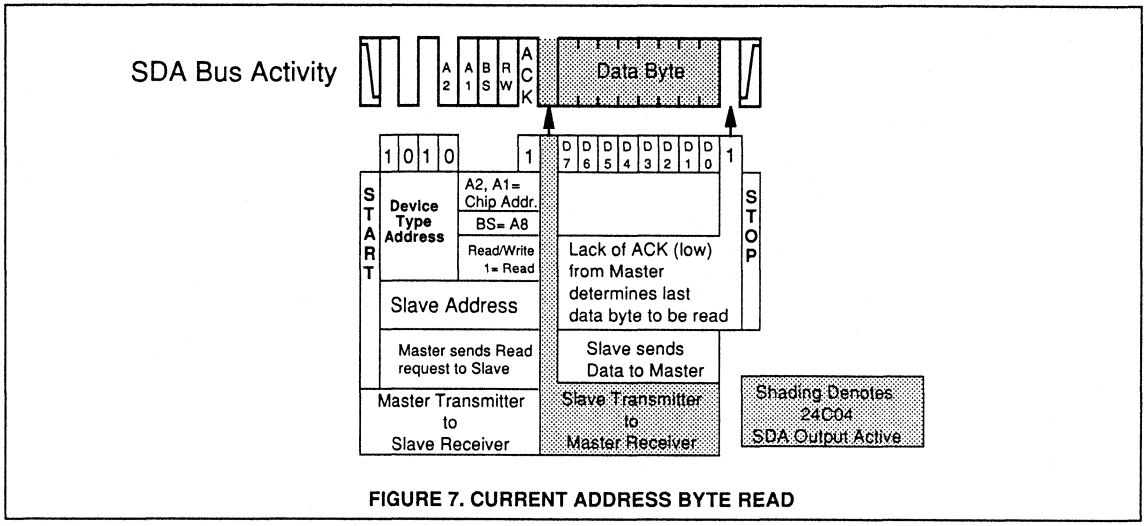


FIGURE 7. CURRENT ADDRESS BYTE READ

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to "0") followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C04 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to "1." The XL24C04 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The XL24C04 discontinues transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.

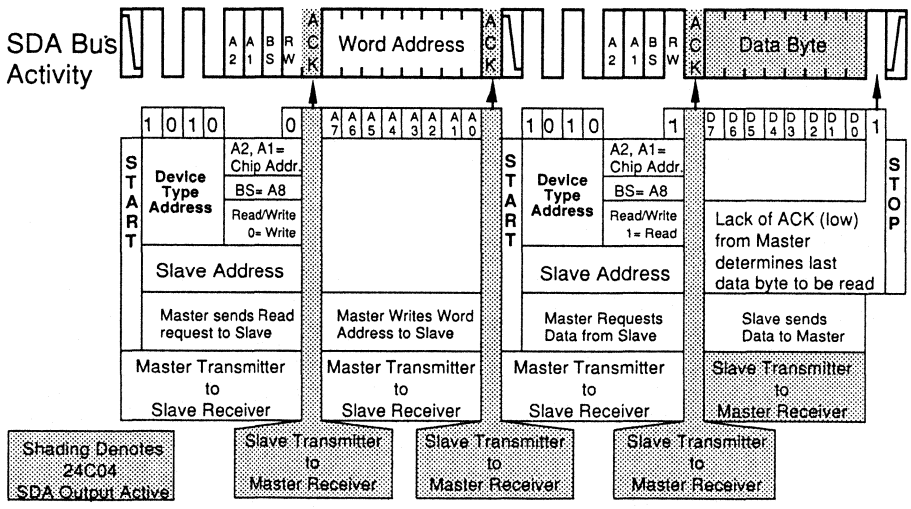


FIGURE 8. RANDOM ACCESS BYTE READ

Sequential Read

The sequential address read operation can be initiated as either a current address read or a random address read. The first data accessed is transmitted by the XL24C04 just as with other byte read modes; however, instead of responding with a stop condition, the master now responds with an acknowledge indicating it requires additional data from the XL24C04. The XL24C04 transmits a new byte of data for each acknowledge received. The sequential address read operation is terminated by the master withholding the acknowledge and generating a stop condition.

During the sequential address read operation, the internal address counter of the XL24C04 automatically increments with each acknowledge received, ensuring that the data from address n will be followed by the data from address n+1. For read operations, all bits of the address counter are incremented, allowing the entire array to be read using a single read command. When the counter reaches the top of the array, it will "roll over" to the bottom of the array and continue to transmit data for each acknowledge it receives. See Figure 9 for the address, acknowledge and data transfer sequence.

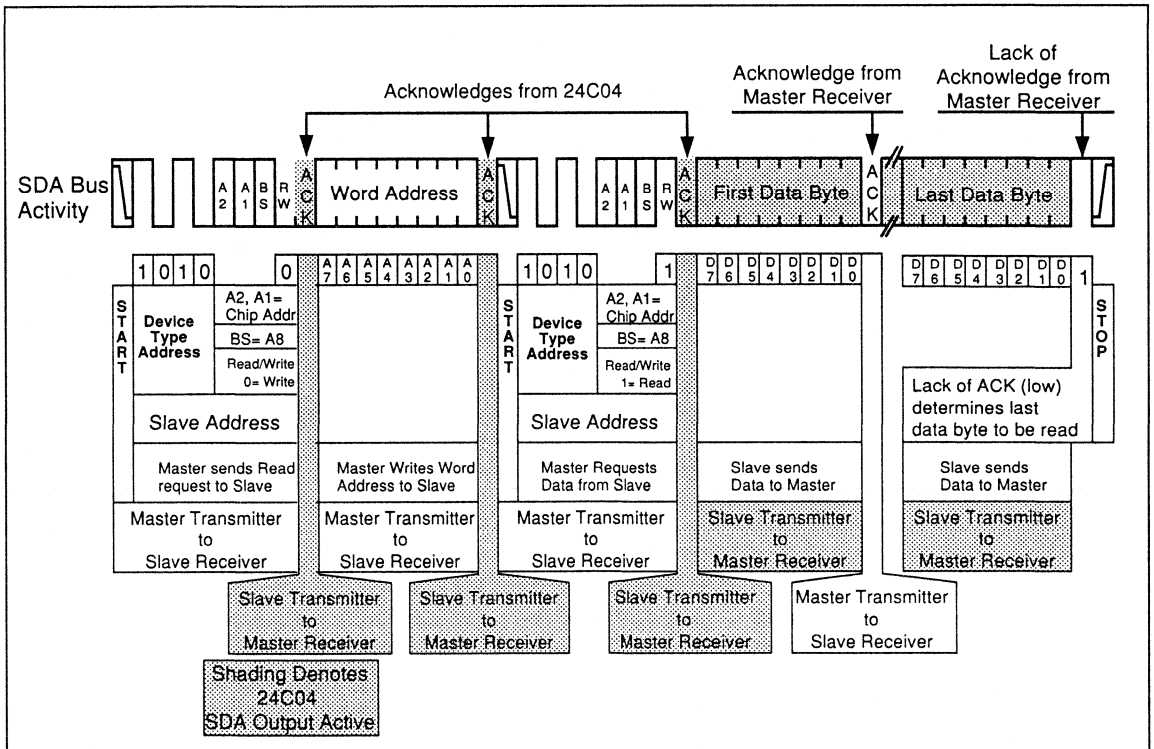


FIGURE 9. SEQUENTIAL READ (starting with a Random Address)

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds) .....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
Output Current .....+5mA
Electrostatic Discharge Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04 or -40°C to +85°C for the XLE24C04, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC1}	Supply Current (CMOS)	SCL=CMOS Levels @ 100KHz SDA=Open, all other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL=SDA=Vcc All other inputs=GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to 5V			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to 5V			10	µA
V_{IL}	Input Low Voltage	A1-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A1-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA (SDA only)			0.4	V
V_{WI}	Write Inhibit Voltage		2.5	3.4	4.5	V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04 or -40°C to +85°C for the XLE24C04, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1.0	µs
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time constant @ SCL, SDA inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

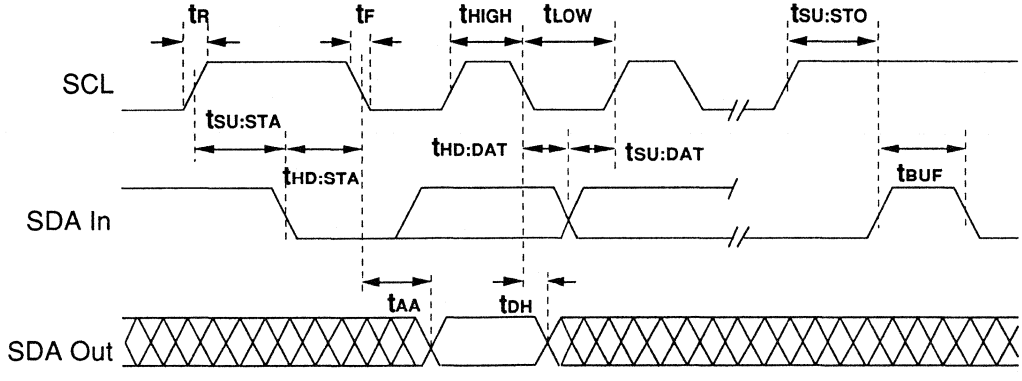


FIGURE 10. BUS TIMING

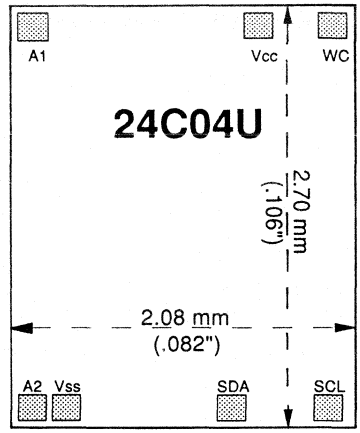
Preliminary

4,096-Bit Serial Electrically Erasable PROM
5 Volt Only Operation

FEATURES

- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2μA**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low V_{CC} lockout write protection**
- **Internally Organized as Two Banks**
  - **— Each 256 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **—Bidirectional data transfer protocol**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 write cycles per byte**
  - **— Data retention: 10 years**
- **Available in wafer form or in waffle pack**

DIE CONFIGURATION



PAD NAMES

A1	Address Input
A2	Address Input
V_{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{CC}	Supply Voltage

OVERVIEW

The XL24C04U is a low-cost, 4,096-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The part operates from a single 5 volt supply.

The XL24C04U is internally organized as two 256 x 8 memory banks. The XL24C04U features the I^2C™ serial interface and software protocol allowing operation on a simple two-wire bus. Up to four XL24C04Us may be individually addressed on the two-wire bus by establishing their device address using the address inputs (A1 and A2).

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

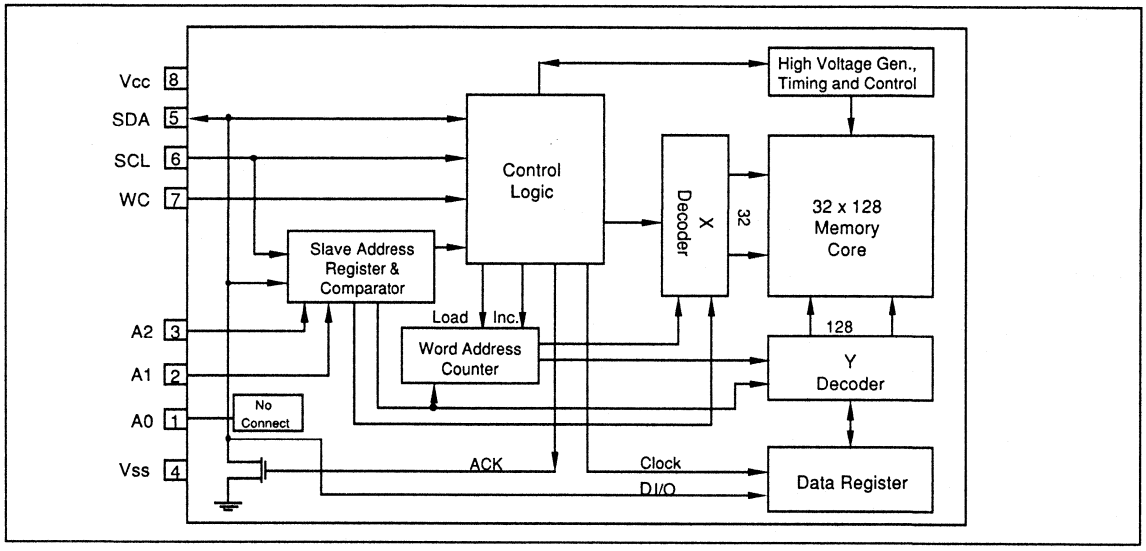
Serial Data (SDA) - The SDA pad is a bidirectional pad used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address (A0) - The A0 pad is non-existent on the XL24C04U device.

Address (A1, A2) - The address input pads are used to set the two-bit device address of the XL24C04U which will identify it on the two-wire bus. These inputs may be tied HIGH, LOW, or they may be actively driven. These inputs allow up to four XL24C04U devices to be distinguished on the bus.

Write Control (WC) - The Write Control input pad is used to disable the write circuitry to the memory. When HIGH, the write function is disabled, protecting data; when LOW, the write function is enabled.

BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL24C04U is designed for applications requiring up to 100,000 write cycles per bit and unlimited read cycles. It provides 10 years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C04U is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. (See Figure 1.) Data transfer between devices may be initiated only when SCL and SDA are HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line when SCL is HIGH will be interpreted as control signals. (See Figure 2.)

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. (See Figure 3.)

DEVICE OPERATION

The XL24C04U is a 4,096-bit serial E²PROM. The device supports the I²C™ bidirectional data transmission protocol. The protocol defines any device sending data onto the bus as a "transmitter," and any device which is receiving data as a "receiver." The device controlling the data transmission is defined as the "master," and the controlled device is called the "slave." In all cases, the XL24C04U will be a "slave" device, since it never initiates any data transfers.

Up to four XL24C04Us can be connected to the bus, selected by the A1 and A2 device addresses. A0 is not electrically connected. A1 and A2 must be connected to either V_{CC} or V_{SS}. A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

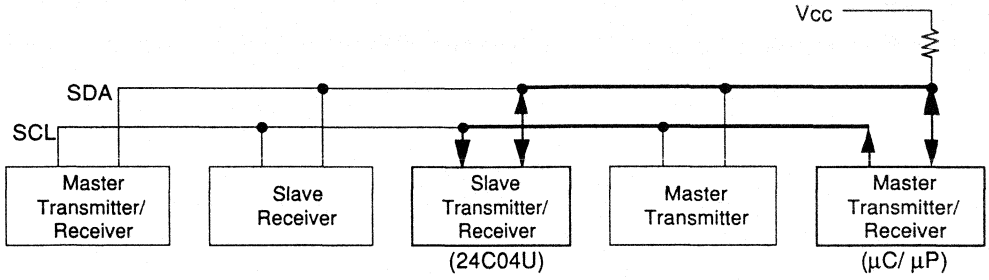


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

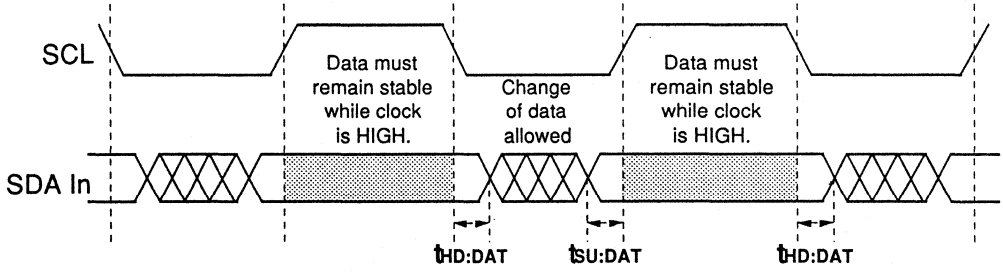


FIGURE 2. INPUT DATA PROTOCOL

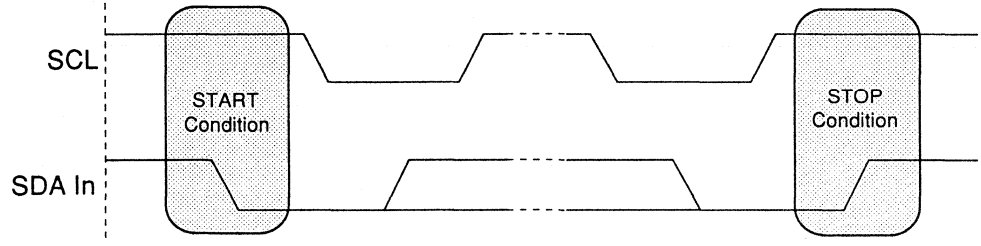


FIGURE 3. START AND STOP CONDITIONS

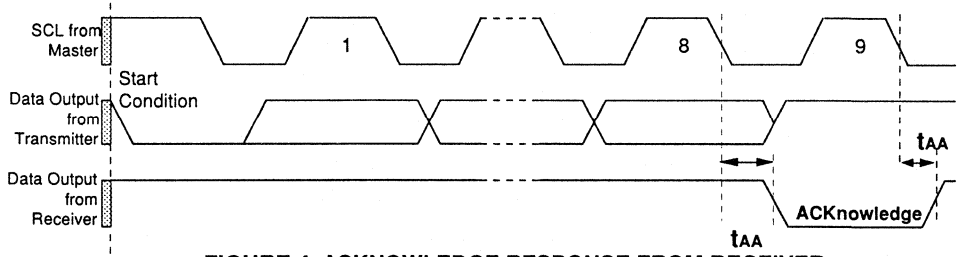


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Acknowledge (ACK)
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C04U will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation have been selected, the XL24C04U will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C04U will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C04U will continue to transmit data. If an ACKnowledge is not detected, the XL24C04U will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Slave Address Byte
Following a START condition, the master must output the device address of the slave to be accessed. The most significant four bits of the slave address are the "device type identifier." For the XL24C04U this is fixed as 1010. (See Figure 5.)

The next two bits (device address), address a particular device. Using this addressing scheme, a system may have up to four XL24C04U devices on the bus. The device address is defined by the state of the A1 and A2 input pins.

Bank Select Bit
The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Op Code
The last bit of the stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The XL24C04U allows two types of write operations: byte write and page write. The first writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows for a full 16-byte page to be stored during t_{WR}.

Byte Write
After the slave address is sent (to identify the slave device, select the bank and specify a read or write instruction), a second field is sent from the master to the slave. This field contains the word address and is comprised of eight bits providing access to any one of the 256 words in the bank.

Upon receipt of the word address, the XL24C04U responds with an ACKnowledge, and waits for the eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C04U begins the internal write cycle to the nonvolatile array.

While the internal write cycle is in progress, the XL24C04U inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Device Type Identifier				Device Address		Bank Select	Read/ Write
Slave Address							
1	0	1	0	A2	A1	BS (A8)	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

Page Write

The XL24C04U is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words of data. After the receipt of each word, the XL24C04U will respond with an ACKnowledge.

The XL24C04U automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

V_{CC} Lockout – Inadvertent Write Protection

To ensure against inadvertent write operations, the XL24C04U has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below V_{WI}, the XL24C04U is inhibited from executing write operations, thereby protecting the nonvolatile data from inadvertent write operations.

READ OPERATIONS

Read operations are initiated in the same manner as write operations except that the R/W bit of the identification field is set to "1." There are four different read operation options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The XL24C04U contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address n, the next read operation would access data from address n+1 and update the current address pointer. When the XL24C04U receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address read operation only accesses a single byte of data, the master does not acknowledge the transfer but does generate a stop condition. At this point, the XL24C04U discontinues transmission. See Figure 7 for the address acknowledge and data transfer sequence.

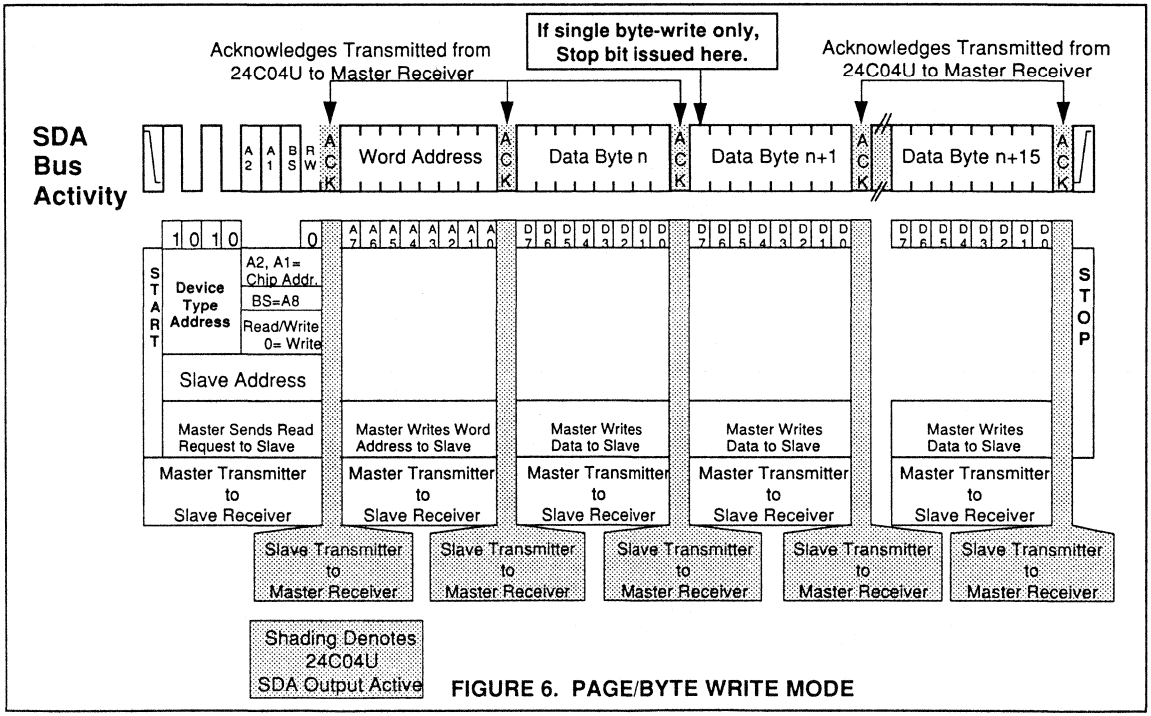


FIGURE 6. PAGE/BYTE WRITE MODE

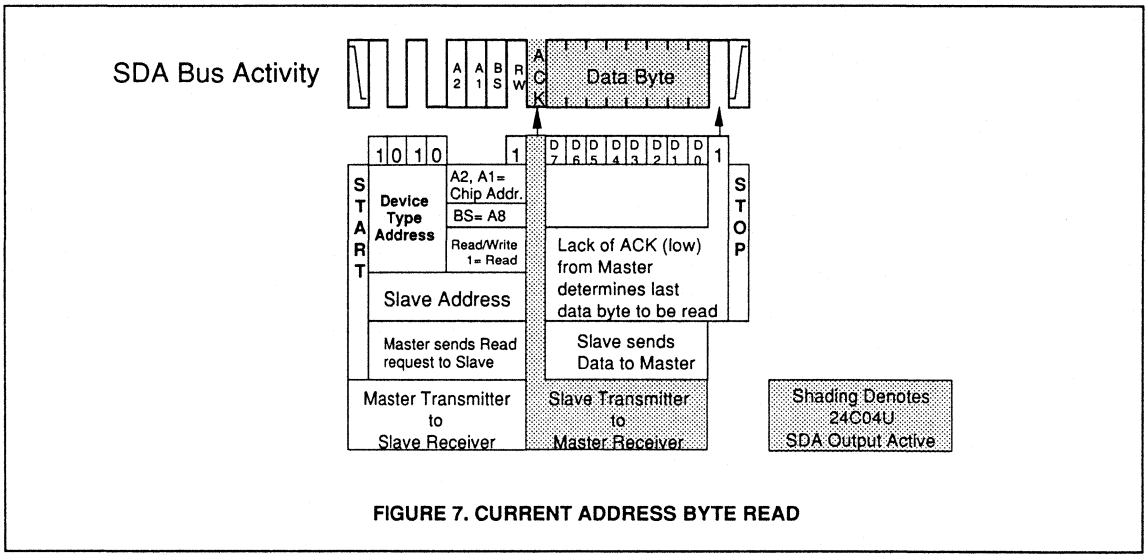


FIGURE 7. CURRENT ADDRESS BYTE READ

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to "0") followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C04U to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to "1." The XL24C04U will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The XL24C04U discontinues transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.

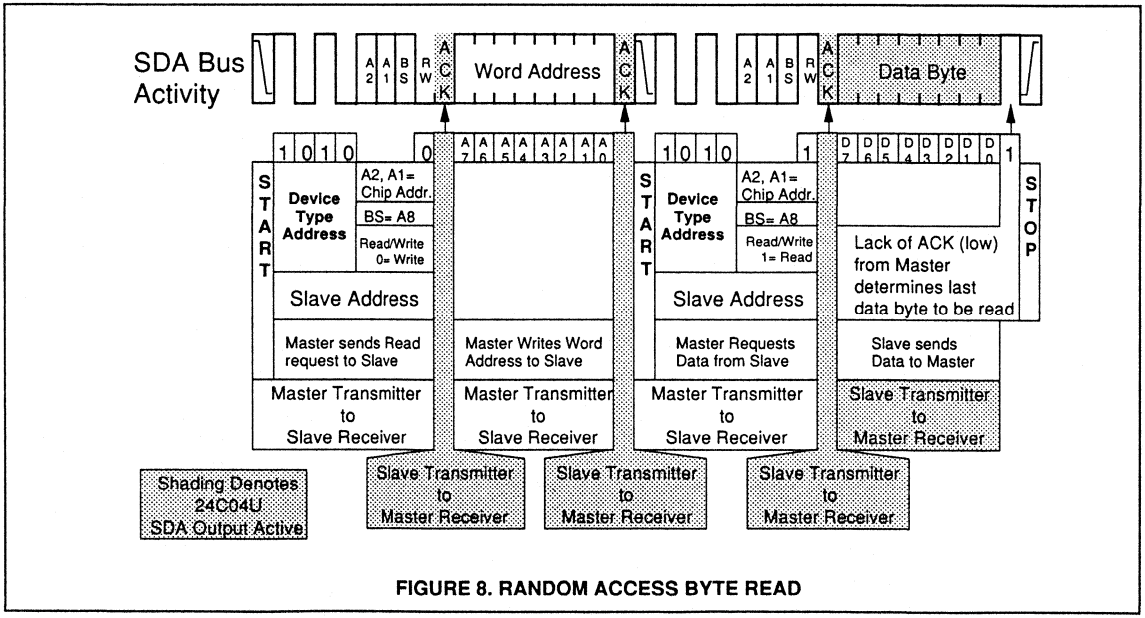


FIGURE 8. RANDOM ACCESS BYTE READ

Sequential Read

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During the sequential address read operation, the internal address counter of the XL24C04U automatically increments with each acknowledge received, ensuring that the data from address n will be followed by the data from address n+1. For read operations, all bits of the address counter are incremented, allowing the entire array to be read using a single read command. When the counter reaches the top of the array, it will "roll over" to the bottom of the array and continue to transmit data for each acknowledge it receives. See Figure 9 for the address, acknowledge and data transfer sequence.

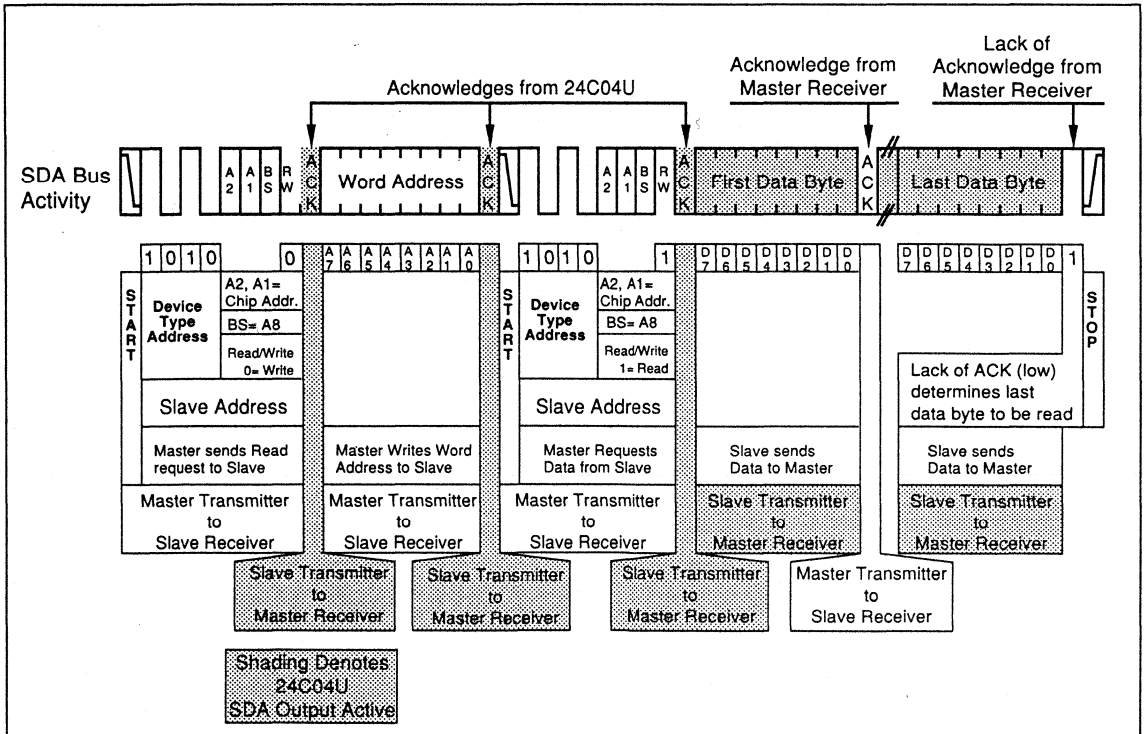

FIGURE 9. SEQUENTIAL READ (starting with a Random Address)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.5V to V_{CC}+0.5V
Output Current 5mA
Electrostatic Discharge Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

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T_A = 0°C to +70°C for the XLS24C04U or -40°C to +85°C for the XLE24C04U, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC1}	Supply Current (CMOS)	SCL=CMOS Levels @ 100KHz SDA=Open, all other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL=SDA=Vcc All other inputs=GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to 5V			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to 5V			10	µA
V_{IL}	Input Low Voltage	A1-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A1-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA (SDA only)			0.4	V
V_{WI}	Write Inhibit Voltage		2.5	3.4	4.5	V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04U or -40°C to +85°C for the XLE24C04U, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1.0	µs
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time constant @ SCL, SDA inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

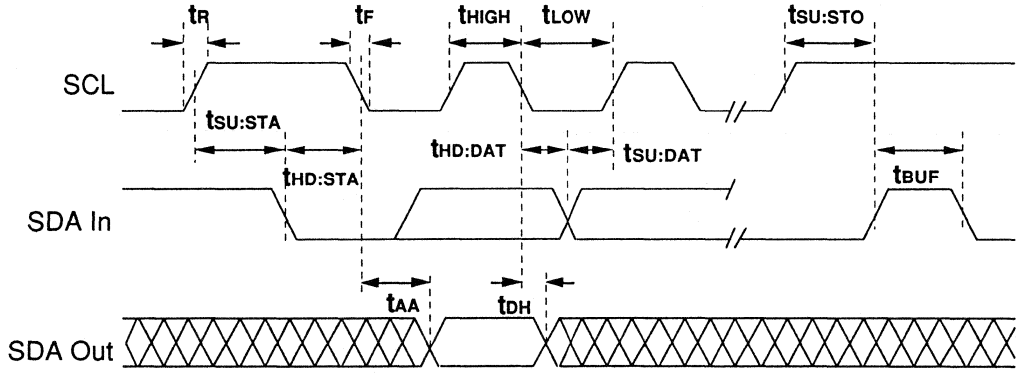


FIGURE 10. BUS TIMING

Preliminary

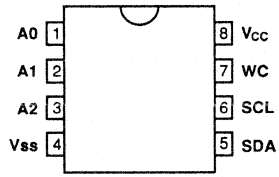
4,096-Bit Serial Electrically Erasable PROM
3 to 5 Volt Operation

FEATURES

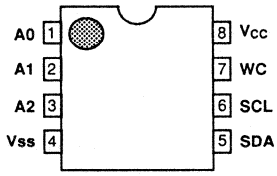
- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2µA**
- **Hardware Write Protection**
  - **— Write Control pin**
- **2.7 to 5.5V Operation**
- **Internally Organized as Two Banks**
  - **— Each 256 x 8**
- **Two Wire Serial Interface (I^2C™)**
  - **—Bidirectional data transfer protocol**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms @ 5V**
- **High Reliability**
  - **— Endurance: 100,000 write cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



EIAJ Small Outline "JR" Package



PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

OVERVIEW

The XL24C04-3 is a low-cost, 4,096-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The part operates from a single supply over the range of 2.7 to 5.5 volts.

The XL24C04-3 is internally organized as two 256 x 8 memory banks. The XL24C04-3 features the I^2C™serial interface and software protocol allowing operation on a simple two-wire bus. Up to four XL24C04-3s may be individually addressed on the two-wire bus by establishing their device address using the address input pins (A1 and A2).

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

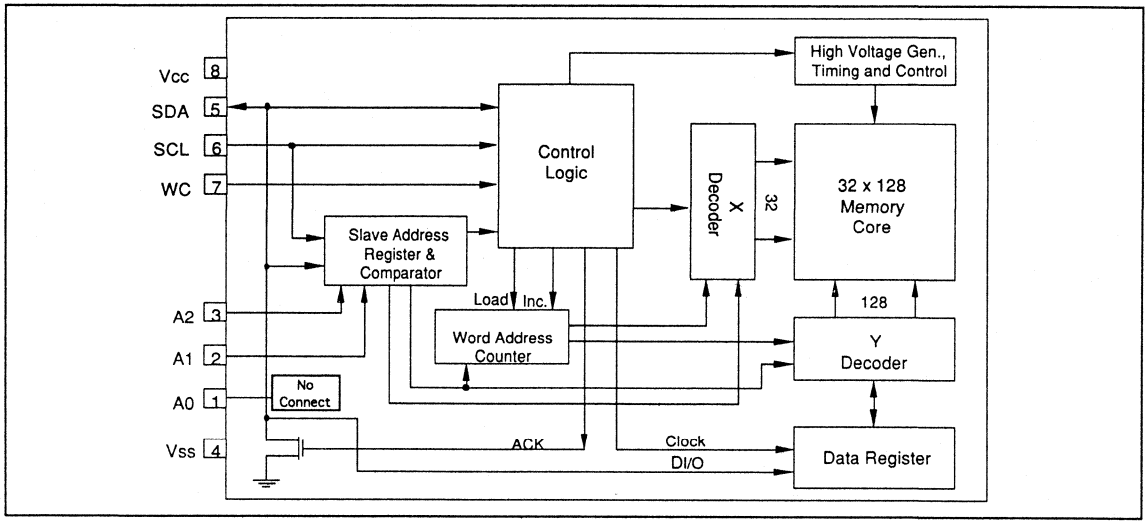
Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address (A0) - The A0 pin is not electrically connected to the XL24C04-3 device.

Address (A1, A2) - The address input pins are used to set the two-bit device address of the XL24C04-3 which will identify it on the two-wire bus. These inputs may be tied HIGH, LOW, or they may be actively driven. These inputs allow up to four XL24C04-3 devices to be distinguished on the bus.

Write Control (WC) - The Write Control input pin is used to disable the write circuitry to the memory. When HIGH, the write function is disabled, protecting data; when LOW, the write function is enabled.

BLOCK DIAGRAM



ENDURANCE AND DATA RETENTION

The XL24C04-3 is designed for applications requiring up to 100,000 write cycles per bit and unlimited read cycles. It provides 10 years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C04-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving, 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. (See Figure 1.) Data transfer between devices may be initiated only when SCL and SDA are HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line when SCL is HIGH will be interpreted as control signals. (See Figure 2.)

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. (See Figure 3.)

DEVICE OPERATION

The XL24C04-3 is a 4,096-bit serial E²PROM. The device supports the I²C™ bidirectional data transmission protocol. The protocol defines any device sending data onto the bus as a "transmitter," and any device which is receiving data as a "receiver." The device controlling the data transmission is defined as the "master," and the controlled device is called the "slave." In all cases, the XL24C04-3 will be a "slave" device, since it never initiates any data transfers.

Up to four XL24C04-3s can be connected to the bus, selected by the A1 and A2 device addresses. A0 is not electrically connected. A1 and A2 must be connected to either V_{CC} or V_{SS}. A1 and A2 define the device address. Other devices may be connected to the bus, but need a different device identification code.

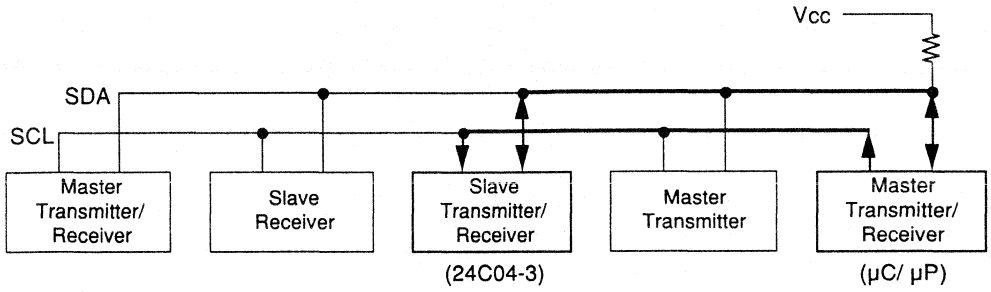


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

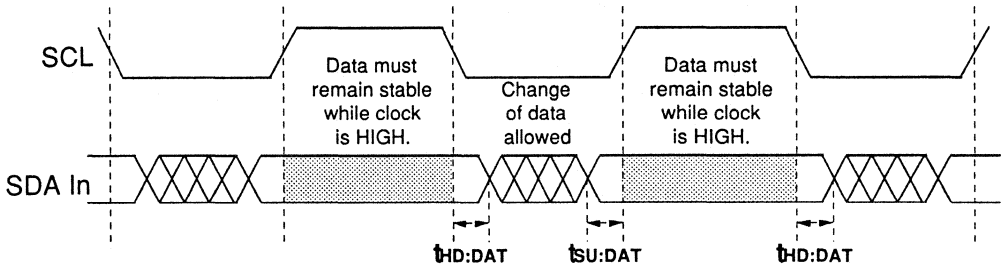


FIGURE 2. INPUT DATA PROTOCOL

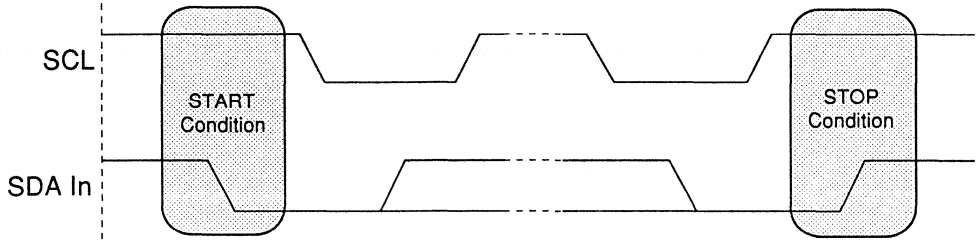


FIGURE 3. START AND STOP CONDITIONS

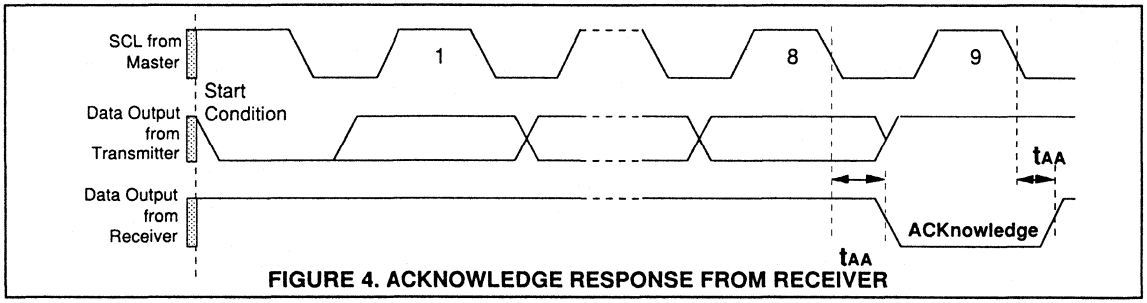


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C04-3 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation have been selected, the XL24C04-3 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C04-3 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C04-3 will continue to transmit data. If an ACKnowledge is not detected, the XL24C04-3 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the device address of the slave to be accessed. The most significant four bits of the slave address are the "device type identifier." For the XL24C04-3 this is fixed as 1010. (See Figure 5.)

The next two bits (device address), address a particular device. Using this addressing scheme, a system may have up to four XL24C04-3 devices on the bus. The device address is defined by the state of the A1 and A2 input pins.

Bank Select Bit

The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Op Code

The last bit of the stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The XL24C04-3 allows two types of write operations: byte write and page write. The first writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows for a full 16-byte page to be stored during t_{WR}.

Byte Write

After the slave address is sent (to identify the slave device, select the bank and specify a read or write instruction), a second field is sent from the master to the slave. This field contains the word address and is comprised of eight bits providing access to any one of the 256 words in the bank.

Upon receipt of the word address, the XL24C04-3 responds with an ACKnowledge, and waits for the eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C04-3 begins the internal write cycle to the nonvolatile array.

While the internal write cycle is in progress, the XL24C04-3 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Device Type Identifier				Device Address		Bank Select	Read/ Write
Slave Address							
1	0	1	0	A2	A1	BS (A8)	Read = 1 Write = 0

FIGURE 5. SLAVE ADDRESS BYTE

Page Write

The XL24C04-3 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words of data. After the receipt of each word, the XL24C04-3 will respond with an ACKnowledge.

The XL24C04-3 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

READ OPERATIONS

Read operations are initiated in the same manner as write operations except that the R/W bit of the identification field is set to "1." There are four different read operation options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The XL24C04-3 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address n, the next read operation would access data from address n+1 and update the current address pointer. When the XL24C04-3 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address read operation only accesses a single byte of data, the master does not acknowledge the transfer but does generate a stop condition. At this point, the XL24C04-3 discontinues transmission. See Figure 7 for the address acknowledge and data transfer sequence.

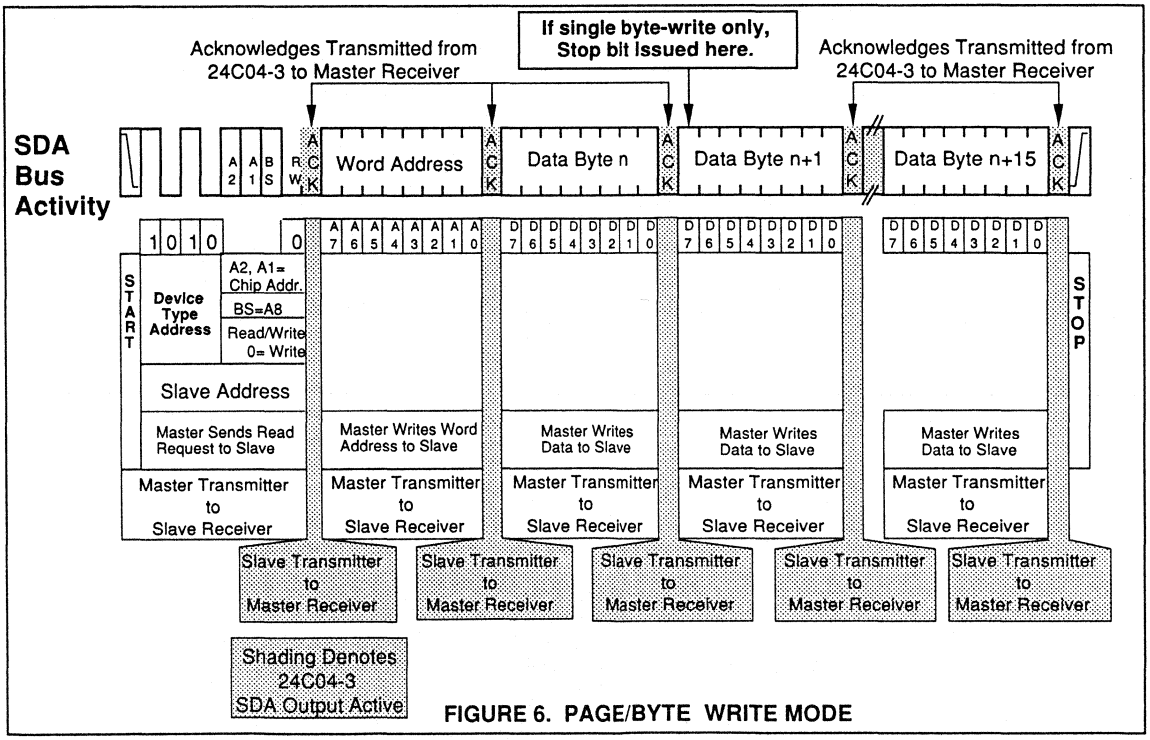


FIGURE 6. PAGE/BYTE WRITE MODE

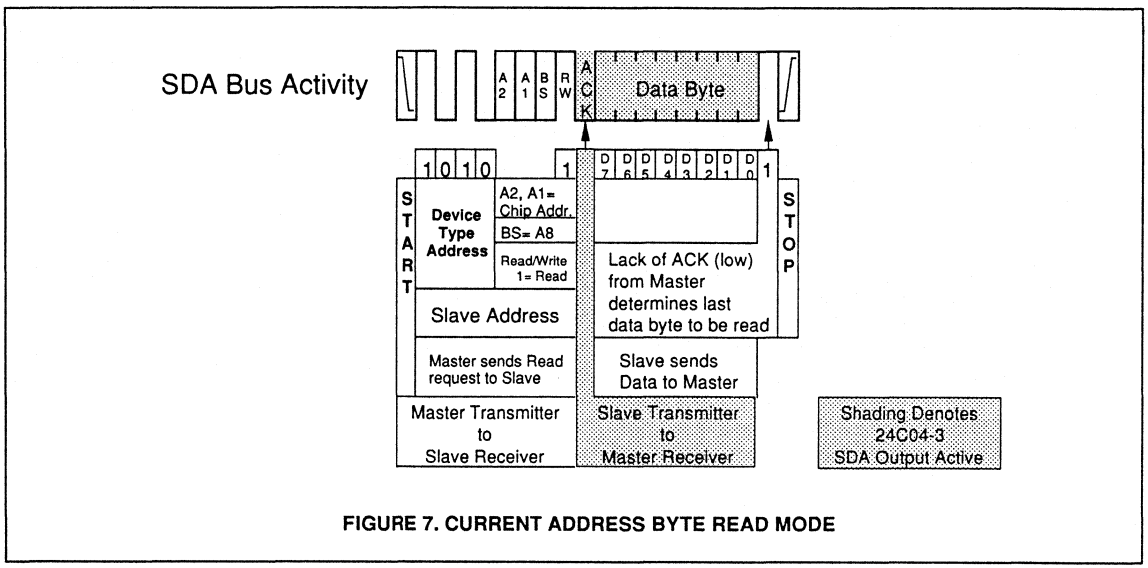


FIGURE 7. CURRENT ADDRESS BYTE READ MODE

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to "0") followed by the address of the word it is to read. This procedure sets the internal address counter of the XL24C04-3 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to "1." The XL24C04-3 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The XL24C04-3 discontinues transmission and reverts to its standby power mode. See Figure 8 for the address, acknowledge and data transfer sequence.

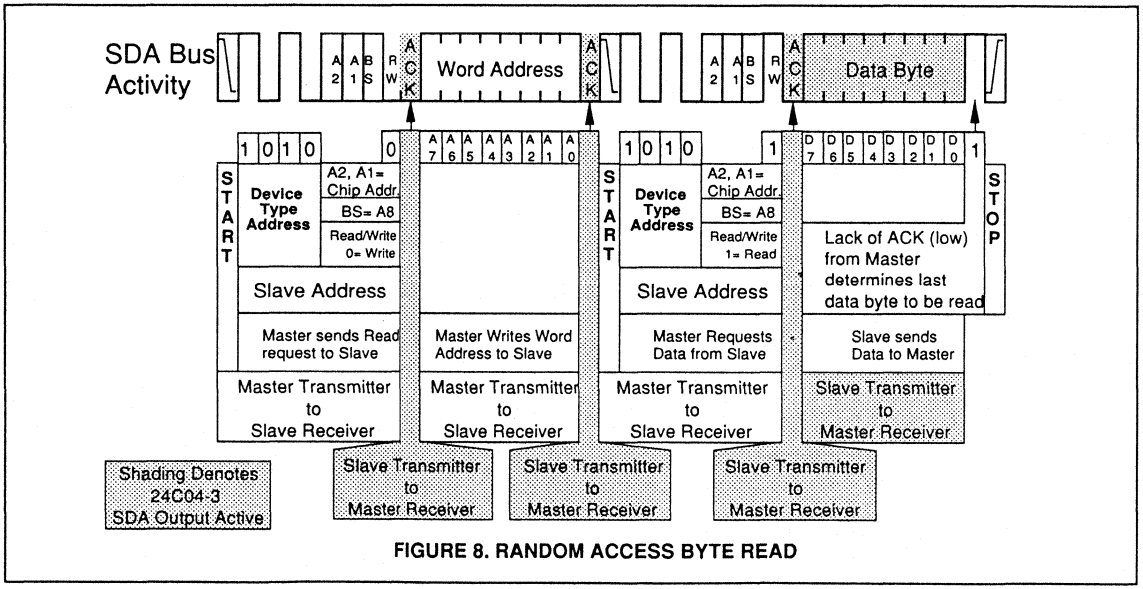


FIGURE 8. RANDOM ACCESS BYTE READ

Sequential Read

The sequential address read operation can be initiated as either a current address read or a random address read. The first data accessed is transmitted by the XL24C04-3 just as with other byte read modes; however, instead of responding with a stop condition, the master now responds with an acknowledge indicating it requires additional data from the XL24C04-3. The XL24C04-3 transmits a new byte of data for each acknowledge received. The sequential address read operation is terminated by the master withholding the acknowledge and generating a stop condition.

During the sequential address read operation, the internal address counter of the XL24C04-3 automatically increments with each acknowledge received, ensuring that the data from address n will be followed by the data from address n+1. For read operations, all bits of the address counter are incremented, allowing the entire array to be read using a single read command. When the counter reaches the top of the array, it will "roll over" to the bottom of the array and continue to transmit data for each acknowledge it receives. See Figure 9 for the address, acknowledge and data transfer sequence.

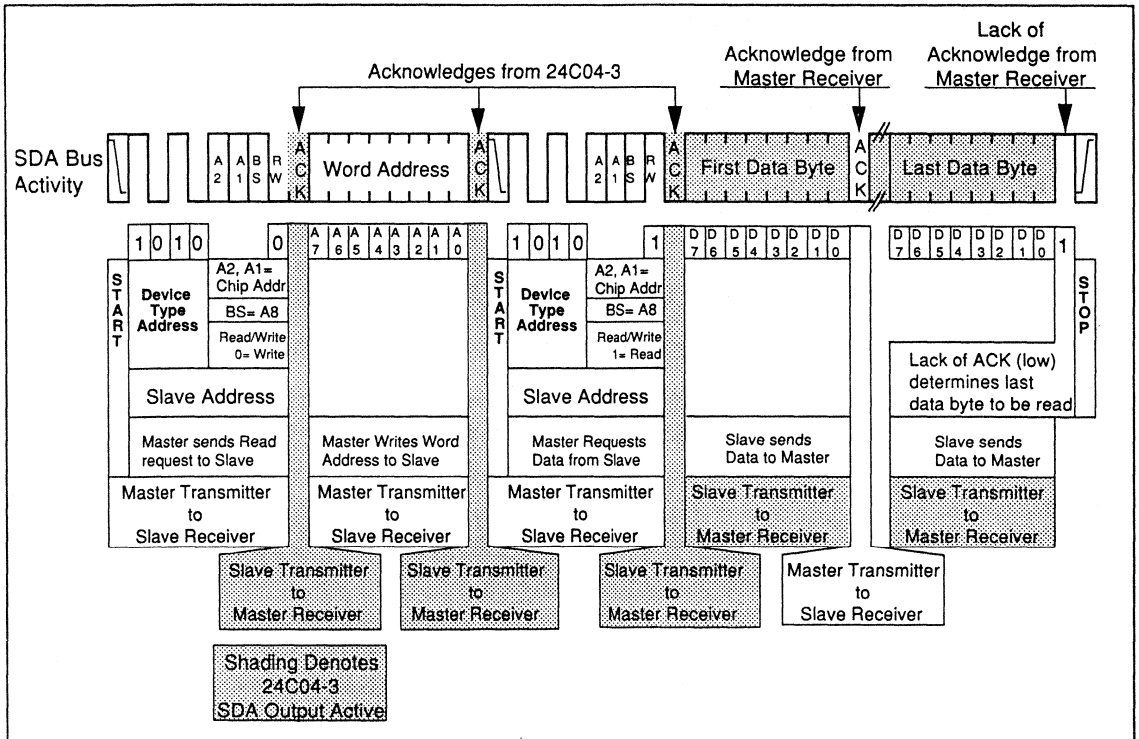


FIGURE 9. SEQUENTIAL READ (starting with a Random Address)

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds) .....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
Output Current 5mA
Electrostatic Discharge Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04-3 or -40°C to +85°C for the XLE24C04-3, V_{CC} = 3V ±10% or 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC1}	Supply Current (CMOS)	SCL=CMOS Levels @ 100KHz SDA=Open, all other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL=SDA=Vcc All other inputs=GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc			10	µA
V_{IL}	Input Low Voltage	A1-A2, SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	A1-A2, SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA (SDA only)			0.4	V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C04-3 or -40°C to +85°C for the XLE24C04-3, V_{CC} = 3V ±10% or 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid Vcc = 5V Vcc = 3V	0.3 0.3	3.5 4.7	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1.0	µs
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time constant @ SCL, SDA inputs		100	ns
t_{WR}	Write Cycle Time	XLS24C04-3 Vcc = 5V Vcc = 3V		10 20	ms
		XLE24C04-3 Vcc = 5V Vcc = 3V		10 25	

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

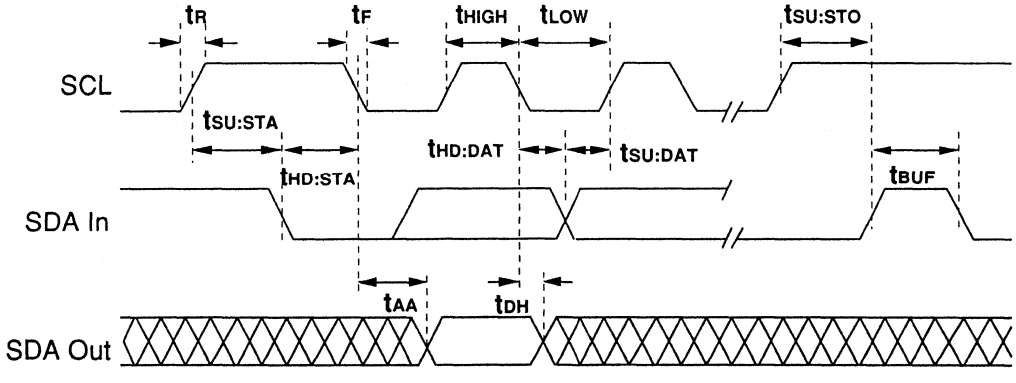


FIGURE 10. BUS TIMING

Advance Information

16,384-Bit Serial Electrically Erasable PROM
3 Volt and 5 Volt Operation

FEATURES

- **Low Power CMOS**
  - **— Active current less than 1mA**
  - **— Standby current less than 2μA**
- **Two Voltage Ranges**
  - **— 2.7 to 5.5V**
  - **— 4.5 to 5.5V**
- **Hardware Write Protection**
  - **— Write Control pin**
  - **— Low Vcc lockout write protection (5V only)**
- **Internally Organized as 2,048 x 8**
- **Two Wire Serial Interface (I²C™)**
  - **— Bidirectional data transfer protocol**
- **Sixteen-Byte Page-Write Mode**
  - **— Minimizes total write time per byte**
- **Automatic Word Address Incrementing**
  - **— Sequential register read**
- **Self-Timed Write Cycle**
  - **— Maximum write cycle time of 10ms**
- **High Reliability**
  - **— Endurance: 100,000 cycles per byte**
  - **— Data retention: 10 years**
- **8-Pin PDIP or SOIC Packages**

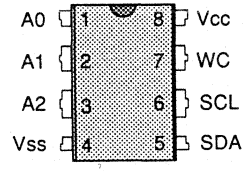
OVERVIEW

The XL24C16 is a low-cost 16,384-bit serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology and operates from a single 3 volt or 5 volt supply.

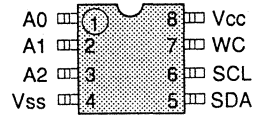
The XL24C16 is internally organized as eight 2K x 8 memory banks. The XL24C16 features a serial interface and software protocol allowing operation on a simple two-wire bus (I²C™). Only one XL24C16 may be connected to the 2-wire bus, due to I²C™ protocol.

PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"JR" Package

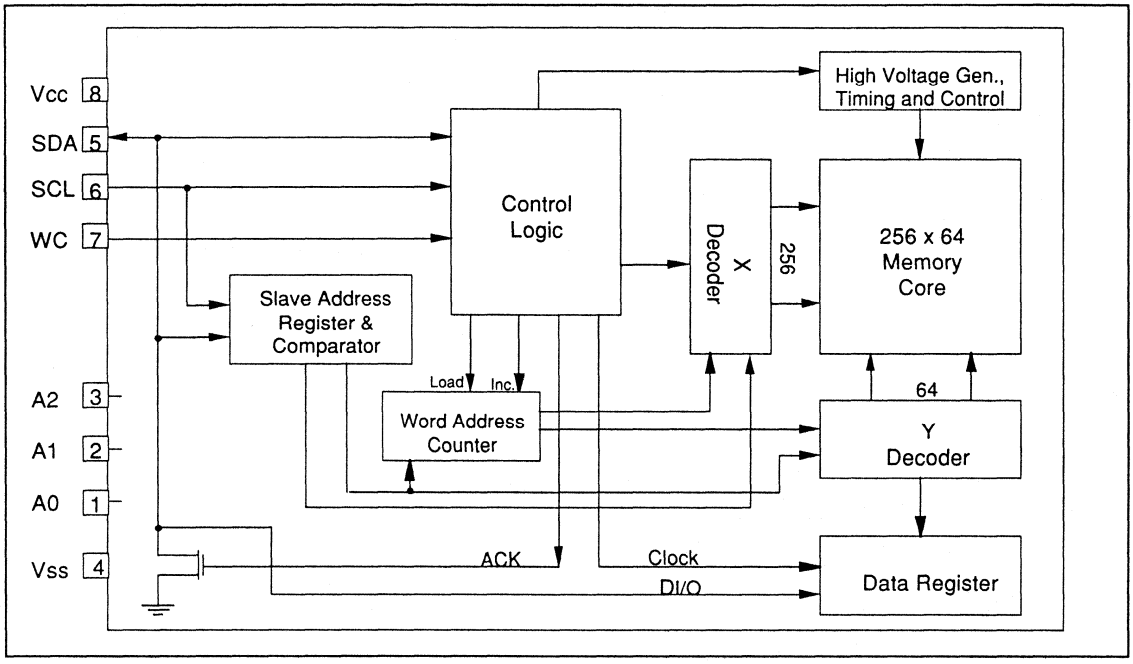


PIN NAMES

A0-A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
WC	Write Control Input
V_{SS}	Ground
V_{CC}	Supply Voltage

Advance Information

BLOCK DIAGRAM



PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock all data into and out of the device. In the WRITE mode, data must remain stable when SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW. It is an open-drain output, and may be wire-ORed with any number of open-drain or open-collector outputs.

A0, A1 and A2 - The address inputs are unused on the XL24C16 and are not connected. They may be tied HIGH, LOW or left open.

Write Control (WC) - The Write Control input is used to disable any attempt to write to the memory. When HIGH, the memory is protected; when LOW, the write function is normal.

ENDURANCE AND DATA RETENTION

The XL24C16 is designed for applications requiring up to 100,000 write cycles and unlimited read cycles. It provides ten years of secure data retention, with or without power applied, after the execution of 100,000 write cycles.

APPLICATIONS

The XL24C16 is ideal for high volume applications requiring low power and low density storage. This device uses a low-cost, space-saving 8-pin plastic package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation.

Vcc Lockout — Inadvertent WRITE Protection (5V parts only)

To insure against inadvertent WRITE operations, the XL24C16 has been equipped with an internal Vcc sensor circuit, which inhibits data alteration when the supply voltage falls below V_{WI}. If the applied Vcc is below 3.0V (typical), the XL24C16 is inhibited from executing WRITE operations, thereby protecting the nonvolatile data from being altered inadvertently.

CHARACTERISTICS OF THE I²C™ BUS

General Description

The I²C™ bus was designed for 2-way, 2-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus. Refer to Figure 1 below, "Typical System Configuration." Data transfer may be initiated only when the bus is "not busy," which is defined as both SCL and SDA inputs being HIGH.

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes on the data line at this time will be interpreted as control signals. Refer to Figure 2 below.

START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the "STOP" condition. Refer to Figure 3 below.

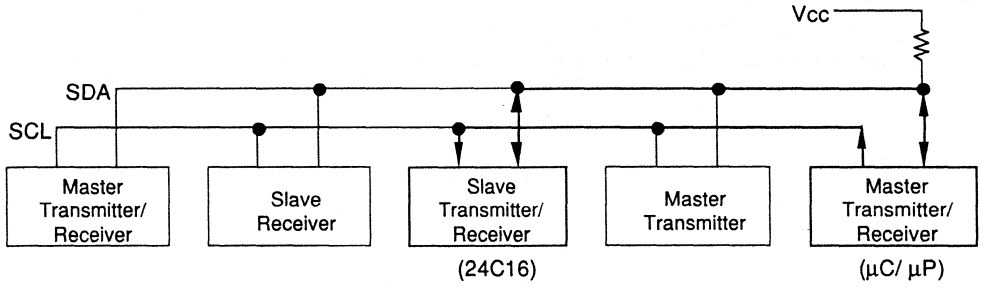


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

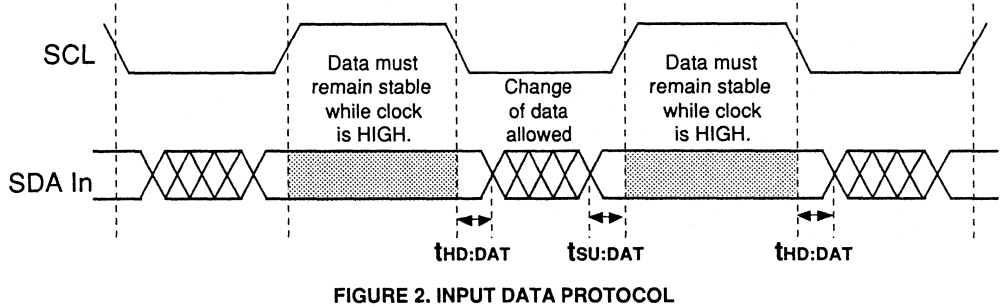


FIGURE 2. INPUT DATA PROTOCOL

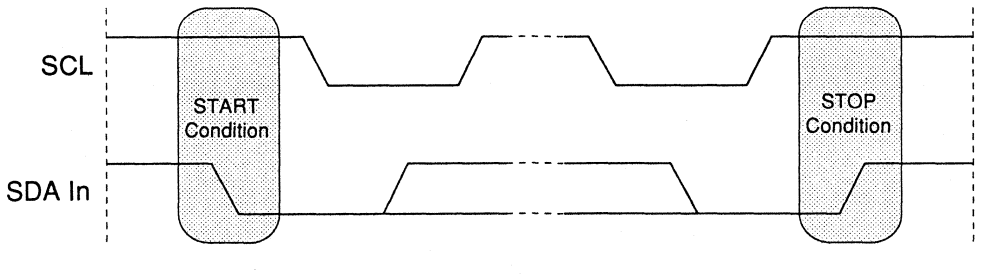


FIGURE 3. START AND STOP CONDITIONS

Advance Information

DEVICE OPERATION

The XL24C16 is a 16,384-bit serial E²PROM. The device supports a bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter," and the receiving device as the "receiver." The device controlling the data transmission is the "master," and the controlled device is the "slave." In all cases, the XL24C16 will be a "slave" device, since it never initiates any data transfers.

A single XL24C16 may be connected to the bus. This is due to the fact that the I²C™ protocol is limited to 16K addresses. The A0, A1 and A2 inputs are not connected.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data. (See Figure 4.)

The XL24C16 will respond with an ACKnowledge after recognition of a START condition and its slave address. If both the device and a WRITE operation have been selected, the XL24C16 will respond with an ACKnowledge, after the receipt of each subsequent 8-bit word.

In the READ mode, the XL24C16 will transmit eight bits of data, release the SDA line, and monitor the line for an ACKnowledge. If an ACKnowledge is detected, and no STOP condition is generated by the master, the XL24C16 will continue to transmit data. If an ACKnowledge is not detected, the XL24C16 will terminate further data transmissions. The master must then issue a STOP condition to return the XL24C16 to the standby power mode.

Slave Address Byte

Following a START condition, the master must output the address of the slave that it is accessing. The most significant four bits of the slave address are the "device type identifier." For an I²C™ memory device, this is fixed as 1010. Refer to Figure 5 below.

The next three significant address bits address a particular bank in the device. They are, in effect, A10, A9 and A8 of the memory device.

The last bit of the slave address defines the operation to be performed. When set to "1," a READ operation is selected; when set to "0," a WRITE operation is selected.

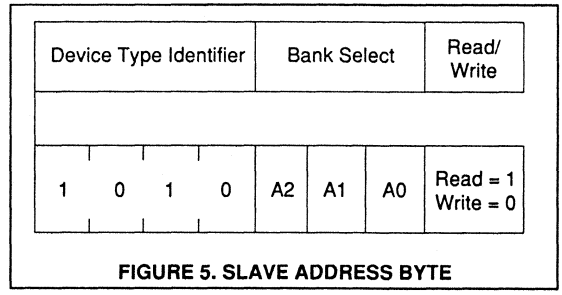


FIGURE 5. SLAVE ADDRESS BYTE

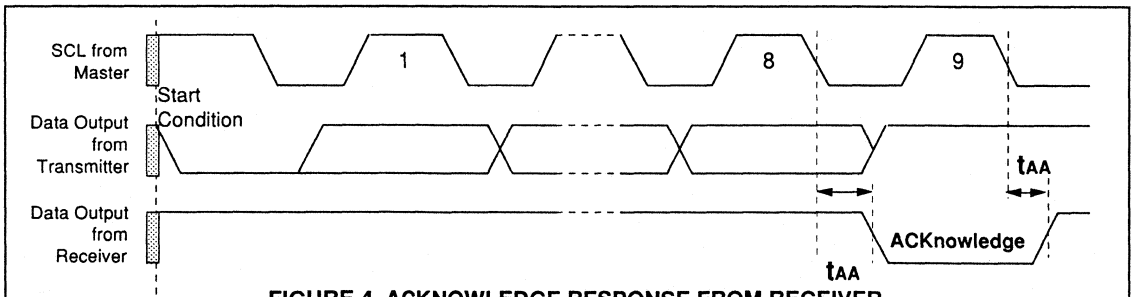


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

WRITE OPERATIONS

Byte WRITE

For a WRITE operation, the XL24C16 requires a second address field. This address field is the word address, comprised of eight bits, which provides access to any one of the 2K words of memory which reside in each bank.

Upon receipt of the word address, the XL24C16 responds with an ACKnowledge, and waits for the next eight bits of data, again responding with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the XL24C16 begins the internal WRITE cycle to the nonvolatile array.

While the internal WRITE cycle is in progress, the XL24C16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

Page WRITE

The XL24C16 is capable of a 16-byte page-WRITE operation. It is initiated in the same manner as the byte-WRITE operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to 15 more words. After the receipt of each word, the XL24C16 will respond with an ACKnowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order four bits of the address remain constant. If the master should transmit more than 16 words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-WRITE operation, all inputs are disabled until completion of the internal WRITE cycle. Refer to Figure 6 below for the address, ACKnowledge, and data transfer sequence.

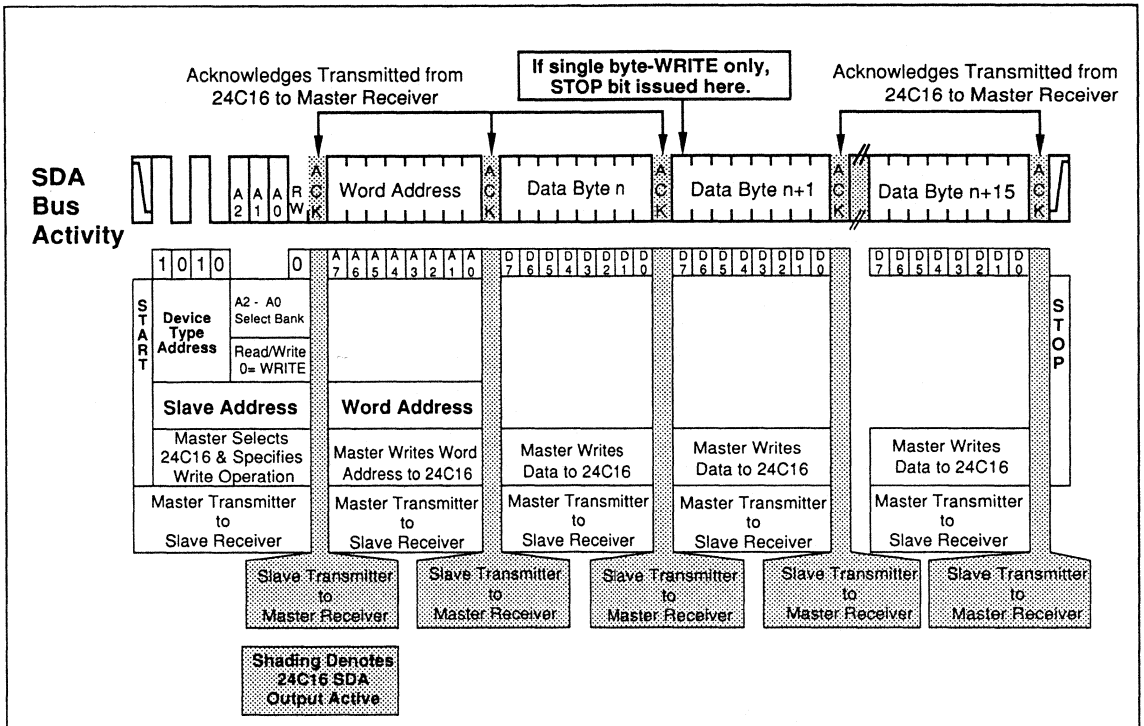


FIGURE 6. PAGE WRITE MODE

Acknowledge Polling

When the XL24C16 is performing an internal WRITE operation, it will not recognize a START condition. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation. Refer to Figure 7 below.

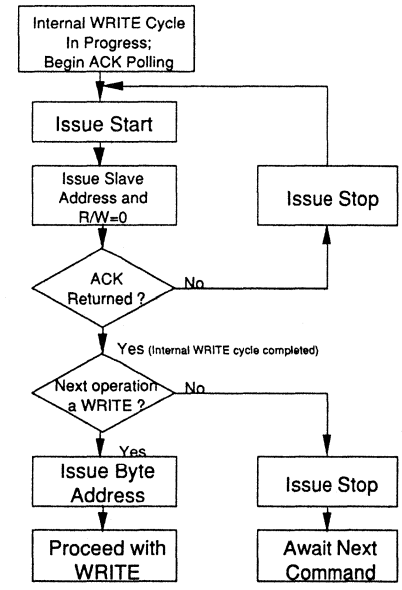


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

READ operations are initiated in the same manner as WRITE operations, except that the R/W bit of the slave address byte is set to "1." There are four different READ operation options:

1. Current Address Byte READ
2. Random Address Byte READ
3. Current Address Sequential READ
4. Random Address Sequential READ

Current Address Byte READ

The XL24C16 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a READ or a WRITE) was to address n, the next READ operation would access data from address n+1, and update the current address pointer. When the XL24C16 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address n+1.

If the current address READ operation only accesses a single byte of data, the master does not acknowledge the transfer, but does generate a STOP condition. At this point, the XL24C16 discontinues transmission. See Figure 8 below for the address, acknowledge, and data transfer sequence.

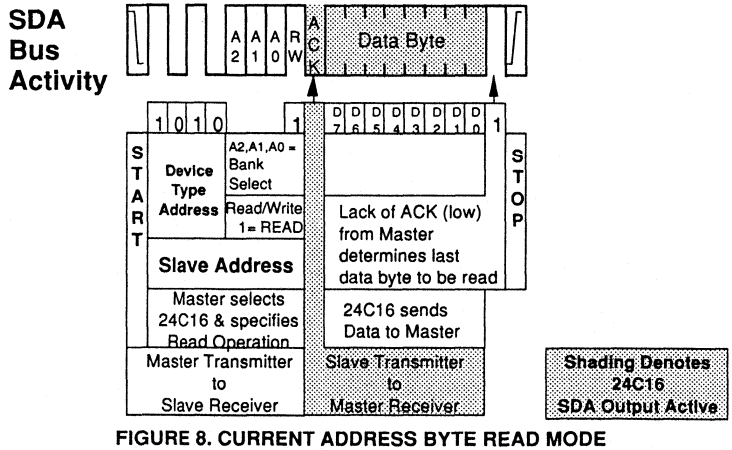


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

READ OPERATIONS (continued)

Random Address Byte READ

Random address READ operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a WRITE command which includes the START condition and the slave address field (with the R/W bit set to "0"), followed by the address of the word it is to READ. This procedure sets the internal address counter of the XL24C16 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a START condition followed by another slave address field with the R/W bit set to "1." The XL24C16 will respond with an acknowledge and transmit the eight data bits stored at the addressed location. At this point, the master does not acknowledge the transmission, but does generate the STOP condition. The XL24C16 discontinues transmission and reverts to its standby power mode. See Figure 9 below for the address, acknowledge, and data transfer sequence.

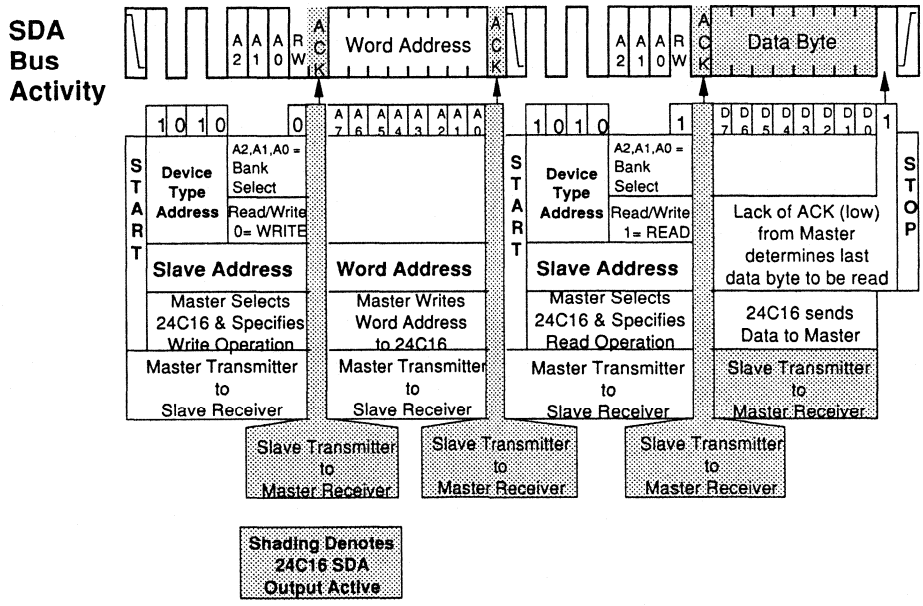


FIGURE 9. RANDOM ACCESS BYTE READ MODE

READ OPERATIONS (continued)

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes; however, the master now responds with an ACKnowledge, indicating that it requires additional data from the XL24C16. The XL24C16 continues to output data for each ACKnowledge received. The sequential READ operation is terminated by the master, by not responding with an ACKnowledge, and by issuing a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n+1. The address counter for READ operations increments automatically, as well as the bank address, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2,047), the counter "rolls over" to address 0, and the XL24C16 continues to output data for each ACKnowledge received.

Refer to Figure 10 below for the address, ACKnowledge, and data transfer sequence. Figure 10 shows a sequential READ starting with a random address. A sequential READ may also begin with a current address READ.

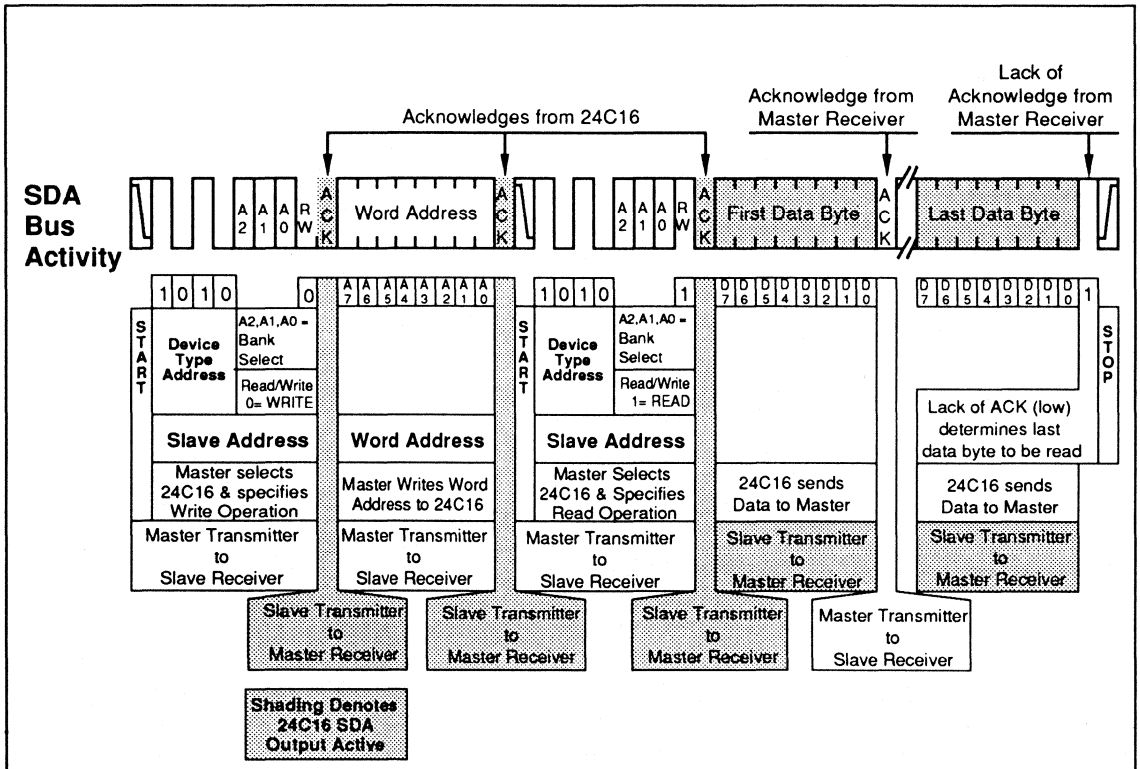


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: .....-40°C to +85°C
Storage Temperature .....-65°C to +125°C
Soldering Temperature (less than 10 seconds).....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin .....-0.5V to V_{CC}+0.5V
ESD Voltage (JEDEC method) 2,000V
Output Current .....+5mA

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C16 or -40°C to +85°C for the XLE24C16, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs=GND or Vcc			1	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = Vcc All other inputs = GND or Vcc			2	µA
I_{LI}	Input Leakage	V_{IN} = 0 to Vcc			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 to Vcc			10	µA
V_{IL}	Input Low Voltage	SCL, SDA			0.3 x V_{CC}	V
V_{IH}	Input High Voltage	SCL, SDA	0.7 x V_{CC}			V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V
V_{WI}	Write Inhibit Voltage	(5 volt part only)	2.5	3.4	4.5	V

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

Advance Information

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS24C16 or -40°C to +85°C for the XLE24C16, V_{CC} = 3V±10% or 5V±10%

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100	KHz
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		µs
t_R	SCL and SDA Rise Time			1000	ns
t_F	SCL and SDA Fall Time			300	ns
$t_{SU:DAT}$	Data In Setup Time		250		ns
$t_{HD:DAT}$	Data In Hold Time		0		ns
T_I	Noise Spike Width	Time Constant @ SCL, SDA Inputs		100	ns
t_{WR}	Write Cycle Time			10	ms

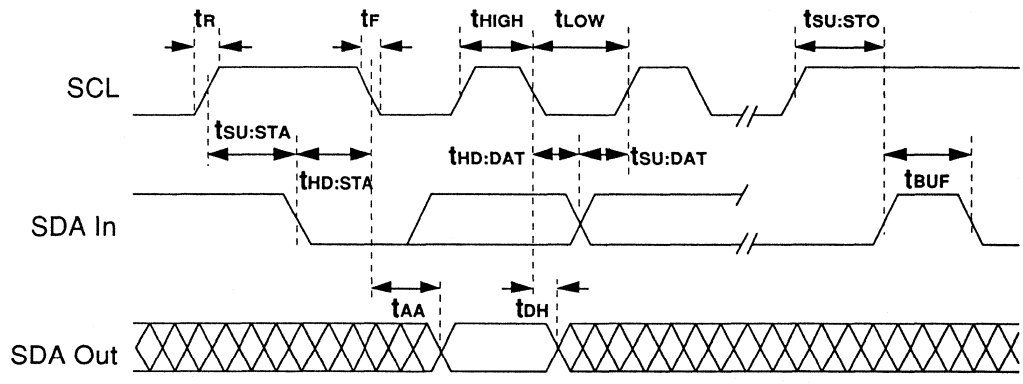


FIGURE 11. BUS TIMING

XL93LC06

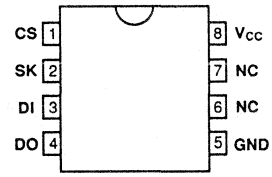
256-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

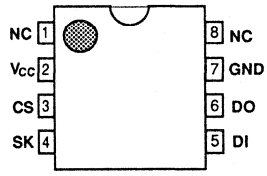
- **State-of-the-Art Architecture**
  - — Nonvolatile data storage
  - — Single supply - 5V operation
  - — Fully TTL compatible inputs and outputs
  - — Auto increment for efficient data dump
  - — 1MHz operation
- **Hardware and Software Write Protection**
  - — Defaults to write-disabled state at power up
  - — Software instructions for write-enable/disable
  - — V_{CC} lockout inadvertent write protection
- **Low Power Consumption**
  - — 1mA active (typical)
  - — 1μA standby (typical)
- **Low Voltage Read Operations**
  - — Reliable read operations down to 2.0 volts
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - — Self-timed programming cycle
  - — Automatic erase-before-write
  - — Programming Status Indicator
  - — Word and chip erasable
- **Durable and Reliable**
  - — 10-year data retention after 100K write cycles
  - — Minimum of 100,000 write cycles per word
  - — Unlimited read cycles
  - — ESD protection

PIN CONFIGURATIONS

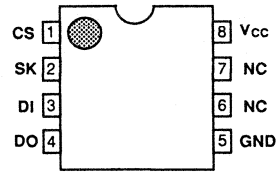
Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"J" Package



EIAJ Small Outline
"JR" Package



PIN NAMES

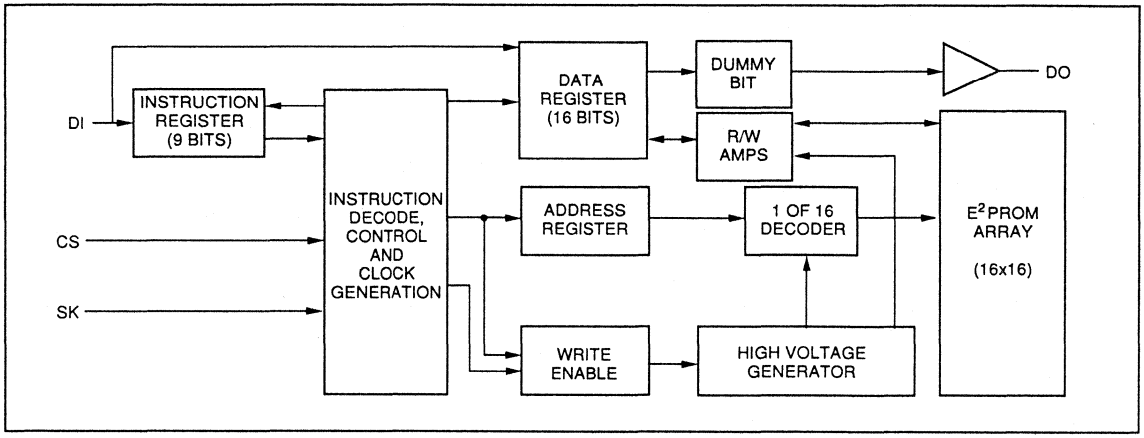
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC06 is a low cost 256-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC06 provides efficient nonvolatile read/write memory arranged as 16 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC06 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC06 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC06 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC06 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC06 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC06 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls as low as 2.0V, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC06 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC06 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC06 is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	XX(A_3-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	XX(A_3-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	XX(A_3-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias: XLS93LC06. ..... 0°C to +70°C
XLE93LC06 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

TA = 0°C to +70°C for the XLS93LC06 or -40°C to +85°C for the XLE93LC06

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current (CMOS)	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4	2.7	4.4	V

AC ELECTRICAL CHARACTERISTICS

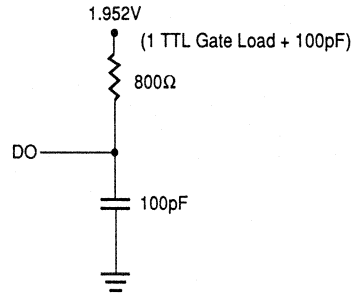
TA = 0°C to +70°C for the XLS93LC06 or -40°C to +85°C for the XLE93LC06

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⌙	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10			ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS

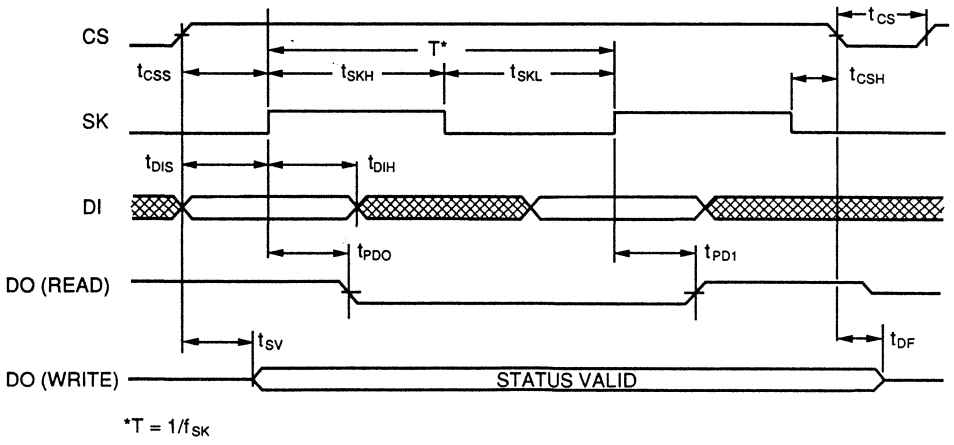
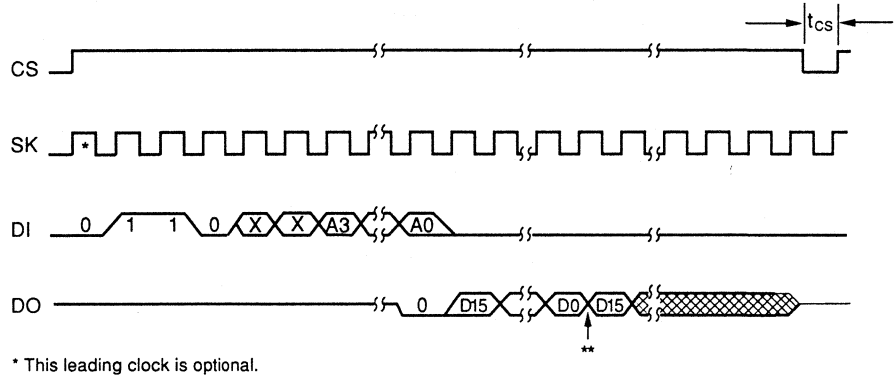


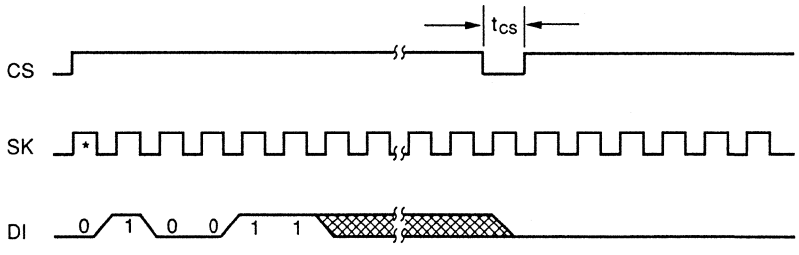
FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.

** Address pointer automatically cycles to the next register.

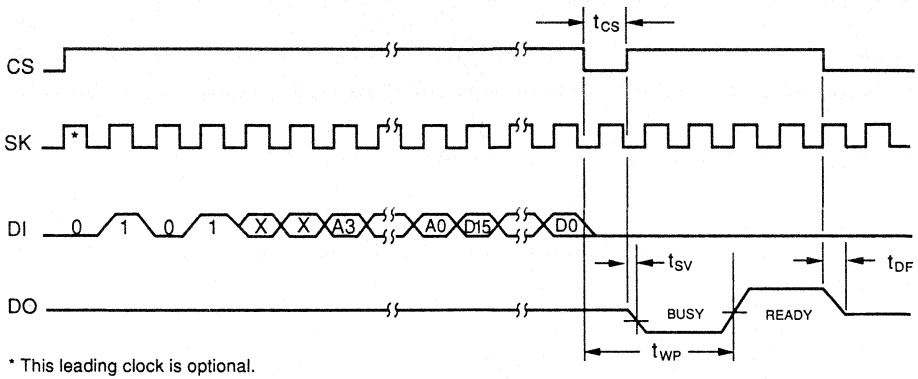
FIGURE 3. READ CYCLE TIMING



DO = 3-state

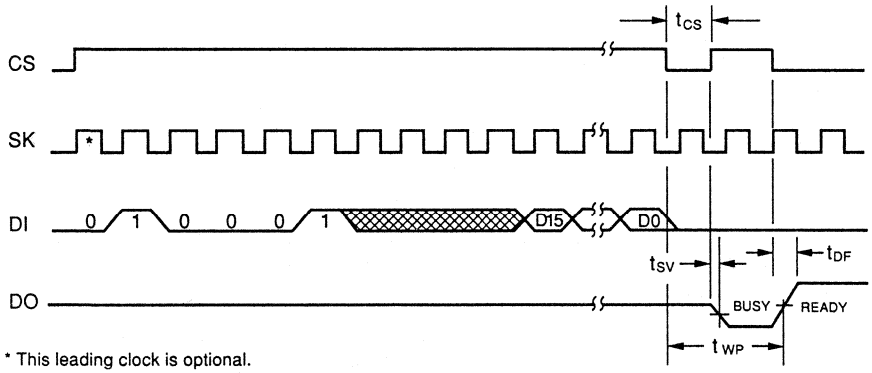
* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



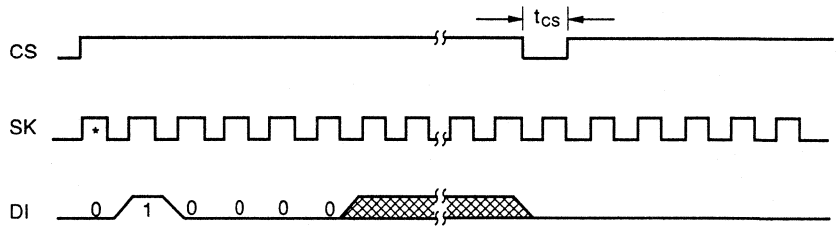
* This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



* This leading clock is optional.

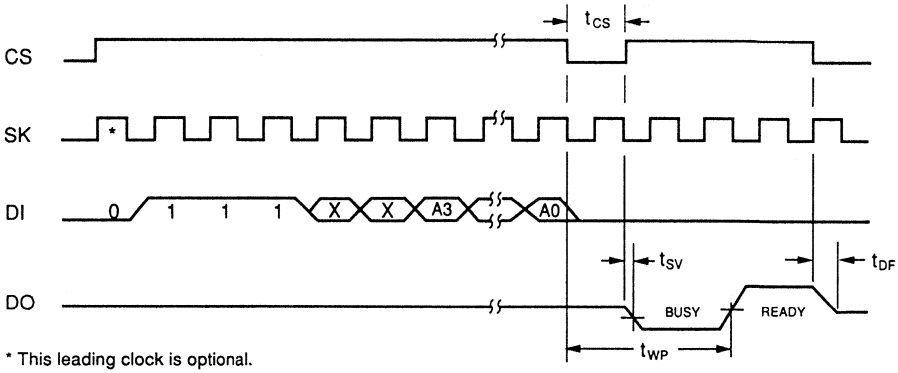
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

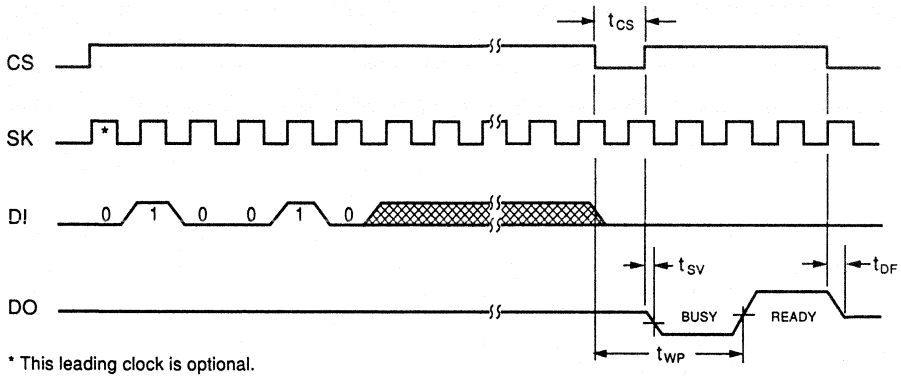
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

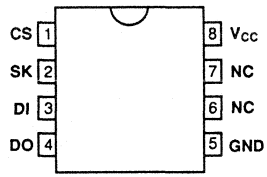
1,024-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

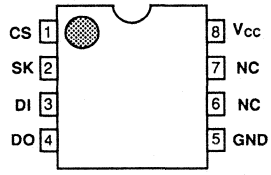
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

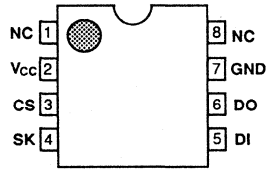
Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"JR" Package



EIAJ Small Outline
"J" Package



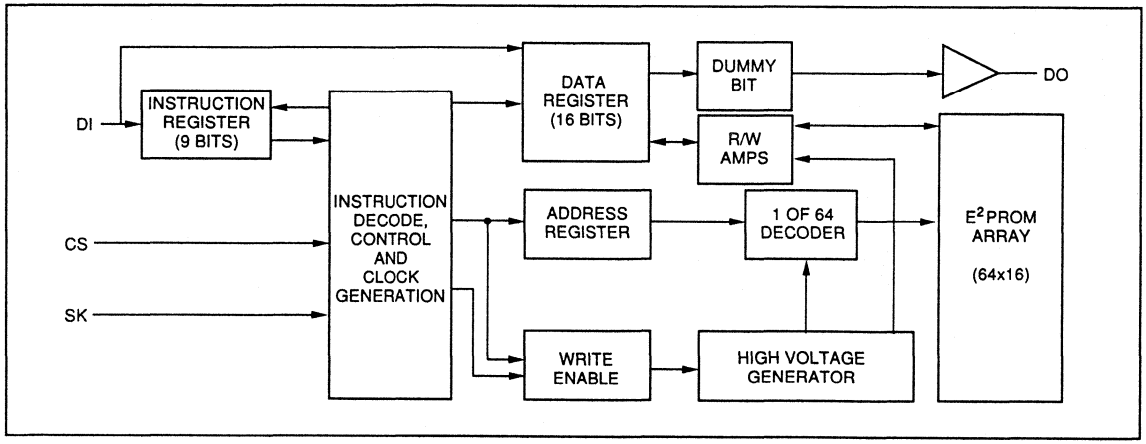
OVERVIEW

The XL93LC46 is a low cost 1,024-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC46 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

BLOCK DIAGRAM



The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

APPLICATIONS

The XL93LC46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC46 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC46 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC46 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC46 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5 volts, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state

until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{BUSY}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{BUSY}$ flag. Therefore, it is important if you want to access the READY/$\overline{BUSY}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC46 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC46 is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC46 ..... 0°C to +70°C
XLE93LC46 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46 or -40°C to +85°C for the XLE93LC46

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc - 0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4	n/a	n/a	V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46 or -40°C to +85°C for the XLE93LC46

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10	n/a	n/a	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

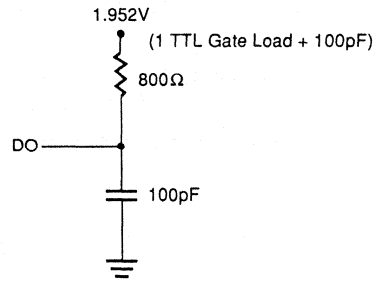
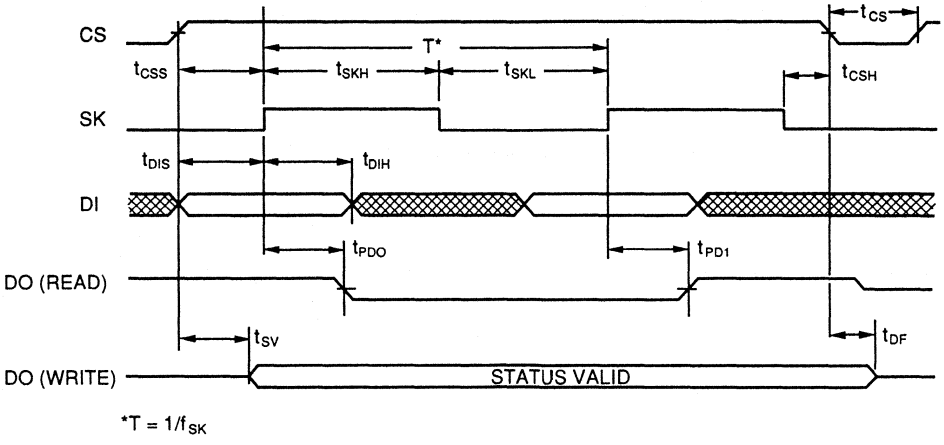
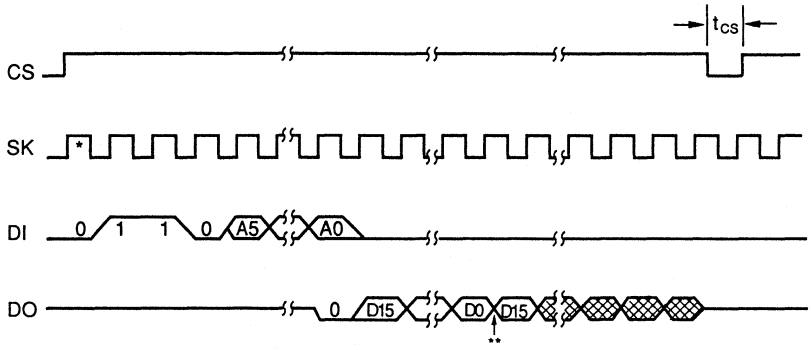


FIGURE 1. AC TEST CONDITIONS



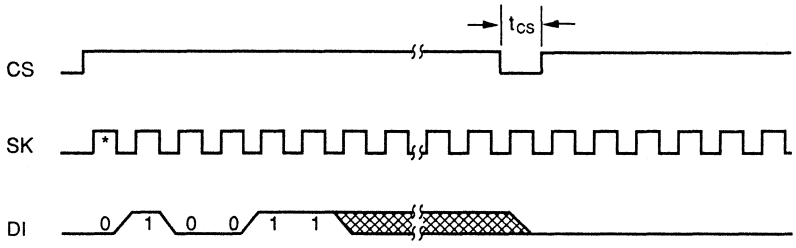
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

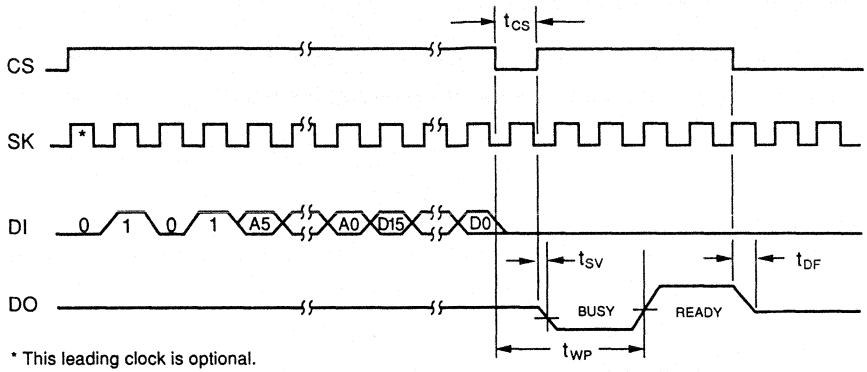


FIGURE 5. WRITE CYCLE TIMING

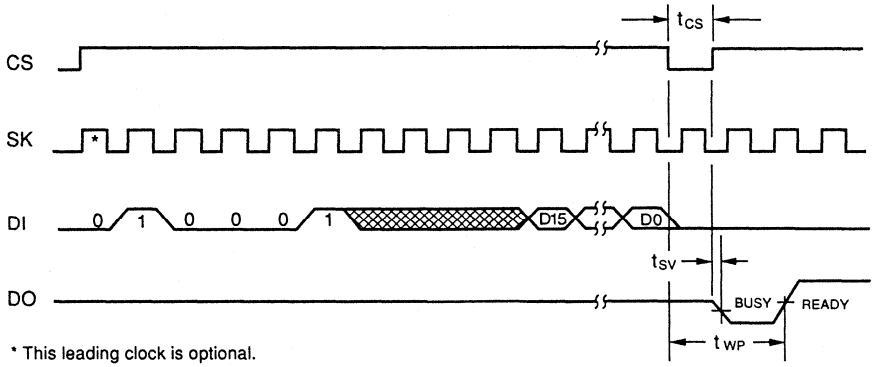
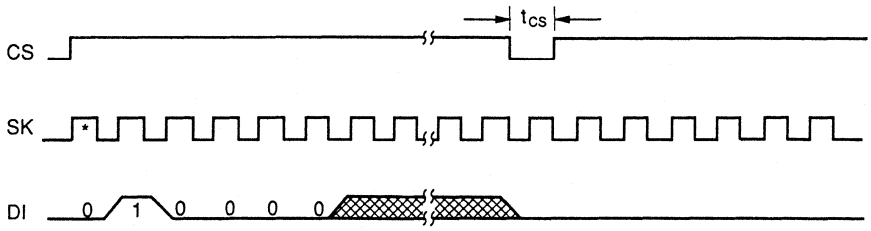


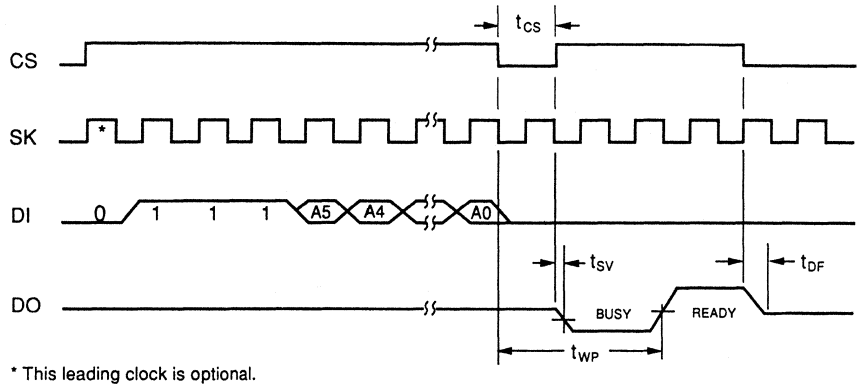
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

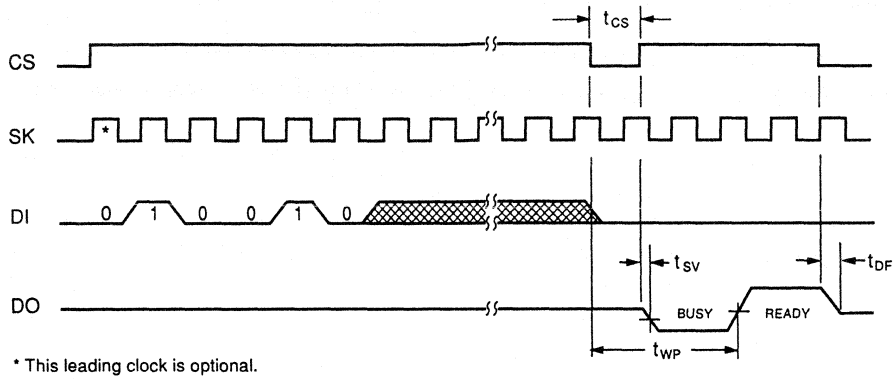
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

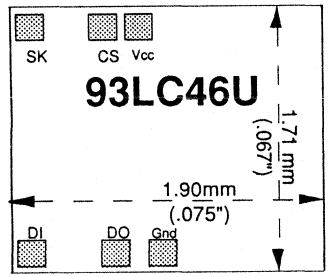
Preliminary

1,024-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

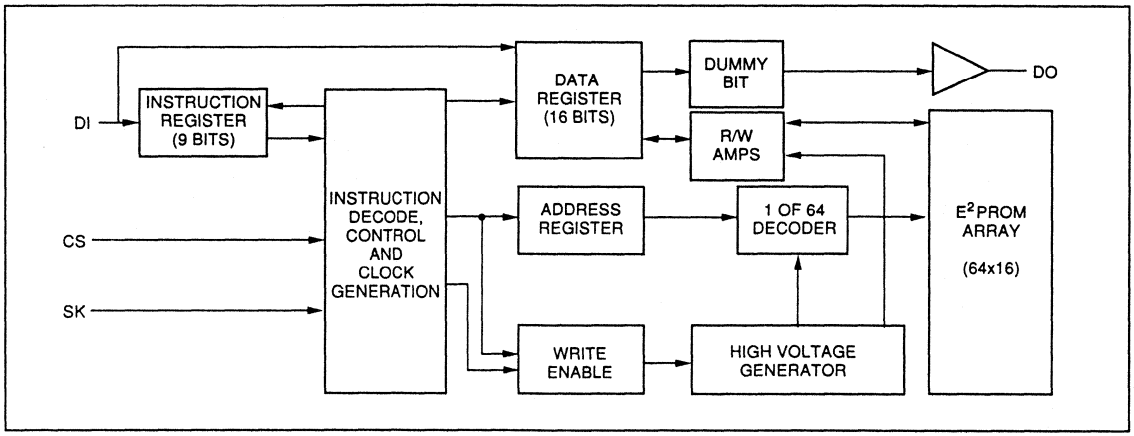
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC46U is a low cost 1,024-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC46U provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC46U dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC46U is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC46U is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC46U is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC46U will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC46U has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC46U is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5 volts, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC46U has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{BUSY}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{BUSY}$ flag. Therefore, it is important if you want to access the READY/$\overline{BUSY}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pad indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC46U has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC46U is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC46U ..... 0°C to +70°C
XLE93LC46U ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46U or -40°C to +85°C for the XLE93LC46U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4	n/a	n/a	V

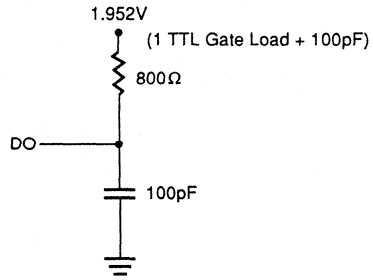
AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46U or -40°C to +85°C for the XLE93LC46U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10	n/a	n/a	ms

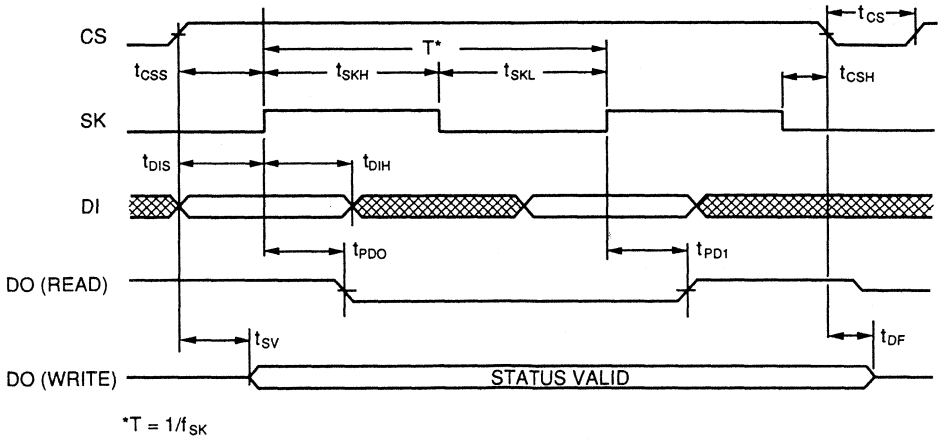
CAPACITANCE
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



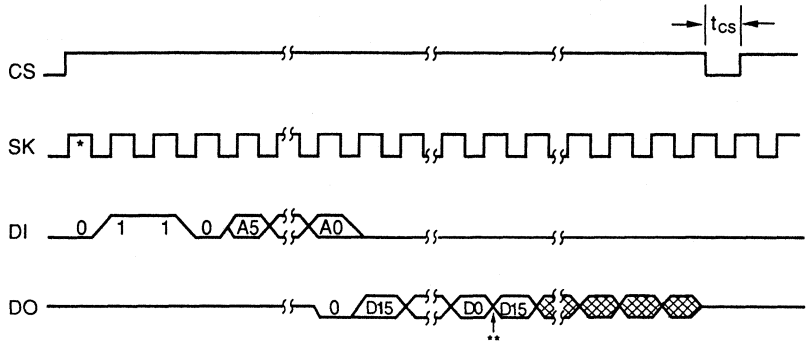
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



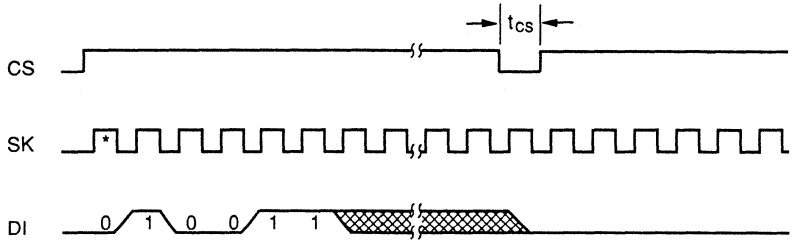
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

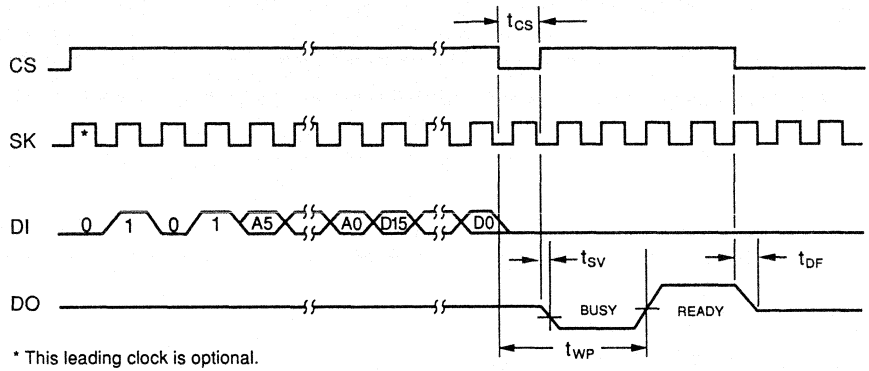


FIGURE 5. WRITE CYCLE TIMING

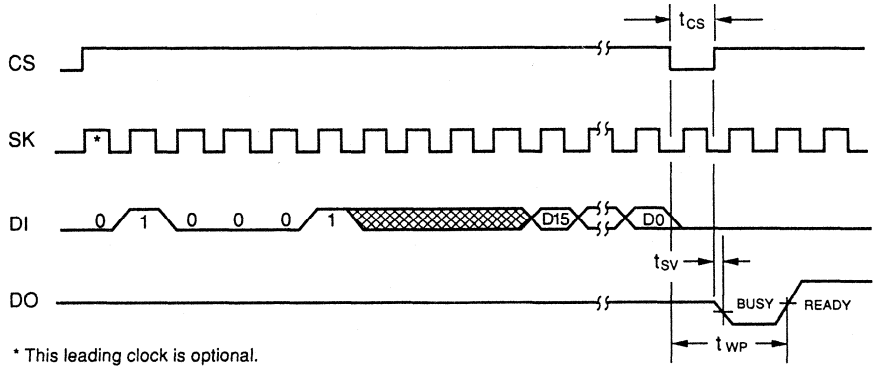
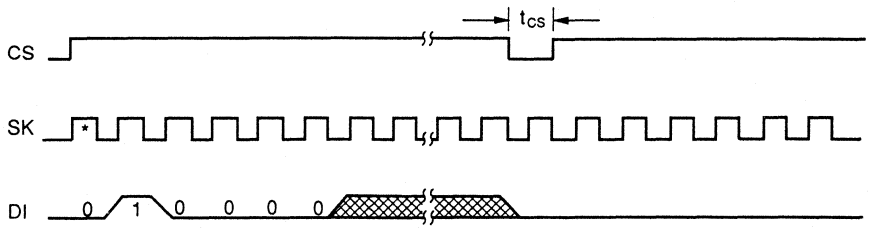


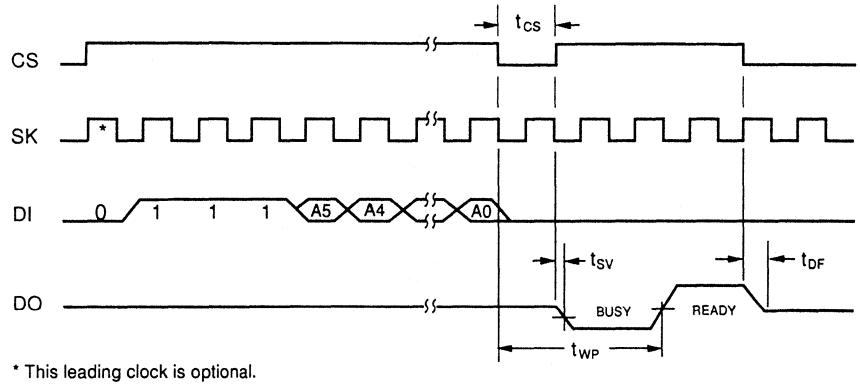
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

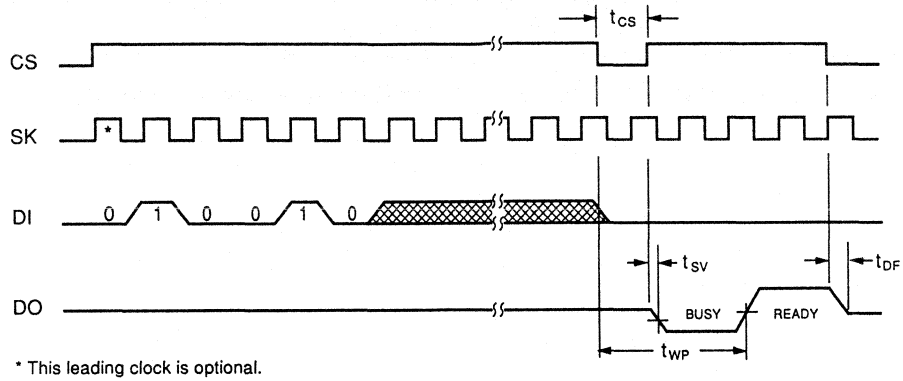
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

XL93LC46-3

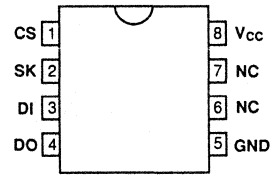
1,024-Bit Serial (3V to 5V) Electrically Erasable PROM **with 2V Read Capability**

FEATURES

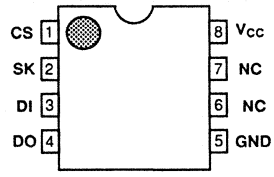
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

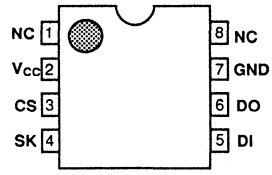
Plastic Dual-in-line "P" Package



EIAJ Small Outline "JR" Package



EIAJ Small Outline "J" Package



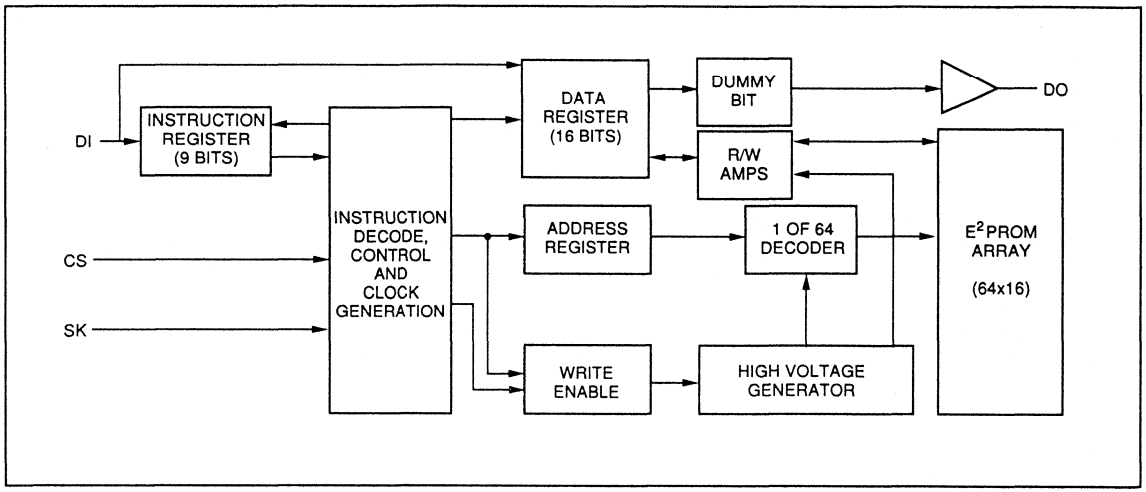
OVERVIEW

The XL93LC46-3 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC46-3 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

BLOCK DIAGRAM



The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

APPLICATIONS

The XL93LC46-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC46-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC46-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC46-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC46-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC46-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** $V_{IL} = 0.1\ V_{CC}$ min., $V_{IH} = 0.9\ V_{CC}$ min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC46-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC46-3 ..... 0°C to +70°C
XLE93LC46-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46-3 or -40°C to +85°C for the XLE93LC46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC46-3		XLE93LC46-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46-3 or -40°C to +85°C for the XLE93LC46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC46-3		XLE93LC46-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐¯	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐¯	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¯⌐	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐¯	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46-3 or -40°C to +85°C for the XLE93LC46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC46-3		XLE93LC46-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46-3 or -40°C to +85°C for the XLE93LC46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC46-3		XLE93LC46-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐¯	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐¯	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¯⌐	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐¯	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

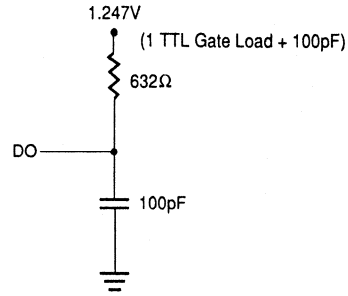
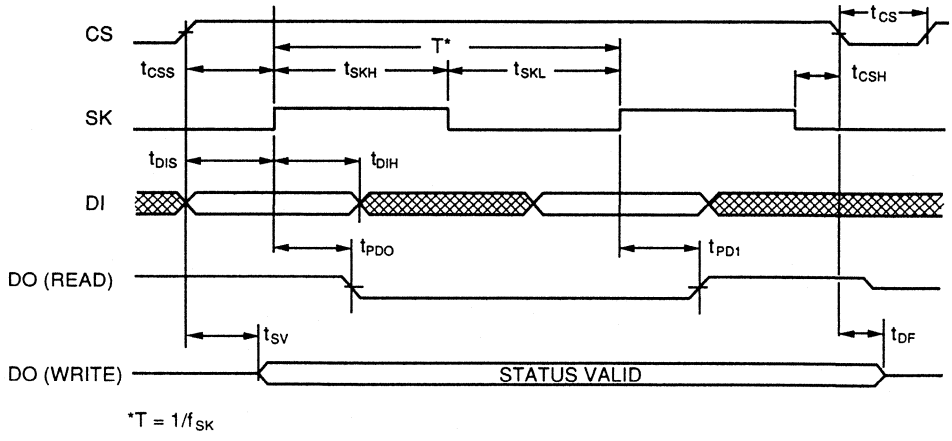
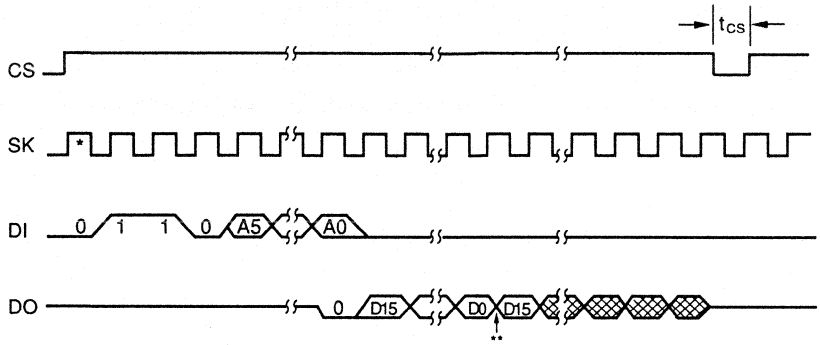


FIGURE 1. AC TEST CONDITIONS



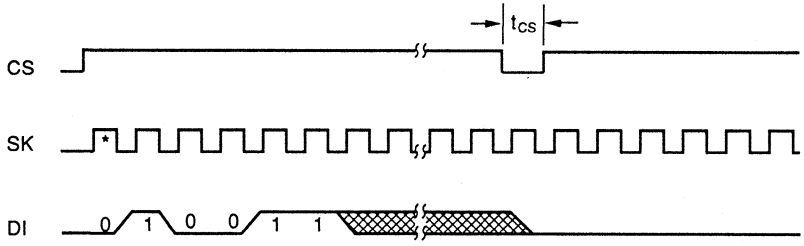
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

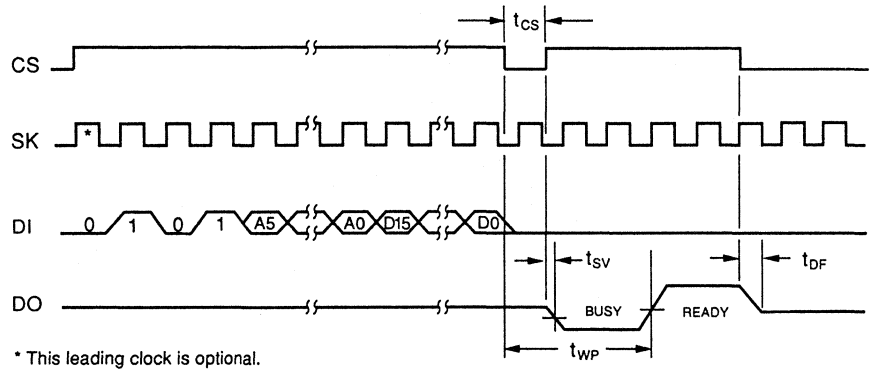
FIGURE 3. READ CYCLE TIMING



DO = 3-state

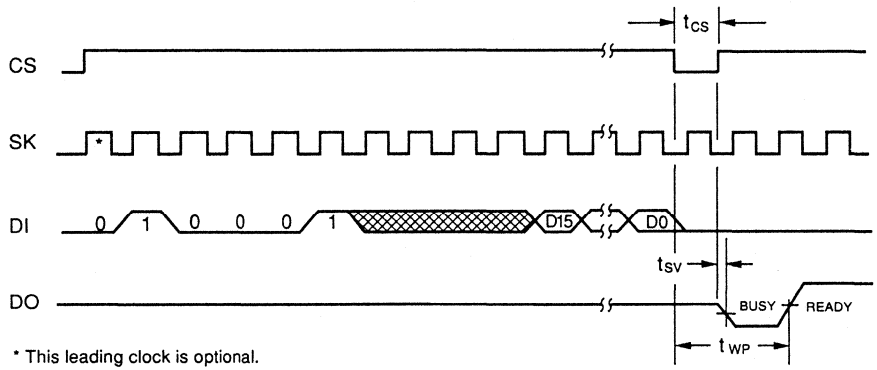
* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



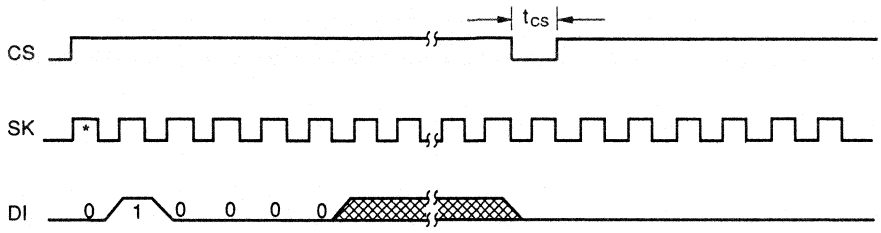
* This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



* This leading clock is optional.

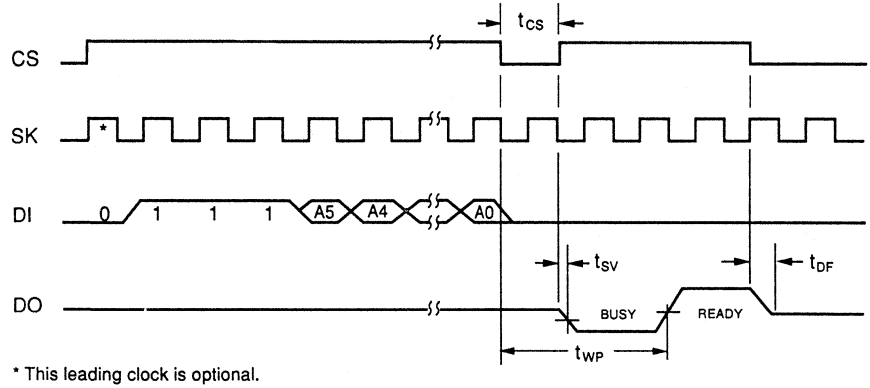
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

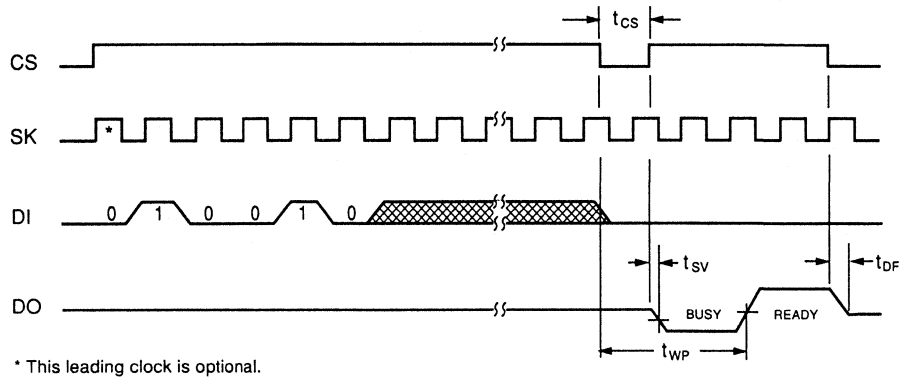
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

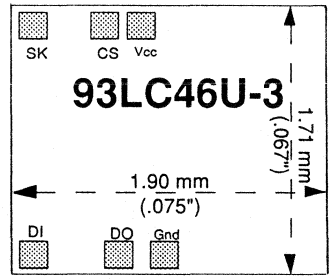
Preliminary

1,024-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

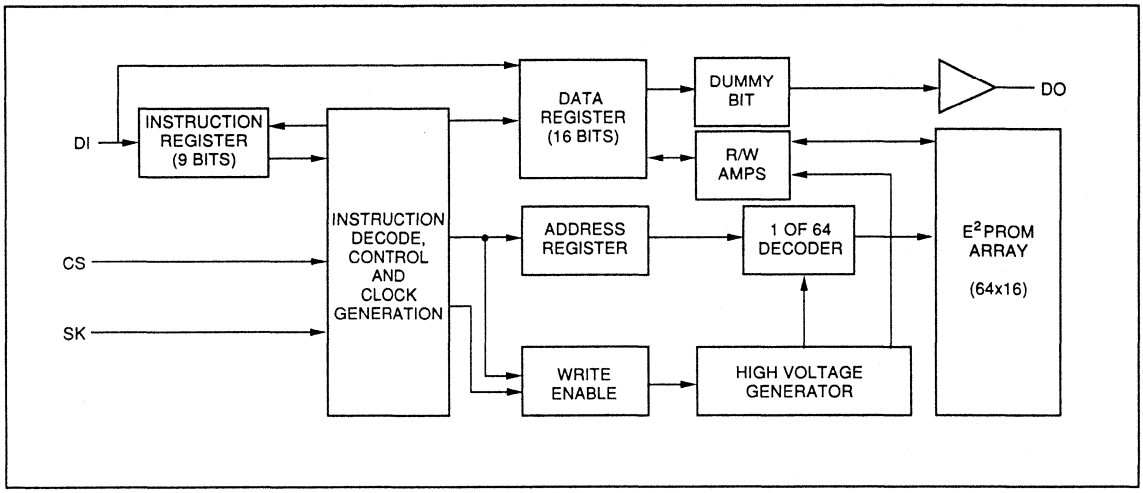
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC46U-3 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC46U-3 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC46U-3 dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/BUSY status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC46U-3 is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC46U-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC46U-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC46U-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC46U-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC46U-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** V_{IL} = 0.1 V_{CC} min., V_{IH} = 0.9 V_{CC} min.; **AC:** t_{SKH} = 2μs min., t_{SKL} = 2μs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC46U-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (tCS), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pad indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tCS, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC46U-3 ..... 0°C to +70°C
XLE93LC46U-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46U-3 or -40°C to +85°C for the XLE93LC46U-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC46U-3		XLE93LC46U-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46U-3 or -40°C to +85°C for the XLE93LC46U-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC46U-3		XLE93LC46U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC46U-3 or -40°C to +85°C for the XLE93LC46U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC46U-3		XLE93LC46U-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

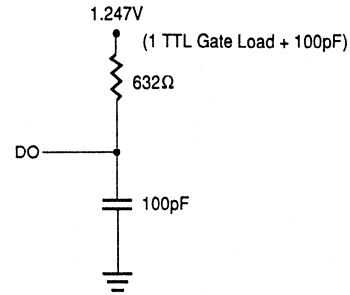
T_A = 0°C to +70°C for the XLS93LC46U-3 or -40°C to +85°C for the XLE93LC46U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC46U-3		XLE93LC46U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

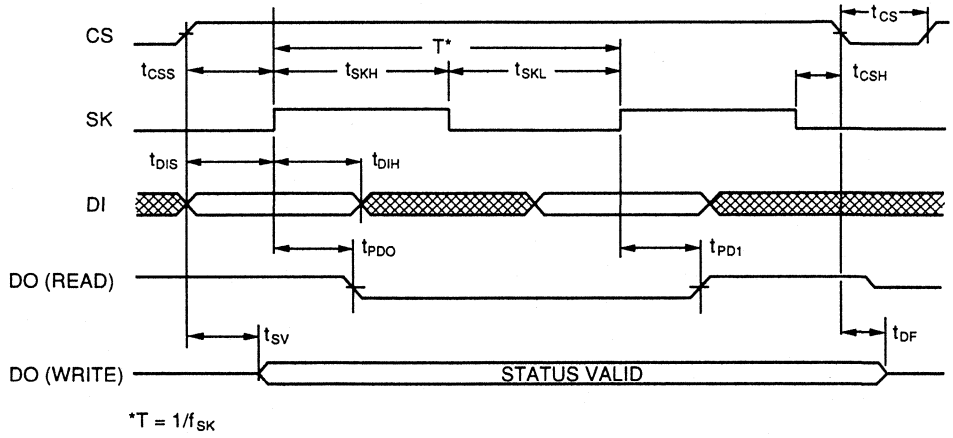
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



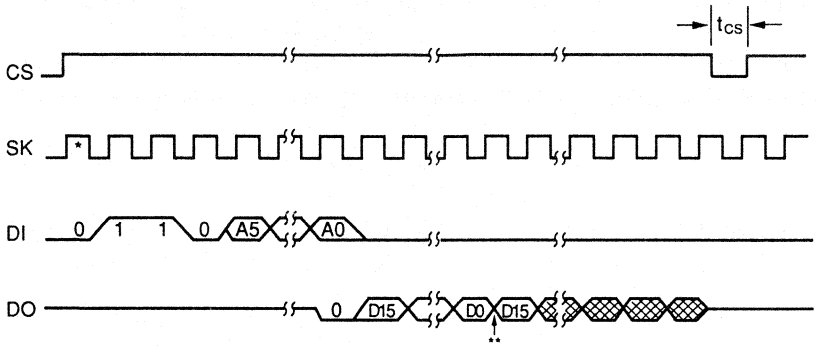
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



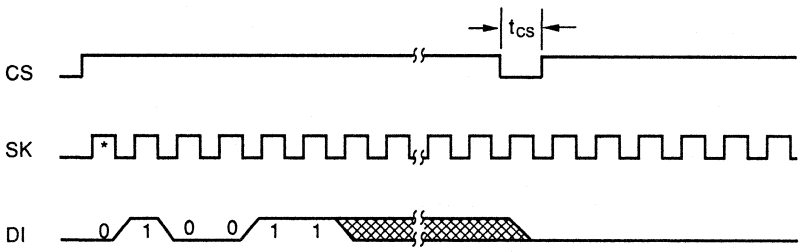
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

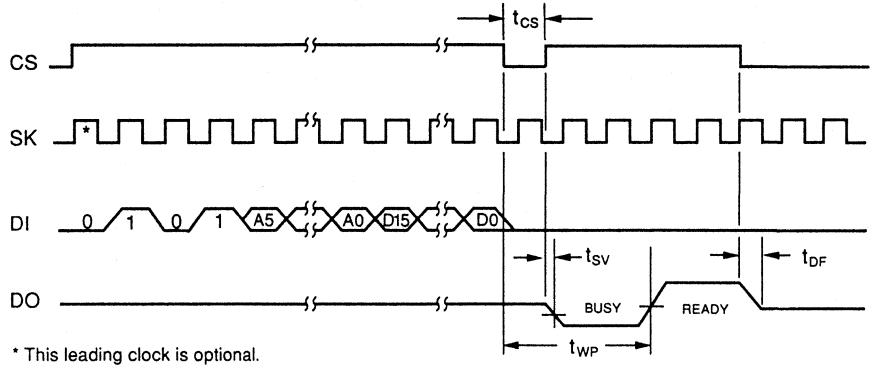
FIGURE 3. READ CYCLE TIMING



DO = 3-state

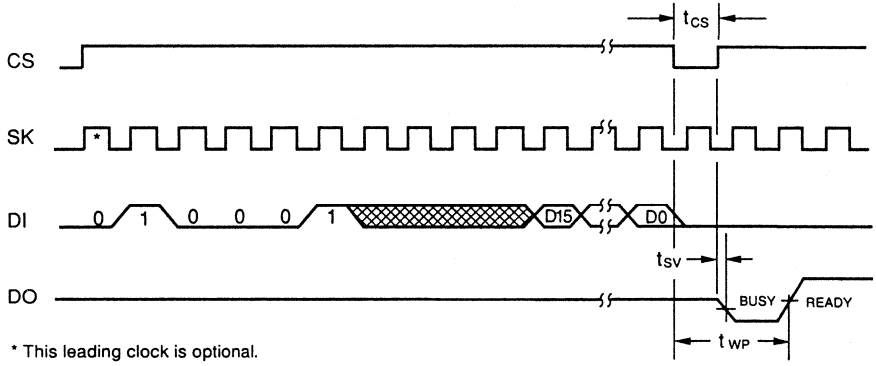
* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



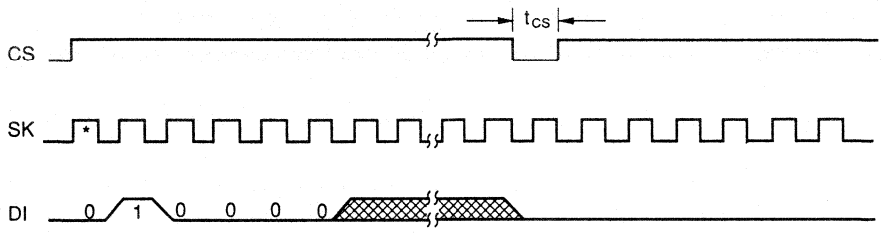
* This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



* This leading clock is optional.

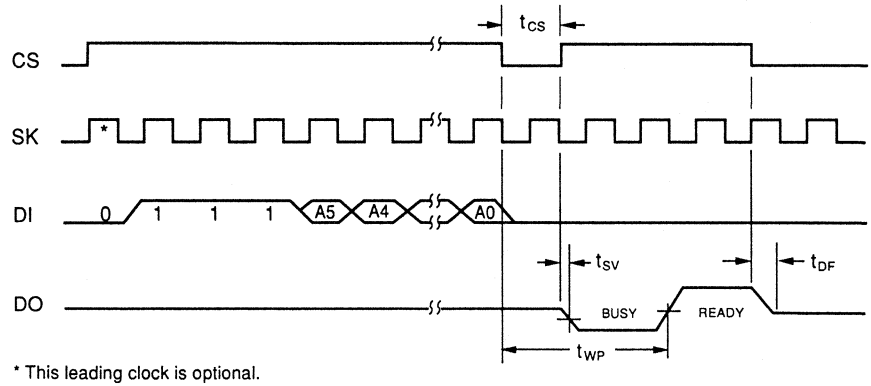
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

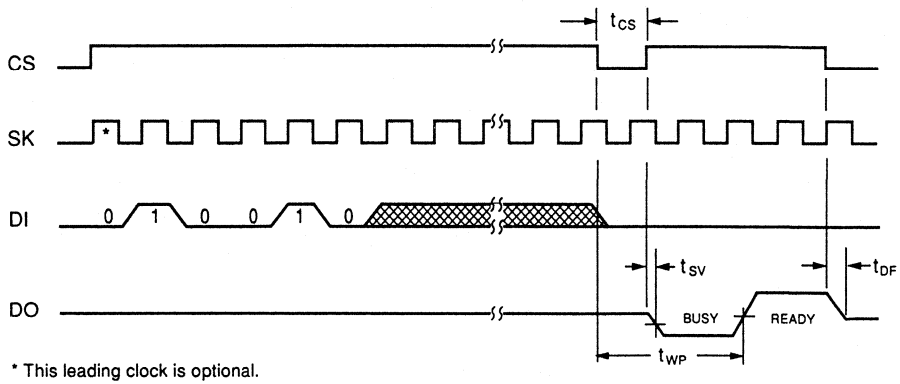
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

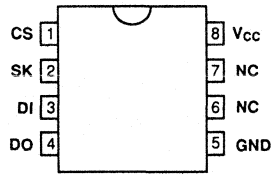
1,024-Bit Serial Electrically Erasable PROM with 2V Read Capability

FEATURES

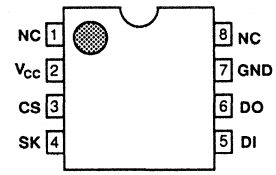
- State-of-the-Art Architecture
  - — Nonvolatile data storage
  - — Single supply - 5V operation
  - — Fully TTL compatible inputs and outputs
  - — Auto increment for efficient data dump
  - — 1MHz operation
- Hardware and Software Write Protection
  - — Defaults to write-disabled state at power up
  - — Software instructions for write-enable/disable
- Low Power Consumption
  - — 1mA active (typical)
  - — 1µA standby (typical)
- Low Voltage Read Operations
  - — Reliable read operations down to 2.0 volts
- Advanced Low Voltage CMOS E²PROM Technology
- Versatile, Easy-to-Use Interface
  - — Self-timed programming cycle
  - — Automatic erase-before-write
  - — Programming Status Indicator
  - — Word and chip erasable
- Durable and Reliable
  - — 10-year data retention after 100K write cycles
  - — Minimum of 100,000 write cycles per word
  - — Unlimited read cycles
  - — ESD protection

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



EIAJ Small Outline "J" Package



PIN NAMES

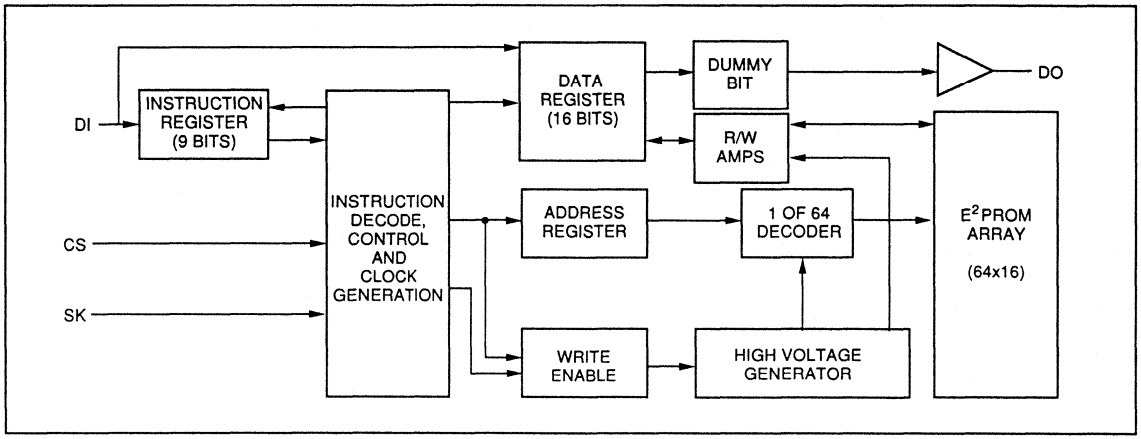
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93C46 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93C46 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93C46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93C46 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93C46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93C46 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93C46 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93C46 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93C46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (tCS), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tCS), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of tCS, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93C46 ..... 0°C to +70°C
XLE93C46 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C46 or -40°C to +85°C for the XLE93C46

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz @ 5V SK = 250KHz @ 2V		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

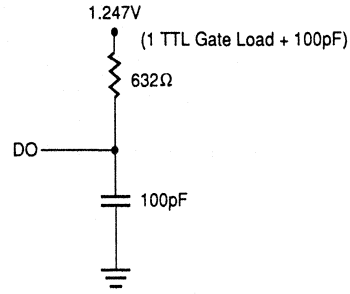
T_A = 0°C to +70°C for the XLS93C46 or -40°C to +85°C for the XLE93C46

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time		400		2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐¯	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐¯	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¯⌐	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐¯	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L= 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		n/a	ms

CAPACITANCE

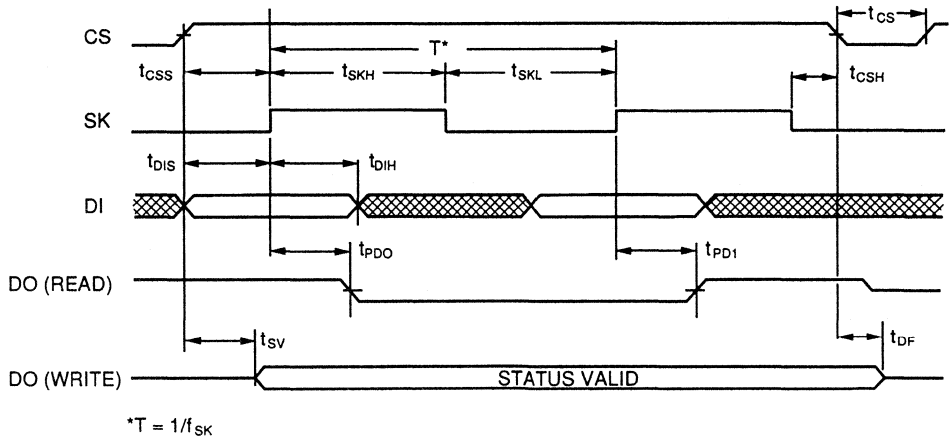
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



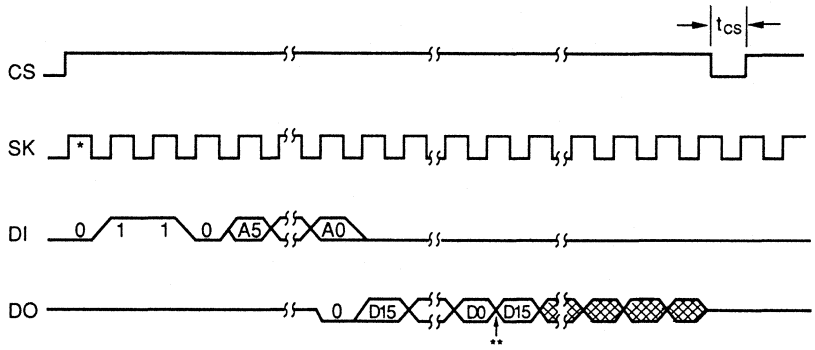
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



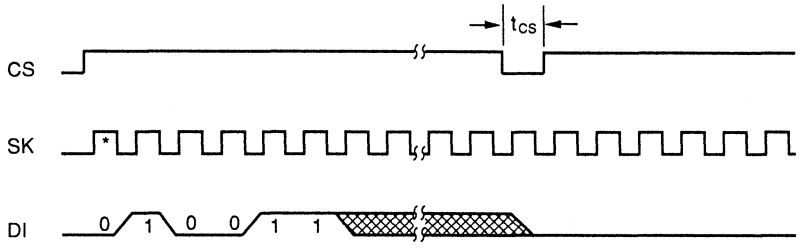
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

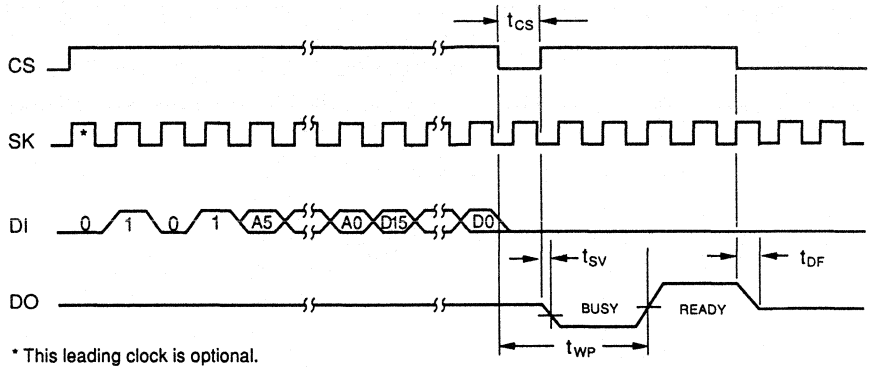


FIGURE 5. WRITE CYCLE TIMING

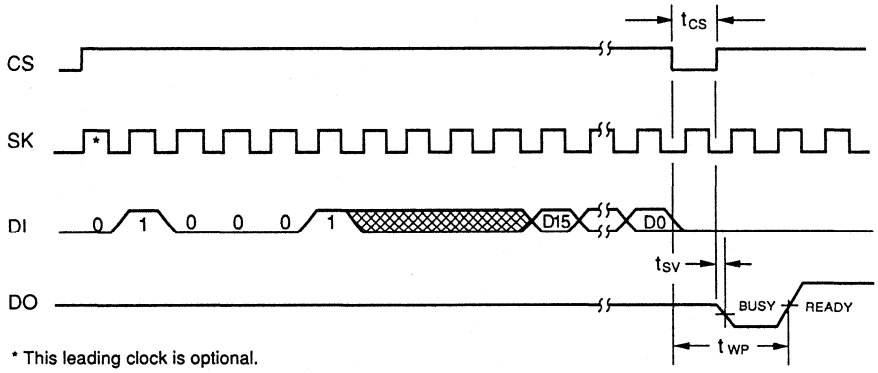
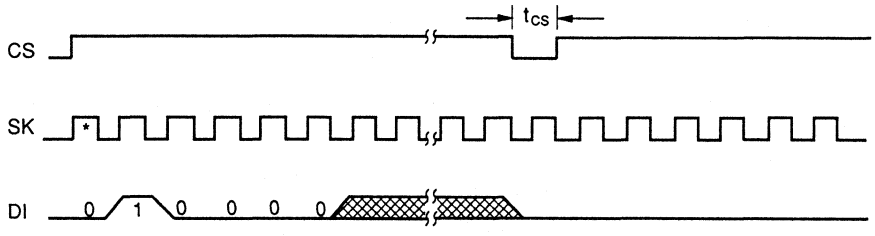


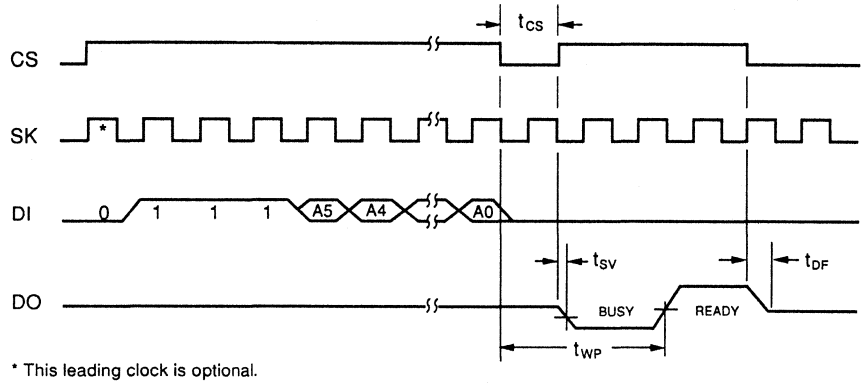
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

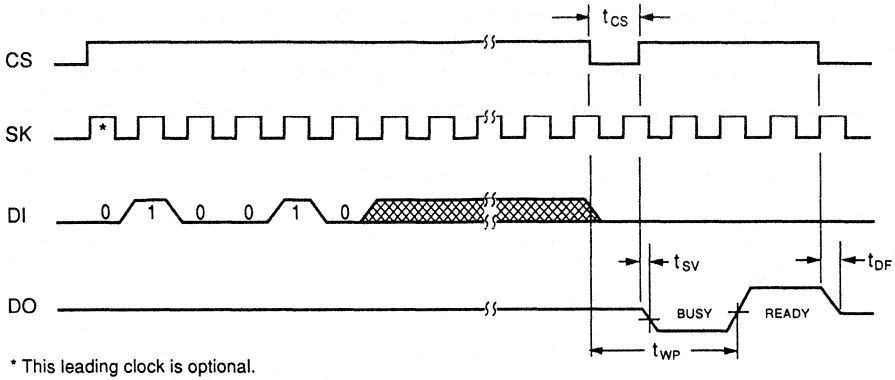
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

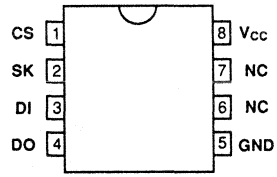
1,024-Bit Serial (3V to 5V) Electrically Erasable PROM
with 2V Read Capability

FEATURES

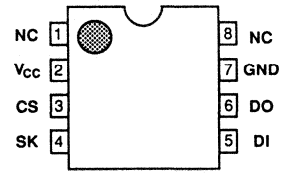
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



EIAJ Small Outline "J" Package



PIN NAMES

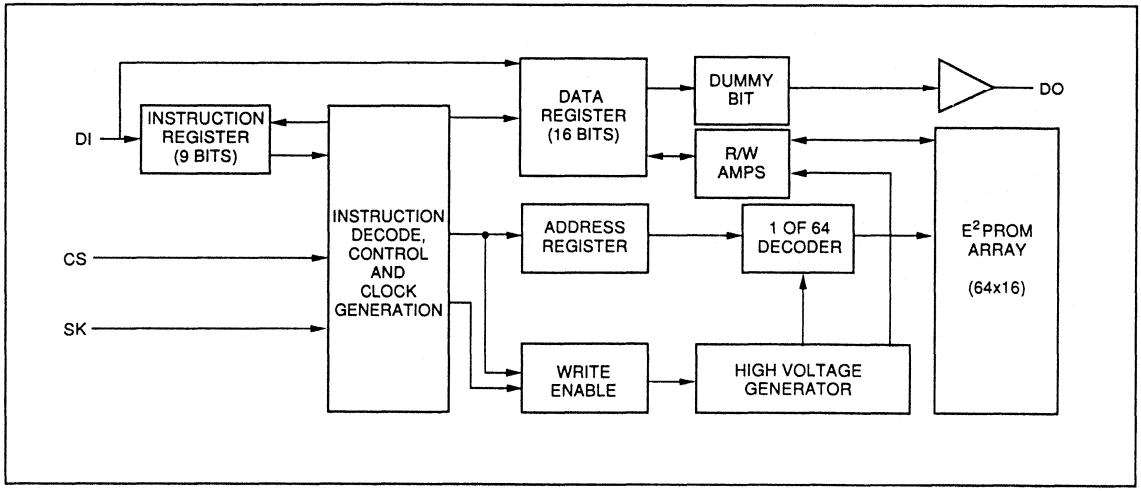
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93C46-3 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93C46-3 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93C46-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93C46-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93C46-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93C46-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93C46-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93C46-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls to 2.0V, the normal 3V specs apply, except for the following: **DC:** $V_{IL} = 0.1\ V_{CC}$ min., $V_{IH} = 0.9\ V_{CC}$ min.; **AC:** t_{SKH} = 2μs min., t_{SKL} = 2μs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93C46-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93C46-3 ..... 0°C to +70°C
XLE93C46-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C46-3 or -40°C to +85°C for the XLE93C46-3, V_{CC}= 3V ±10%

Symbol	Parameter	Conditions	XLS93C46-3		XLE93C46-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current	CS = V_{IH}, SK = 250KHz CMOS Input Levels		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C46-3 or -40°C to +85°C for the XLE93C46-3, V_{CC}= 3V ±10%

Symbol	Parameter	Conditions	XLS93C46-3		XLE93C46-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C46-3 or -40°C to +85°C for the XLE93C46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93C46-3		XLE93C46-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C46-3 or -40°C to +85°C for the XLE93C46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93C46-3		XLE93C46-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		400		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐¯	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐¯	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¯⌐	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐¯	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

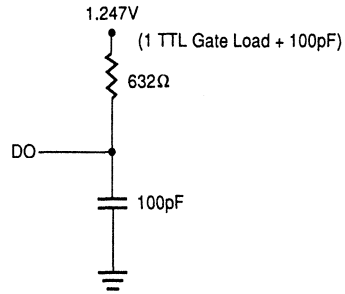
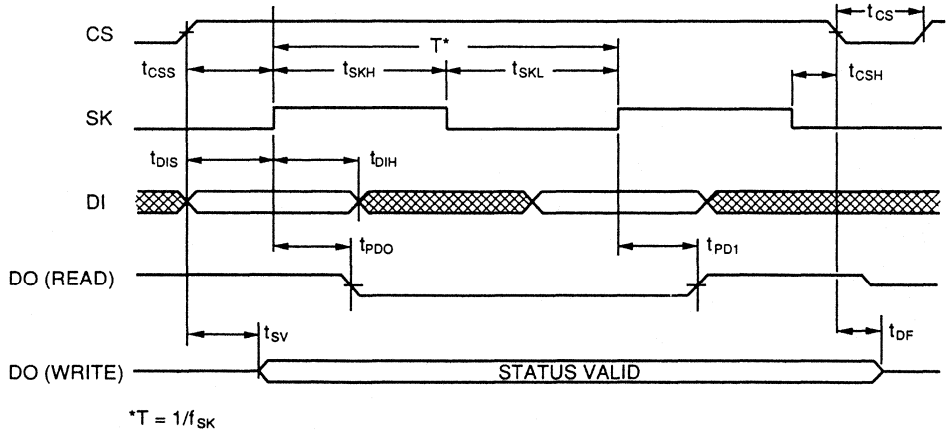
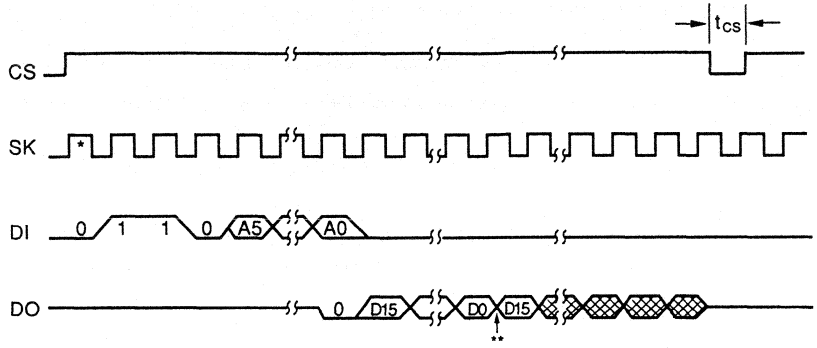


FIGURE 1. AC TEST CONDITIONS



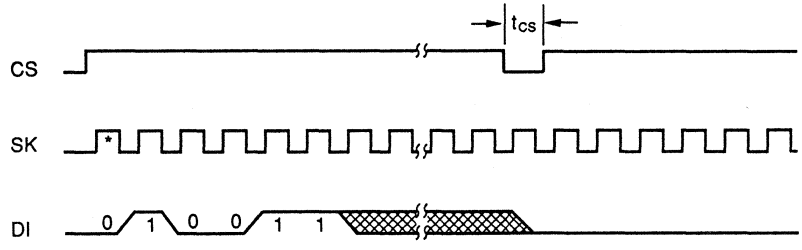
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

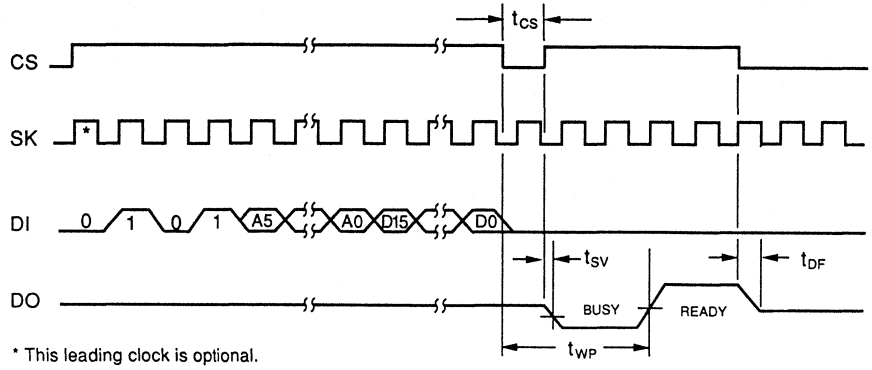


FIGURE 5. WRITE CYCLE TIMING

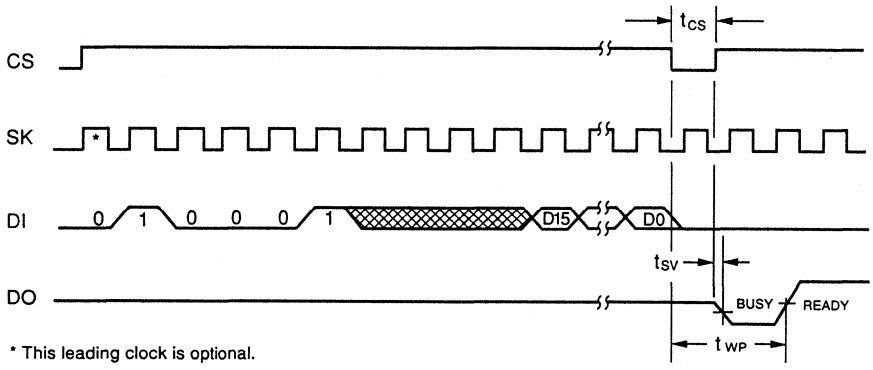
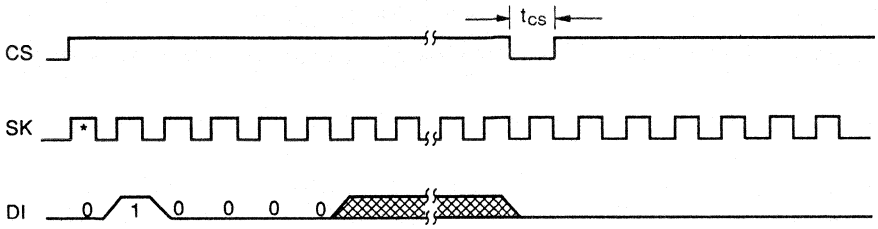


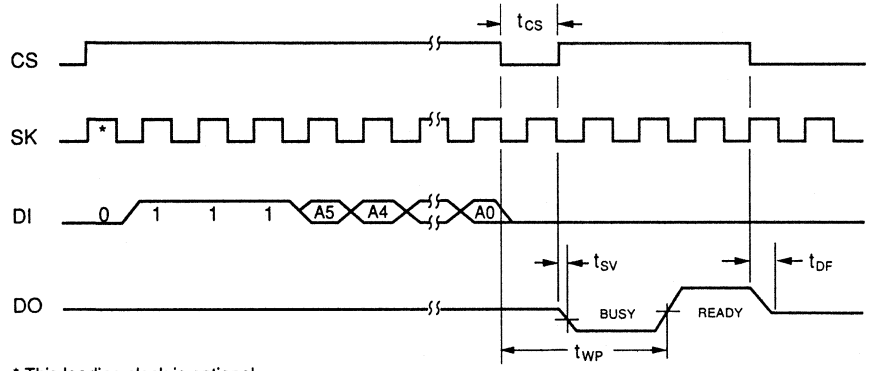
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

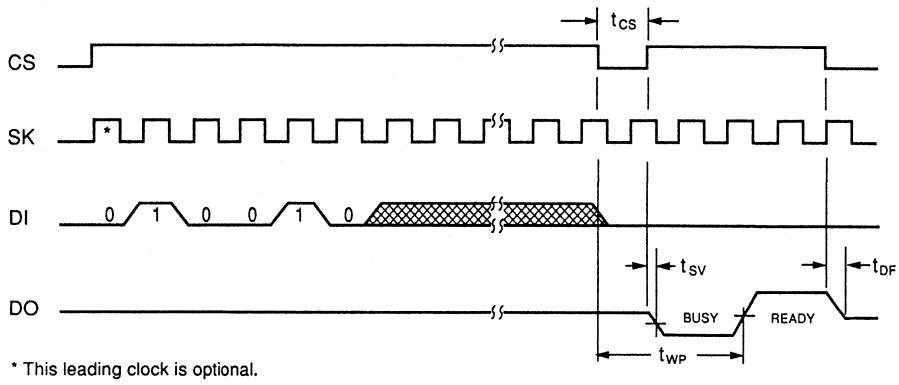
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

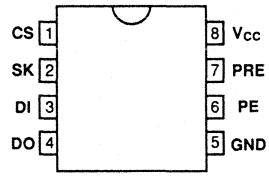
1,024-Bit Serial (5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

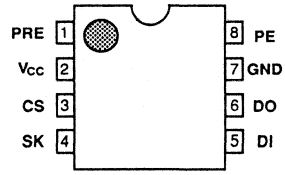
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— Pin-enabled writes to memory and Protect Register**
  - **— Temporary or permanent protection of selected registers**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

Plastic Dual-in-line
Type "P" Package



EIAJ Small Outline
"J" Package



PIN NAMES

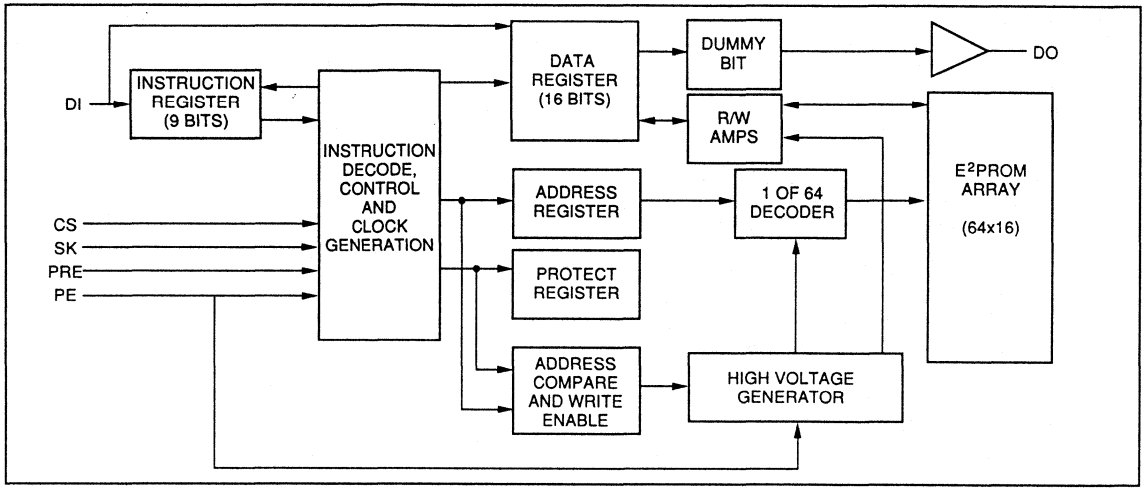
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

OVERVIEW

The XL93CS46 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93CS46 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Any number of the registers can be protected against data modification by programming the on-chip Protect Register. This register holds the address of the lowest memory register to be protected. The value in the Protect Register can be frozen, ensuring that the selected range of registers can never be altered. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. To protect against inadvertent writes, the WRITE instruction is accepted only while Program Enable (PE) is held HIGH, and only functions if the selected address is less than the address in the

BLOCK DIAGRAM



Protect Register. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{BUSY}$ status of the chip.

APPLICATIONS

The XL93CS46 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93CS46 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93CS46 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93CS46 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93CS46 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93CS46 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93CS46 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle. While the WRITE instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The WRALL instruction functions only when the Protect Register has been cleared by a PRCLEAR instruction. While the WRALL instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write-disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A_5-A_0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A_5-A_0)	D_{15}-D_0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A_5-A_0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE REGISTER	1	11	(A_5-A_0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. Registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands cannot be erased. (See Figure 8)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."The erase all (ERAL) command will not erase registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands. (See Figure 9.)

PROTECTION REGISTER LOGIC

Protect Register Read (PRREAD)
The protect register read (PRREAD) instruction causes the address stored in the Protect Register to be output on the DO pin. Data is transferred from the Protect Register into a serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 10.)

After a PRCLEAR instruction is executed, a PRREAD instruction will return all 1's, even though the highest register is NOT protected.

Protect Register Enable (PREN)
The protect register enable (PREN) instruction enables execution of the PRCLEAR, PRWRITE and PRDS instructions. It must be executed immediately before each of these instructions. (The PREN instruction functions only if the part has been write enabled; see the WEN instruction). Both the PRE and PE pins must be held HIGH while the PREN instruction is being loaded; then they become DON'T-CAREs. (See Figure 11.)

Protect Register Clear (PRCLEAR)
The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making all registers accessible to the WRITE and WRALL instructions. If a PRDS instruction has been executed, the PRCLEAR instruction will not function. A PREN instruction must be executed immediately before a PRCLEAR instruction. While the PRCLEAR instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure12.)

Protect Register Write (PRWRITE)
The protect register write (PRWRITE) instruction is used to load the Protect Register with the address of the lowest register to be protected. After the PRWRITE instruction is executed, only registers with addresses less than the address in the Protect Register can be written by the WRITE instruction. The Protect Register must have been cleared (see the PRCLEAR instruction) before executing a PRWRITE instruction. A PREN instruction must be executed immediately before the PRWRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 13.)

Protect Register Disable (PRDS)
The protect register disable (PRDS) instruction is effective exactly once per part. After this instruction has been executed, the Protect Register will accept no further modifications. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the WRITE and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. While the PRDS instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 14.)

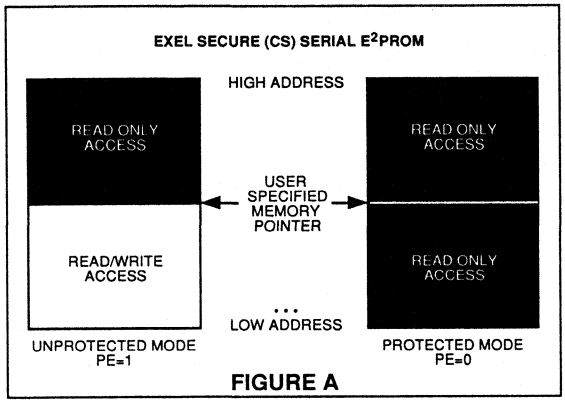


FIGURE A

Figure A shows the status of the memory array regions as defined by the pointer address and the state of the program enable (PE) pin. In the first case, programming operations are enabled through the application of a logic "1" to the PE control pin. All memory locations beneath that of the pointer address are available for data changes. All memory locations at or above the pointer address are protected against data alteration and serve as read only memory.

In the second case, the PE pin is held in a logic "0" state. While this condition is present, the XL93CS46 is protected against any data changes.

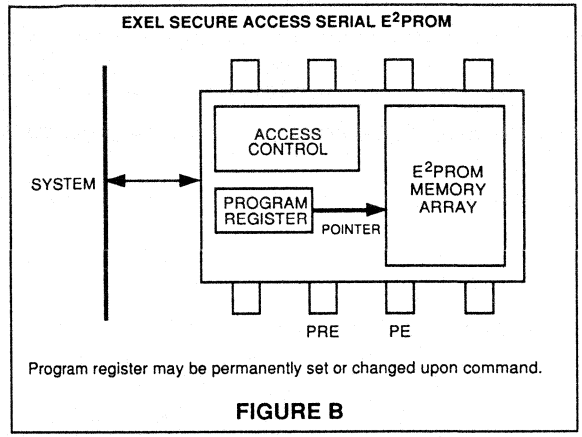


FIGURE B

The conceptual block diagram, Figure B above, shows the simplicity with which the security features of the XL93CS46 may be managed.

The program register is accessed for read or write operations whenever the program register enable (PRE) pin is in a logic "1" state. Normal write operations to the program register establish the E^2 memory array address defining the region to be protected.

When PRE is in a logic "0" state, all read and write operations directed to the XL93CS46 affect the E^2PROM memory array locations.

Setting the address in the program register to the top of the XL93CS46 memory array renders the entire array to be writable. Setting the address to the bottom of the array renders the entire array to be a read only memory.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93CS46 ..... 0°C to +70°C
XLE93CS46 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46 or -40°C to +85°C for the XLE93CS46

			Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz @ 5V SK = 250KHz @ 2V		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, PE and PRE	-20.0	20.0	-1	1	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc - 0.2		Vcc - 0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46 or -40°C to +85°C for the XLE93CS46

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time		400		2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{PRES}	PRE Setup Time	Relative to SK ⌐	50				ns
t_{PES}	PE Setup Time	Relative to SK ⌐	50				ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⌙	0		0		ns
t_{PEH}	PE Hold Time	Relative to CS ⌙	50				ns
t_{PREH}	PRE Hold Time	Relative to CS ⌙	50				ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L= 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10			ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

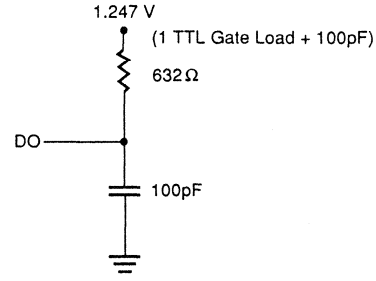


FIGURE 1. AC TEST CONDITIONS

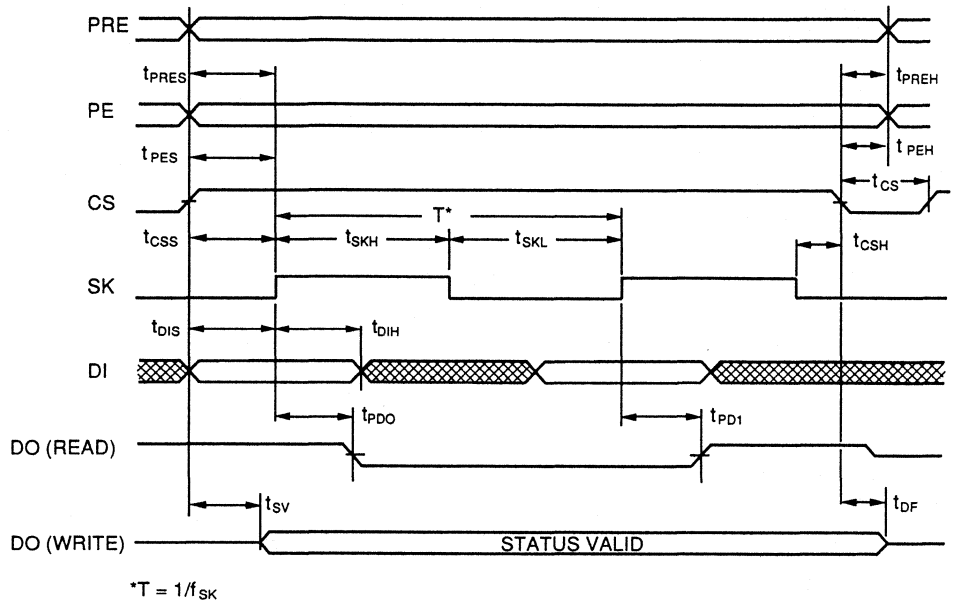
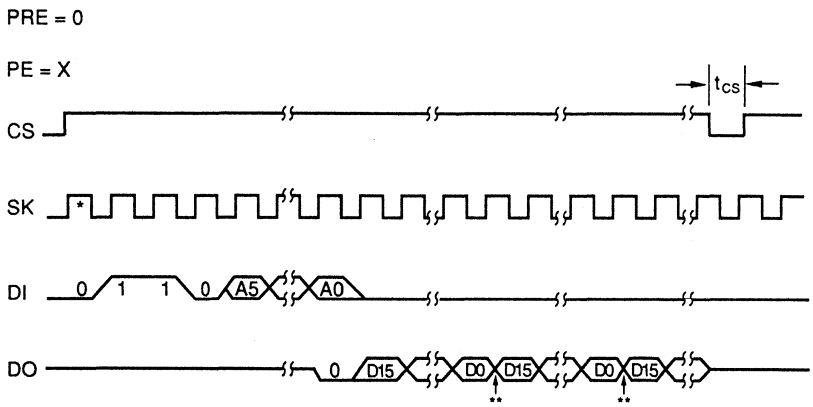


FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING

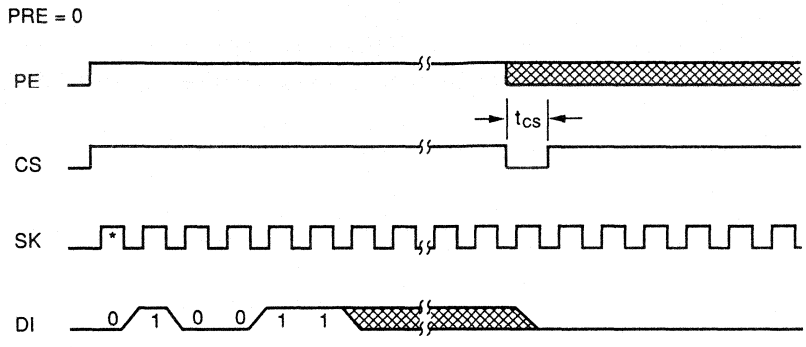


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

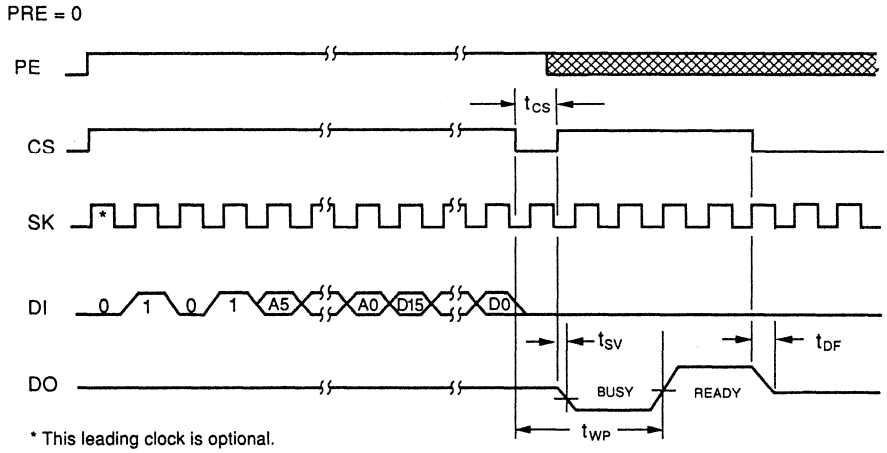


FIGURE 5. WRITE CYCLE TIMING

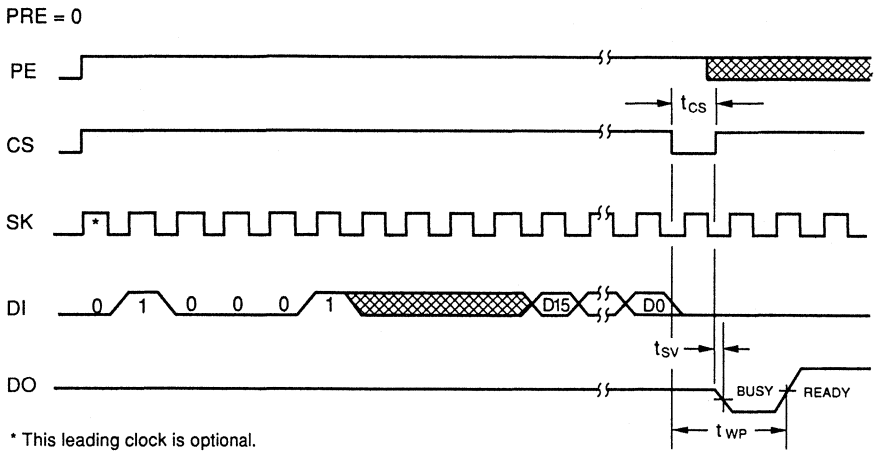


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

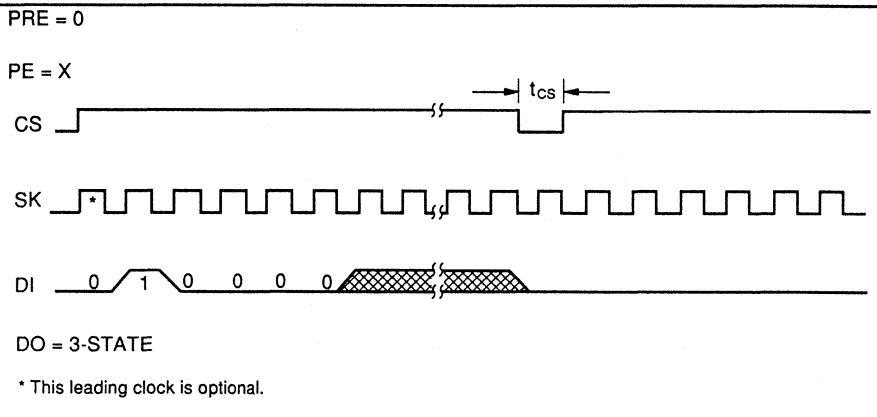
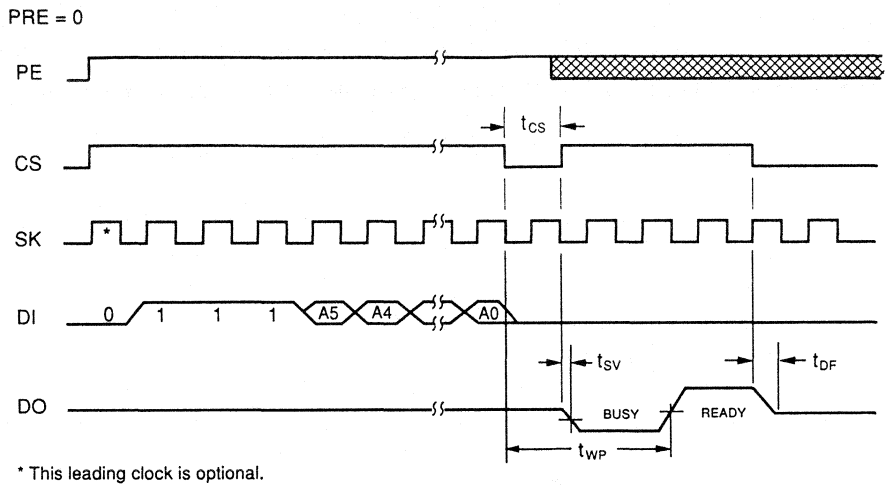
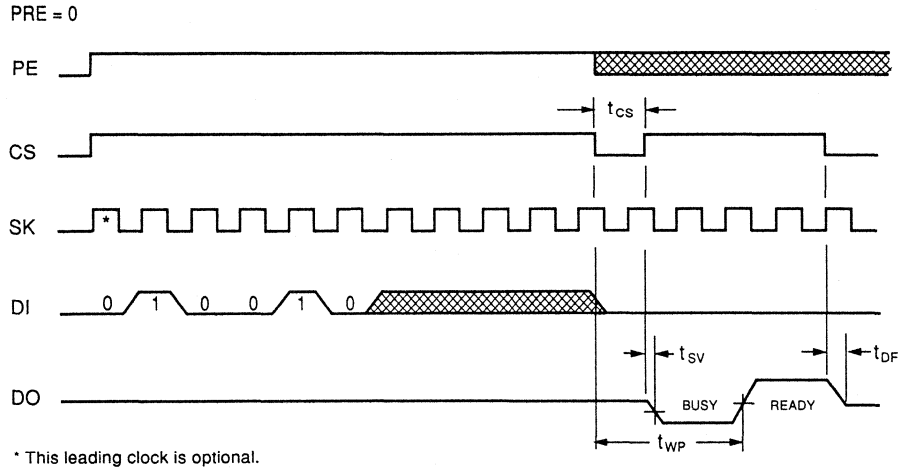


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



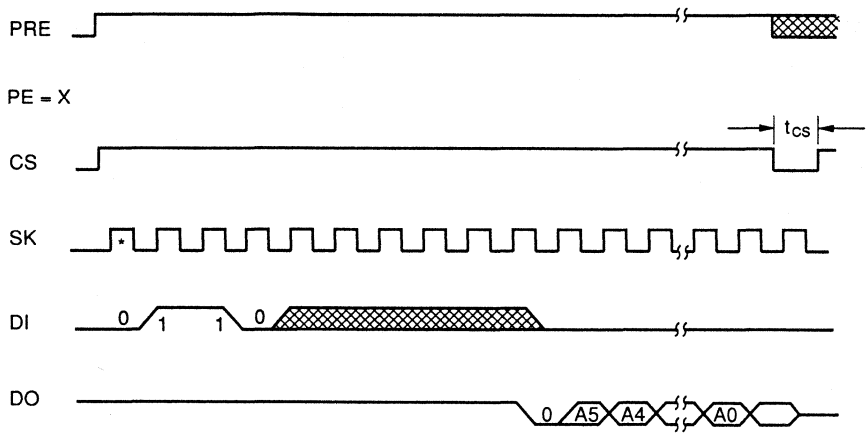
* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



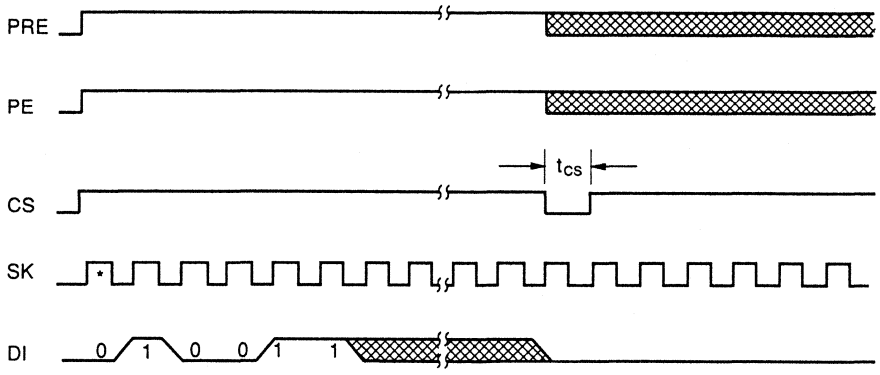
* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING



* This leading clock is optional.

FIGURE 10. PROTECT REGISTER READ (PRREAD) CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 11. PROTECT REGISTER ENABLE (PREN) CYCLE TIMING

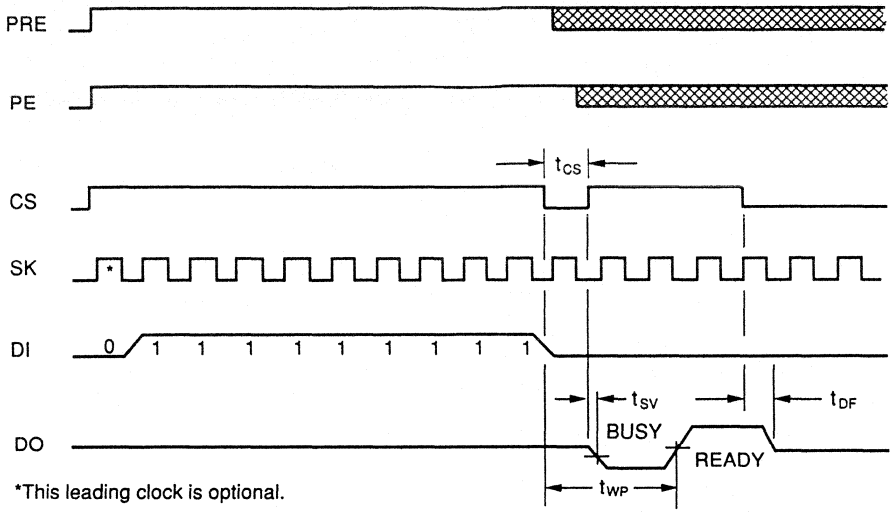


FIGURE 12. PROTECT REGISTER CLEAR (PRCLEAR) CYCLE TIMING

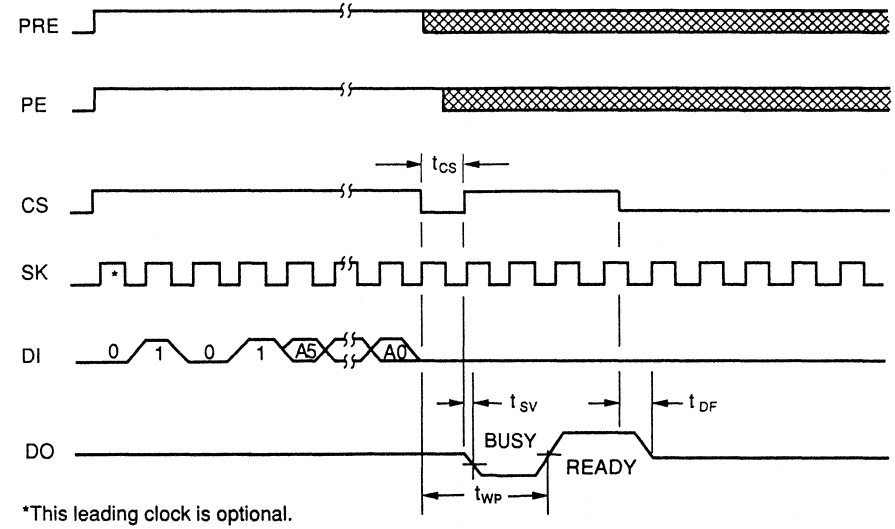


FIGURE 13. PROTECT REGISTER WRITE (PRWRITE) CYCLE TIMING

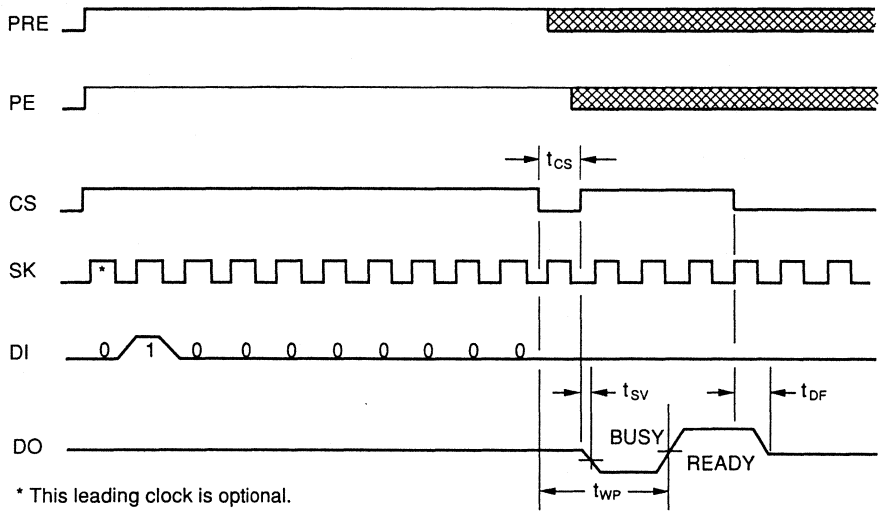


FIGURE 14. PROTECT REGISTER DISABLE (PRDS) CYCLE TIMING

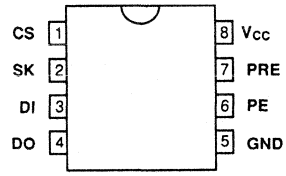
1,024-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

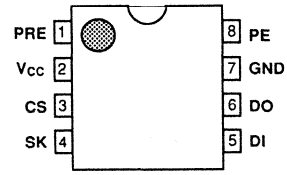
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— Pin-enabled writes to memory and Protect Register**
  - **— Temporary or permanent protection of selected registers**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

Plastic Dual-in-line
Type "P" Package



EIAJ Small Outline
"J" Package



PIN NAMES

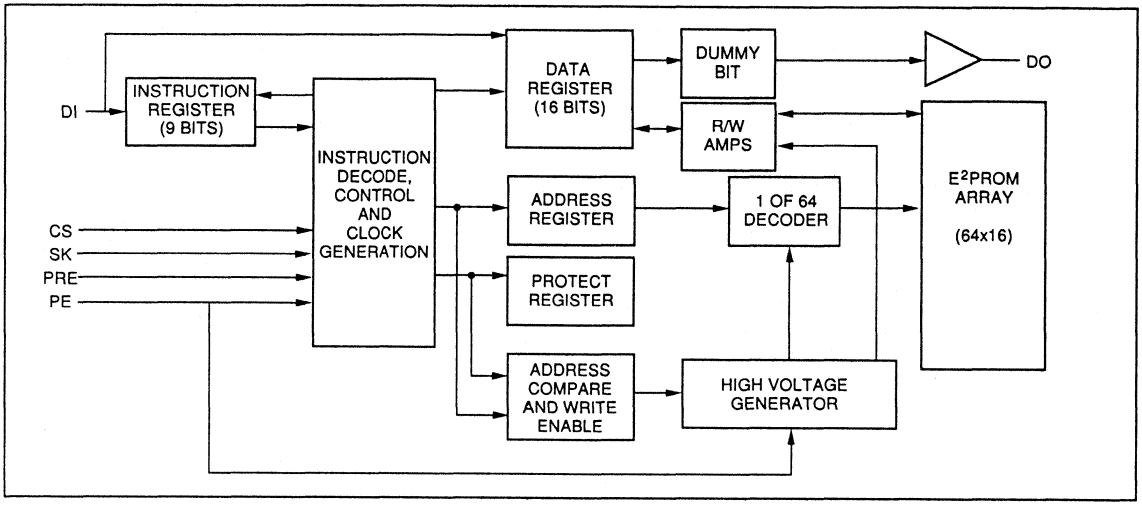
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

OVERVIEW

The XL93CS46-3 is a low cost 1,024-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93CS46-3 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. Any number of the registers can be protected against data modification by programming the on-chip Protect Register. This register holds the address of the lowest memory register to be protected. The value in the Protect Register can be frozen, ensuring that the selected range of registers can never be altered. Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. To protect against inadvertent writes, the WRITE instruction is accepted only while Program Enable (PE) is held HIGH, and only functions if the selected address is less than the address in the

BLOCK DIAGRAM



Protect Register. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

APPLICATIONS

The XL93CS46-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93CS46-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93CS46-3 is controlled by seven 9-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (6 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93CS46-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93CS46-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93CS46-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.0V, the normal 3V specs apply, except for the following: **DC:** V_{IL} = 0.1 V_{CC} min., V_{IH} = 0.9 V_{CC} min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93CS46-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle. While the WRITE instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The WRALL instruction functions only when the Protect Register has been cleared by a PRCLEAR instruction. While the WRALL instruction is being loaded, the PE pin must be held HIGH; then it becomes a DON'T-CARE.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A_5-A_0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A_5-A_0)	D_{15}-D_0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A_5-A_0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE REGISTER	1	11	(A_5-A_0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. Registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands cannot be erased. (See Figure 8)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."The erase all (ERAL) command will not erase registers protected by the protect register write (PRWRITE) or protect register disable (PRDS) commands. (See Figure 9.)

PROTECTION REGISTER LOGIC

Protect Register Read (PRREAD)
The protect register read (PRREAD) instruction causes the address stored in the Protect Register to be output on the DO pin. Data is transferred from the Protect Register into a serial-out shift register. A dummy bit (logical "0") precedes the actual output string. The data on the DO pin changes with the LOW to HIGH transition of the SK clock. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH; then it becomes a DON'T-CARE. (See Figure 10.)

After a PRCLEAR instruction is executed, a PRREAD instruction will return all 1's, even though the highest register is NOT protected.

Protect Register Enable (PREN)
The protect register enable (PREN) instruction enables execution of the PRCLEAR, PRWRITE and PRDS instructions. It must be executed immediately before each of these instructions. (The PREN instruction functions only if the part has been write enabled; see the WEN instruction). Both the PRE and PE pins must be held HIGH while the PREN instruction is being loaded; then they become DON'T-CAREs. (See Figure 11.)

Protect Register Clear (PRCLEAR)
The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making all registers accessible to the WRITE and WRALL instructions. If a PRDS instruction has been executed, the PRCLEAR instruction will not function. A PREN instruction must be executed immediately before a PRCLEAR instruction. While the PRCLEAR instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure12.)

Protect Register Write (PRWRITE)
The protect register write (PRWRITE) instruction is used to load the Protect Register with the address of the lowest register to be protected. After the PRWRITE instruction is executed, only registers with addresses less than the address in the Protect Register can be written by the WRITE instruction. The Protect Register must have been cleared (see the PRCLEAR instruction) before executing a PRWRITE instruction. A PREN instruction must be executed immediately before the PRWRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 13.)

Protect Register Disable (PRDS)
The protect register disable (PRDS) instruction is effective exactly once per part. After this instruction has been executed, the Protect Register will accept no further modifications. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the WRITE and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. While the PRDS instruction is being loaded, the PRE and PE pins must be held HIGH; then they become DON'T-CAREs.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 14.)

Figure A shows the status of the memory array regions as defined by the pointer address and the state of the program enable (PE) pin. In the first case, programming operations are enabled through the application of a logic "1" to the PE control pin. All memory locations beneath that of the pointer address are available for data changes. All memory locations at or above the pointer address are protected against data alteration and serve as read only memory.

In the second case, the PE pin is held in a logic "0" state. While this condition is present the XL93CS46-3 is protected against any data changes.

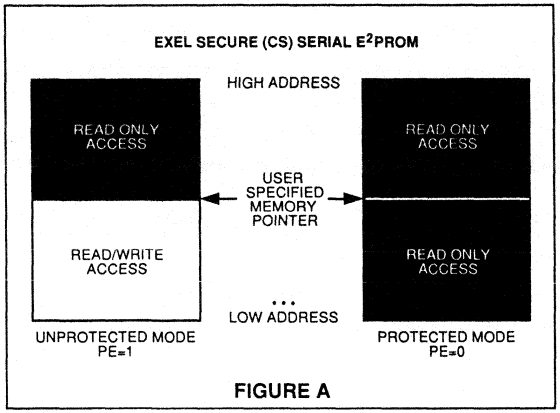


FIGURE A

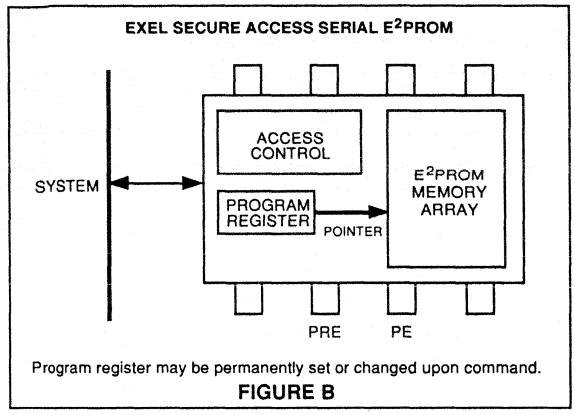


FIGURE B

The conceptual block diagram, Figure B, shows the simplicity with which the security features of the XL93CS46-3 may be managed.

The program register is accessed for read or write operations whenever the program register enable (PRE) pin is in a logic "1" state. Normal write operations to the program register establish the E^2 memory array address defining the region to be protected.

When PRE is in a logic "0" state, all read and write operations directed to the XL93CS46-3 affect the E^2PROM memory array locations.

Setting the address in the program register to the top of the XL93CS46-3 memory array renders the entire array to be writable. Setting the address to the bottom of the array

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93CS46-3 ..... 0°C to +70°C
XLE93CS46-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46-3 or -40°C to +85°C for the XLE93CS46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93CS46-3		XLE93CS46-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH}, SK = 250KHz		2		2	mA
I_{CC3}	Standby Current	PRE = CS = 0V DI = SK = PE = Vcc		3		3	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, PE and PRE	-15.0	15.0	-20.0	20.0	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc	0.8 Vcc		V
V_{OL1}	Output Low Voltage	I_{OL} = 1.0mA TTL		0.3		0.3	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46-3 or -40°C to +85°C for the XLE93CS46-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93CS46-3		XLE93CS46-3		Units
			Min	Max	Min	Max	
fSK	SK Clock Frequency		0	250	0	250	KHz
tSKH	SK High Time		1		1		µs
tSKL	SK Low Time		1		1		µs
tCS	Minimum CS Low Time		1		1		µs
tCSS	CS Setup Time	Relative to SK ⎍	200		200		ns
tPRES	PRE Setup Time	Relative to SK ⎍	200		200		ns
tPES	PE Setup Time	Relative to SK ⎍	200		200		ns
tDIS	DI Setup Time	Relative to SK ⎍	400		400		ns
tCSH	CS Hold Time	Relative to SK ⎎	0		0		ns
tPEH	PE Hold Time	Relative to CS ⎎	200		200		ns
tPREH	PRE Hold Time	Relative to CS ⎎	200		200		ns
tDIH	DI Hold Time	Relative to SK ⎍	400		400		ns
tPD1	Output Delay to "1"	AC Test		2		2	µs
tPD0	Output Delay to "0"	AC Test		2		2	µs
tSV	CS to Status Valid	AC Test		2		2	µs
tDF	CS to DO in 3-state	CS = VIL		400		400	ns
tWP	Write Cycle Time			25		25	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
CIN	Input Capacitance	5	pF
COUT	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

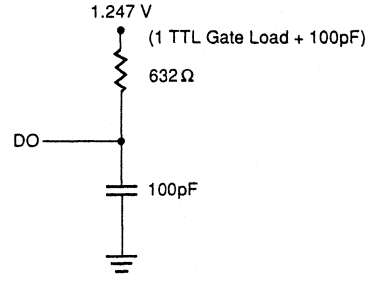


FIGURE 1. AC TEST CONDITIONS

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46-3 or -40°C to +85°C for the XLE93CS46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93CS46-3		XLE93CS46-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, PE and PRE	-20.0	20.0	-20.0	20.0	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93CS46-3 or -40°C to +85°C for the XLE93CS46-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93CS46-3		XLE93CS46-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		400		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		50		ns
t_{PRES}	PRE Setup Time	Relative to SK ⌐	50		50		ns
t_{PES}	PE Setup Time	Relative to SK ⌐	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{PEH}	PE Hold Time	Relative to CS ¬	50		50		ns
t_{PREH}	PRE Hold Time	Relative to CS ¬	50		50		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L= 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

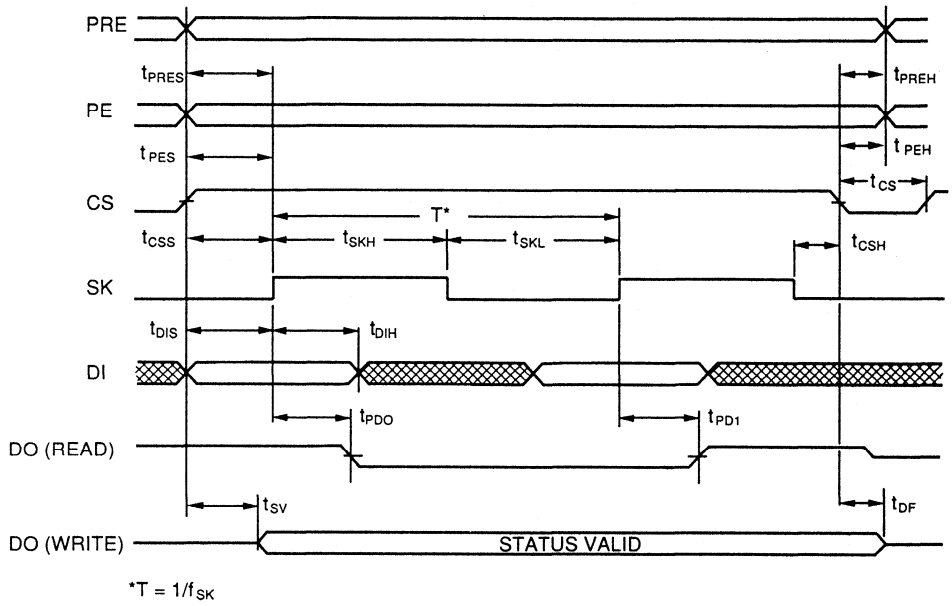
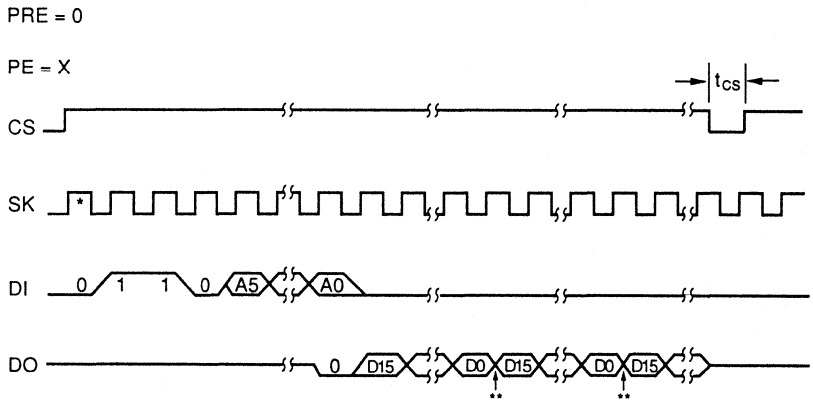


FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
**Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING

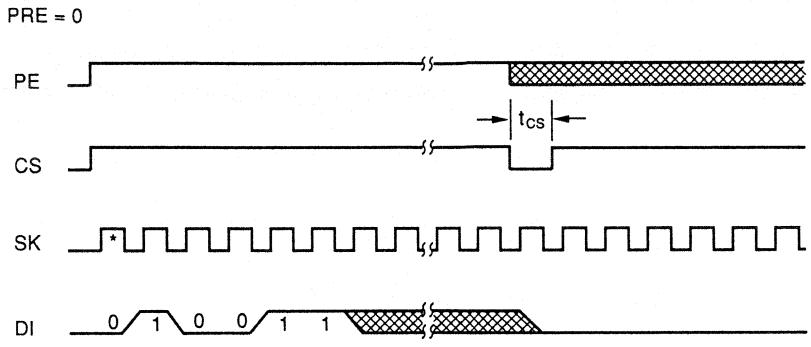


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

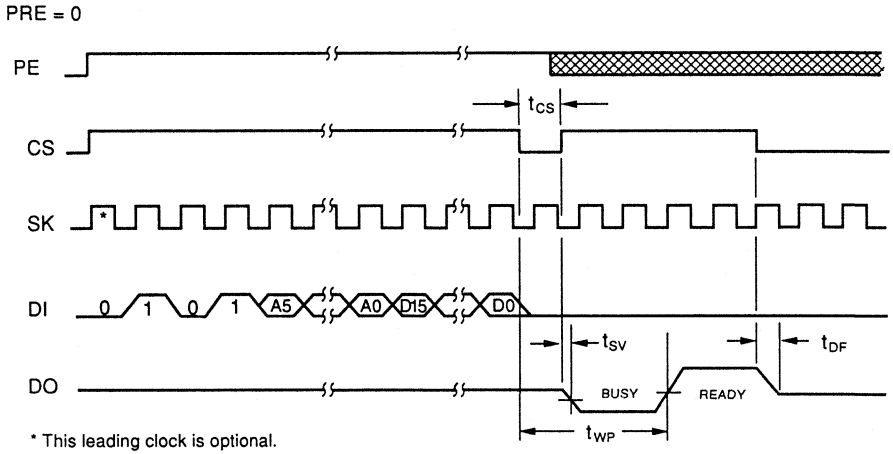


FIGURE 5. WRITE CYCLE TIMING

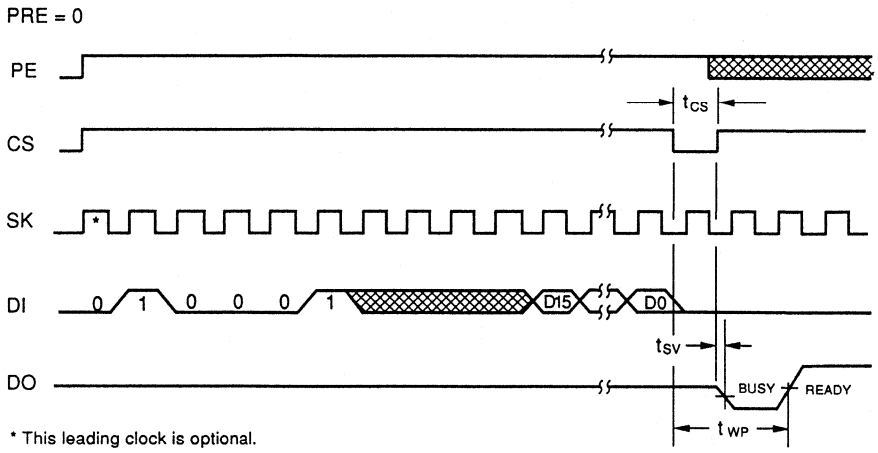


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

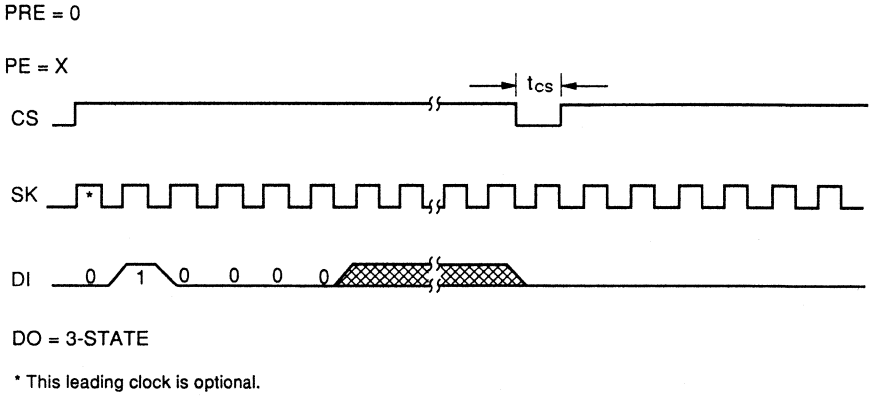


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

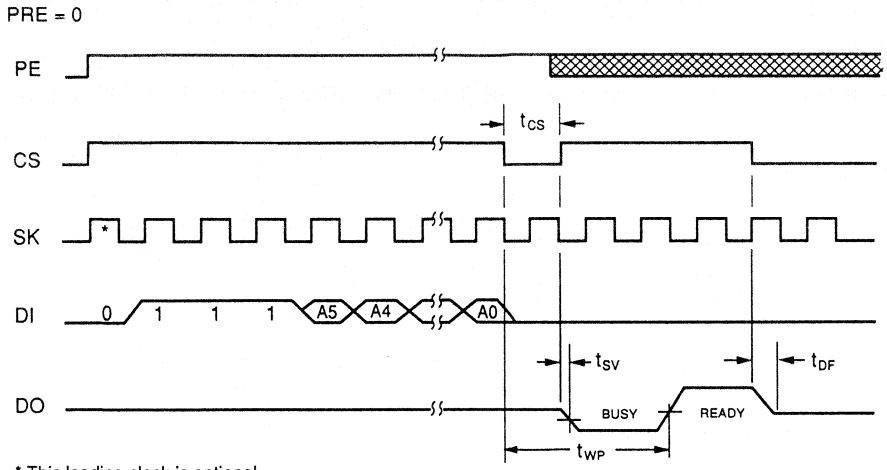


FIGURE 8. ERASE (REGISTER) CYCLE TIMING

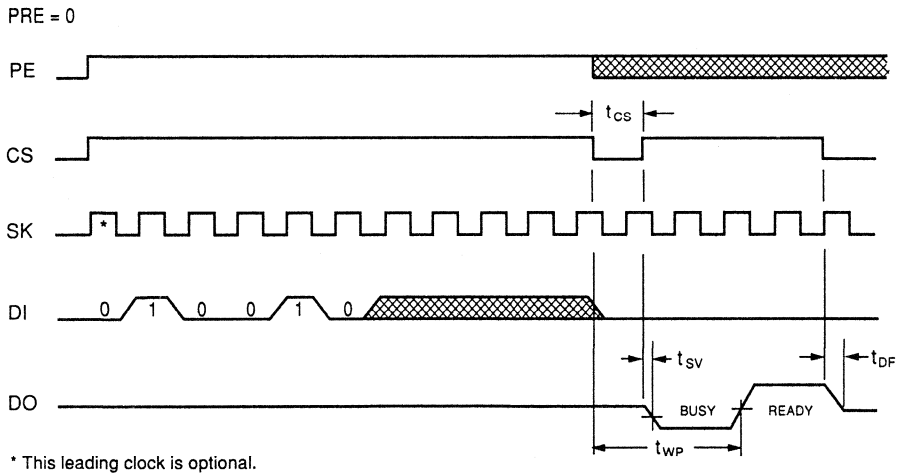
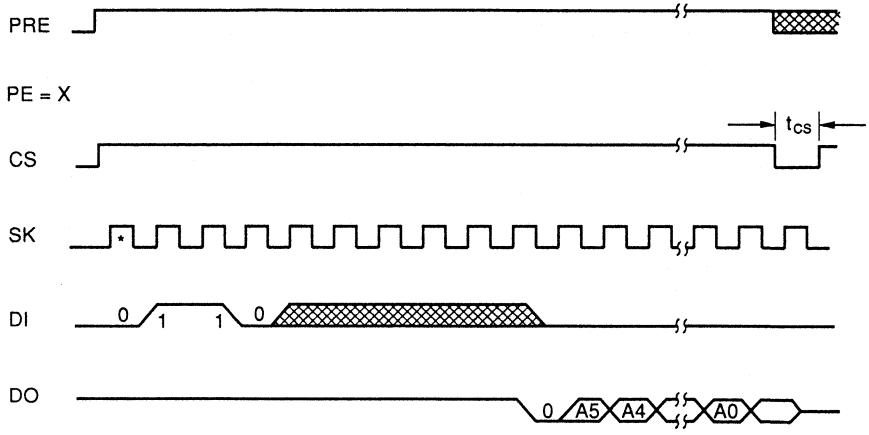
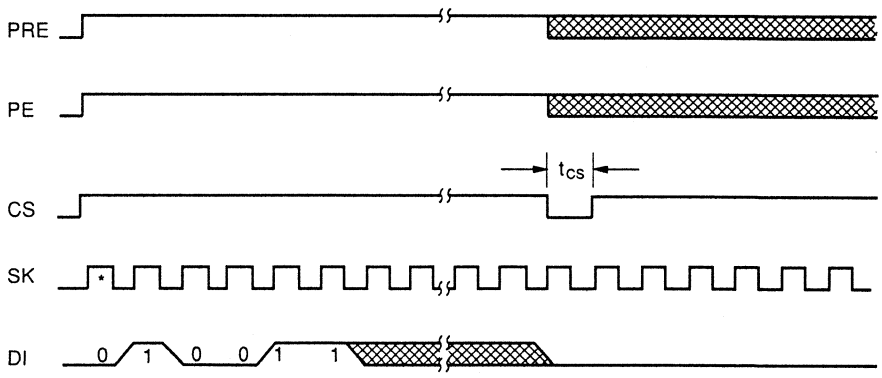


FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING



* This leading clock is optional.

FIGURE 10. PROTECT REGISTER READ (PRREAD) CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 11. PROTECT REGISTER ENABLE (PREN) CYCLE TIMING

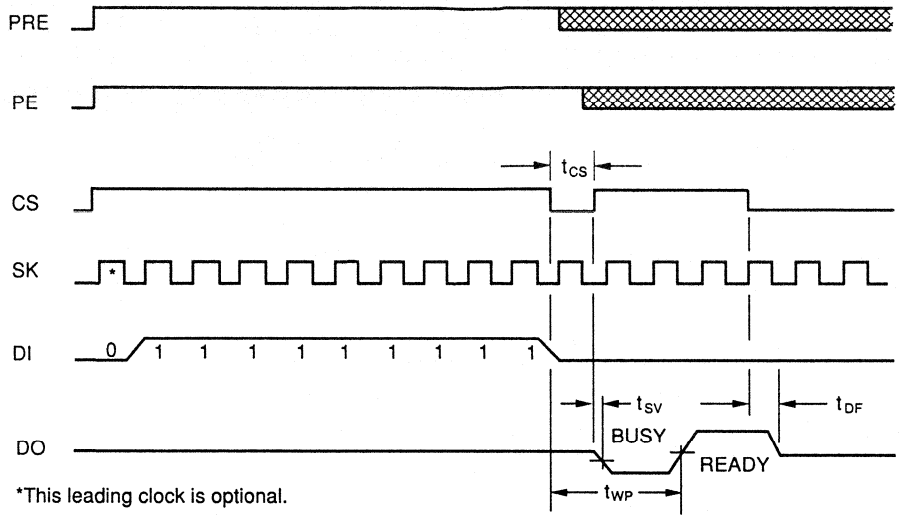


FIGURE 12. PROTECT REGISTER CLEAR (PRCLEAR) CYCLE TIMING

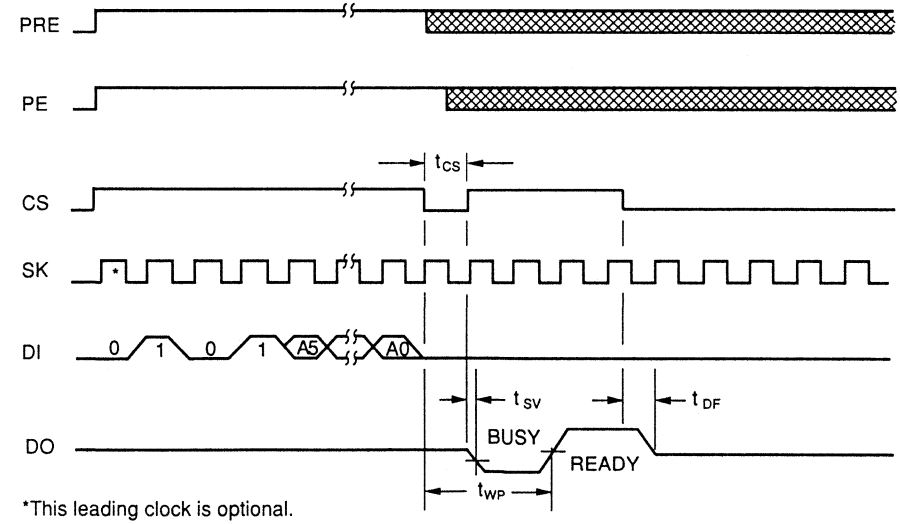


FIGURE 13. PROTECT REGISTER WRITE (PRWRITE) CYCLE TIMING

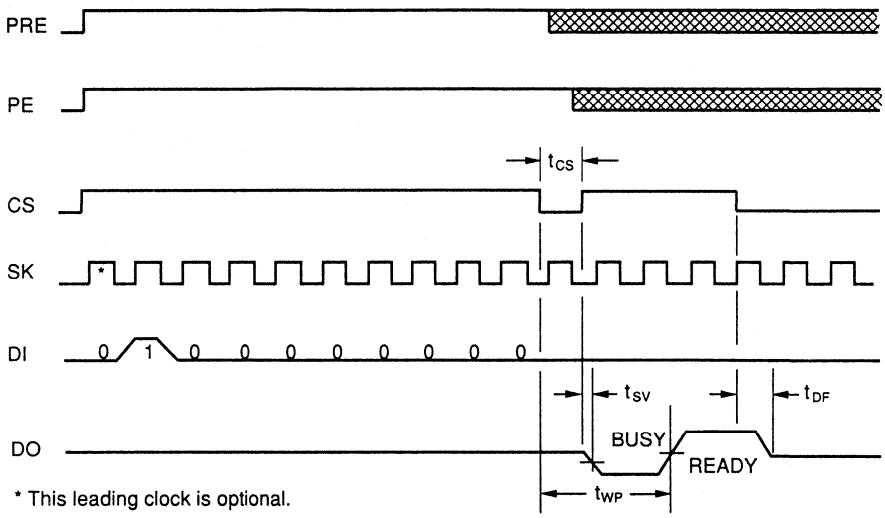


FIGURE 14. PROTECT REGISTER DISABLE (PRDS) CYCLE TIMING

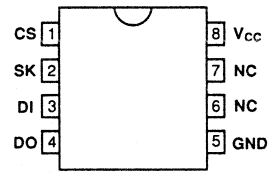
2,048-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

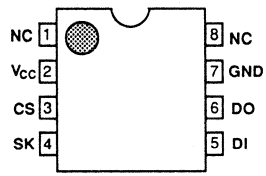
- **State-of-the-Art Architecture**
  - — Nonvolatile data storage
  - — Single supply - 5V operation
  - — Fully TTL compatible inputs and outputs
  - — Auto increment for efficient data dump
  - — 1MHz operation
- **Hardware and Software Write Protection**
  - — Defaults to write-disabled state at power up
  - — Software instructions for write-enable/disable
  - — V_{CC} lockout inadvertent write protection
- **Low Power Consumption**
  - — 1mA active (typical)
  - — 1µA standby (typical)
- **Low Voltage Read Operations**
  - — Reliable read operations down to 2.0 volts
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - — Self-timed programming cycle
  - — Automatic erase-before-write
  - — Programming Status Indicator
  - — Word and chip erasable
- **Durable and Reliable**
  - — 10-year data retention after 100K write cycles
  - — Minimum of 100,000 write cycles per word
  - — Unlimited read cycles
  - — ESD protection

PIN CONFIGURATIONS

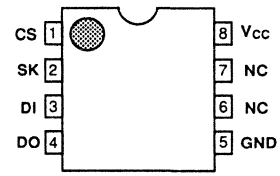
Plastic Dual-in-line
"P" Package



EIAJ Small Outline
"J" Package



EIAJ Small Outline
"JR" Package



PIN NAMES

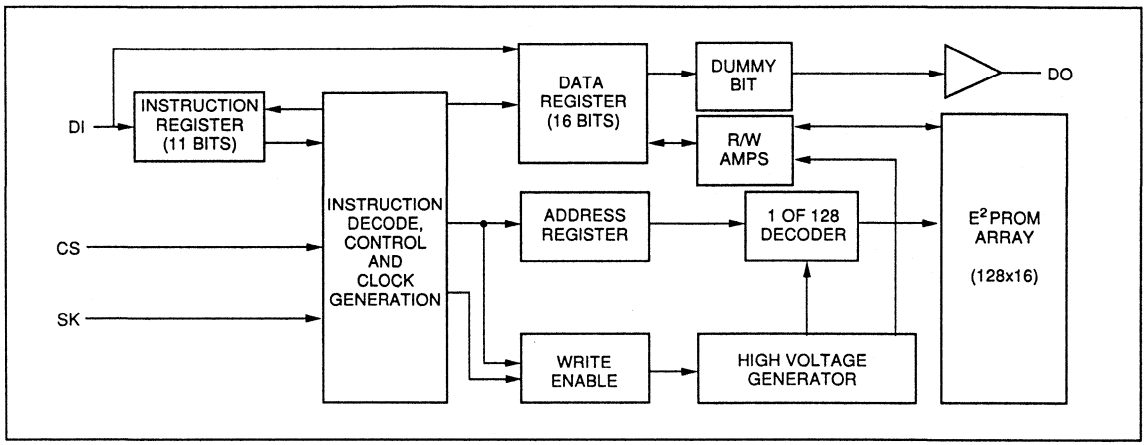
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC56 is a low cost 2,048-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC56 provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC56 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC56 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC56 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC56 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC56 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC56 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5V, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC56 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC56 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC56 is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A_6-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A_6-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A_6-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC56 ..... 0°C to +70°C
XLE93LC56 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56 or -40°C to +85°C for the XLE93LC56

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4			V

AC ELECTRICAL CHARACTERISTICS

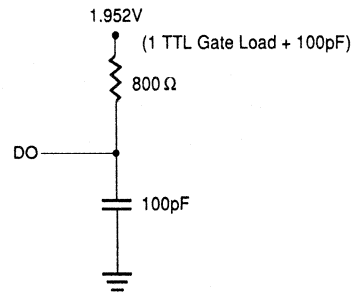
T_A = 0°C to +70°C for the XLS93LC56 or -40°C to +85°C for the XLE93LC56

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌜	50		100		ns
t_{DIS}	DI Setup Time	Relative to SK ⌜	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⌞	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌜	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10			ms

CAPACITANCE

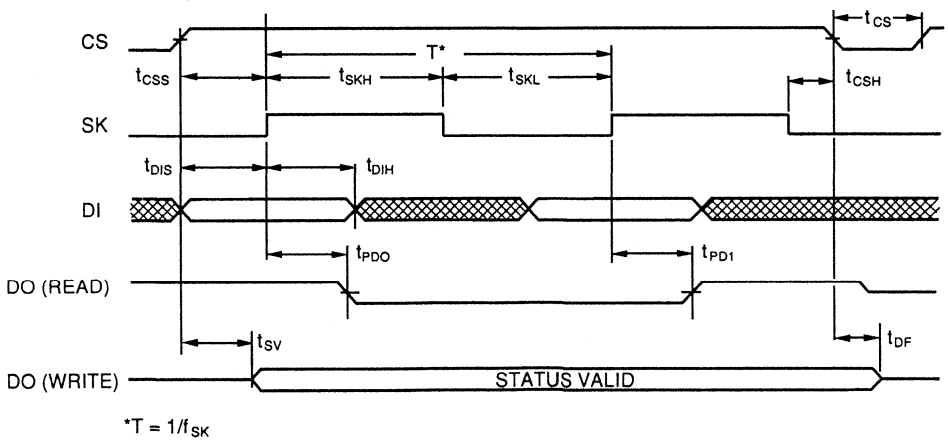
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



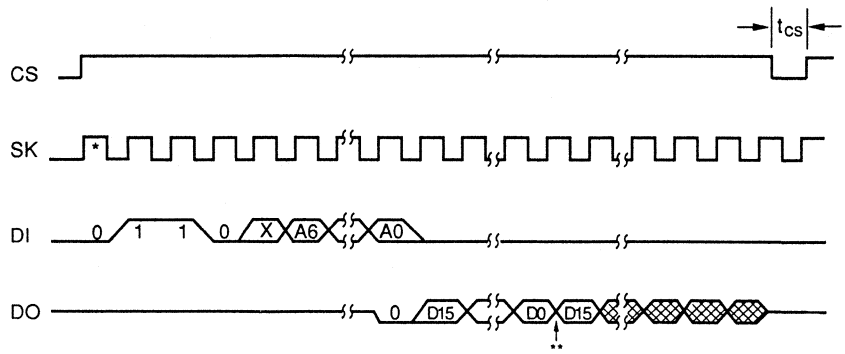
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST LOAD CONDITIONS



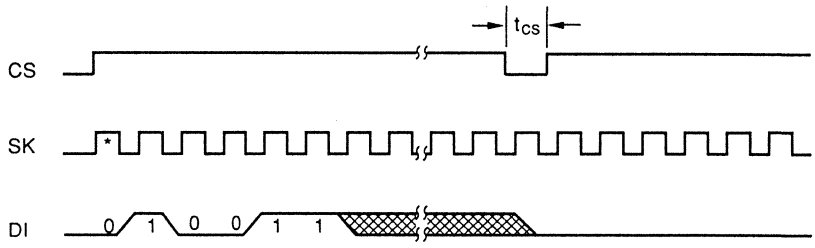
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

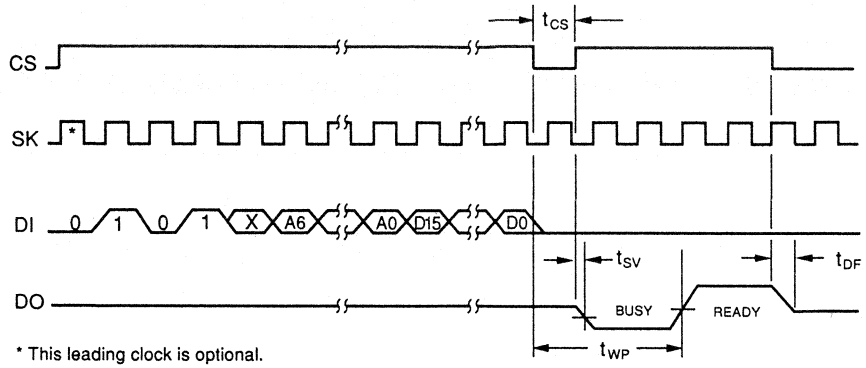


FIGURE 5. WRITE CYCLE TIMING

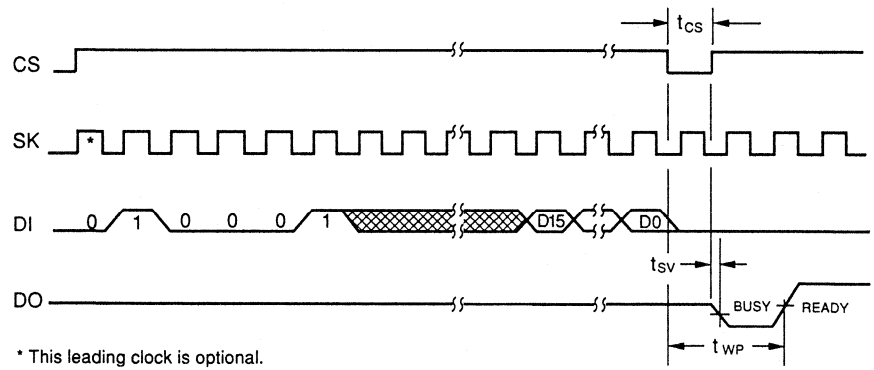
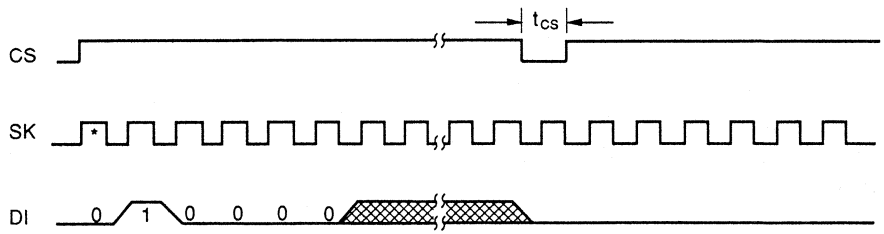


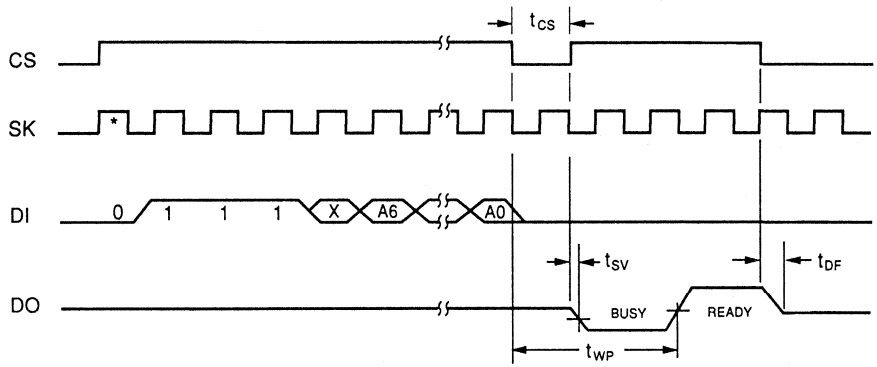
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

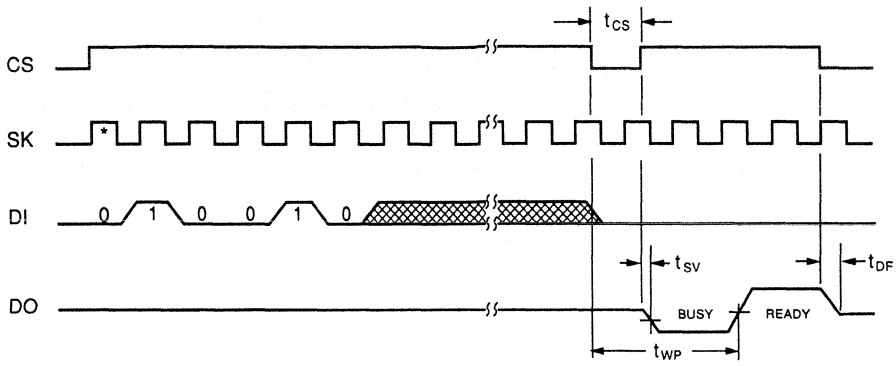
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

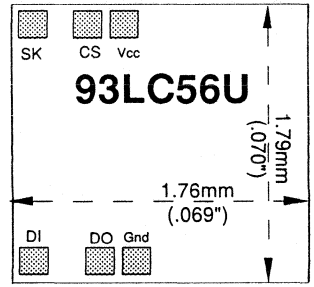
Preliminary

2,048-Bit Serial Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

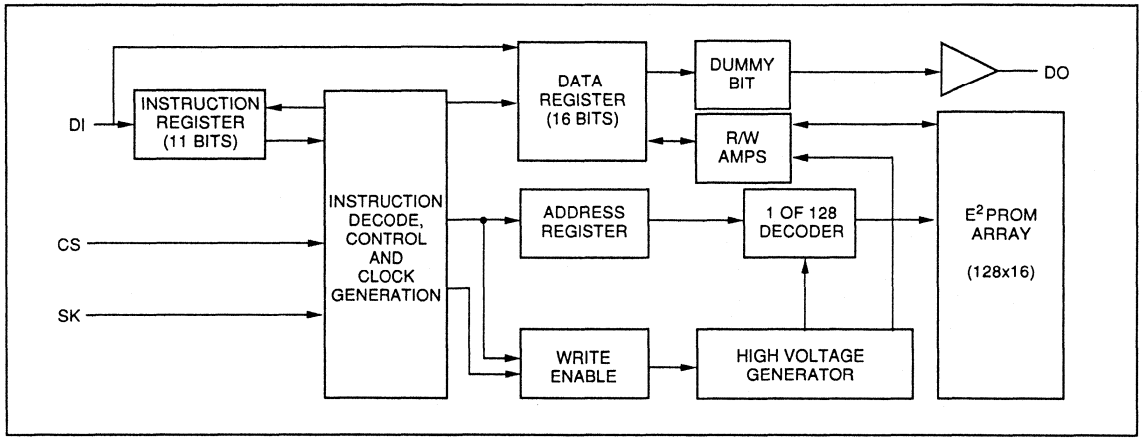
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC56U is a low cost 2,048-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC56U provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC56U dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC56U is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC56U is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC56U is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC56U will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC56U has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC56U is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5V, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC56U has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{BUSY}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{BUSY}$ flag. Therefore, it is important if you want to access the READY/$\overline{BUSY}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pad indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC56U has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC56U is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A_6-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A_6-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A_6-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC56U ..... 0°C to +70°C
XLE93LC56U ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U or -40°C to +85°C for the XLE93LC56U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4	n/a	n/a	V

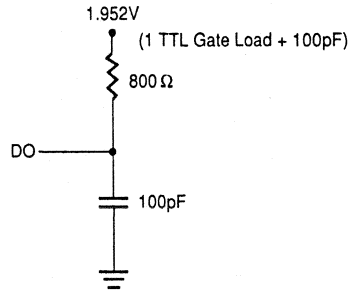
AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U or -40°C to +85°C for the XLE93LC56U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		100		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⌙	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10	n/a	n/a	ms

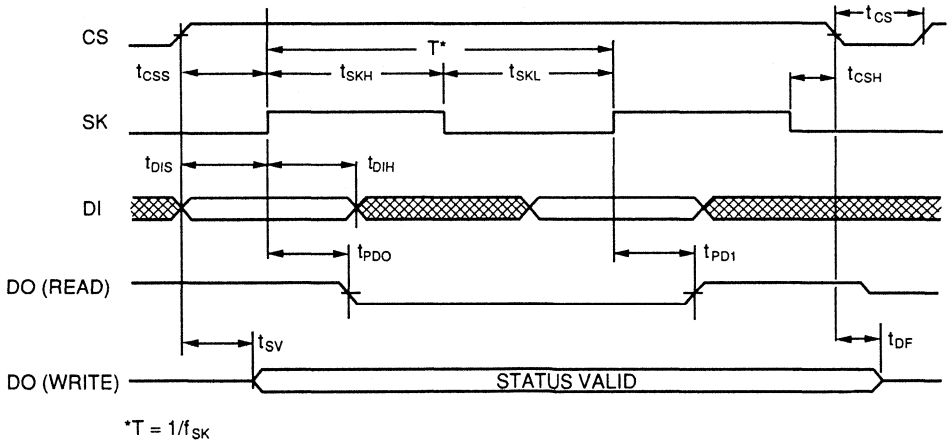
CAPACITANCE
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



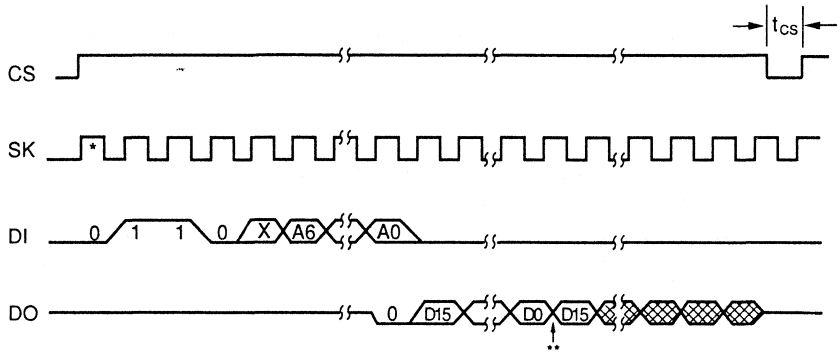
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST LOAD CONDITIONS



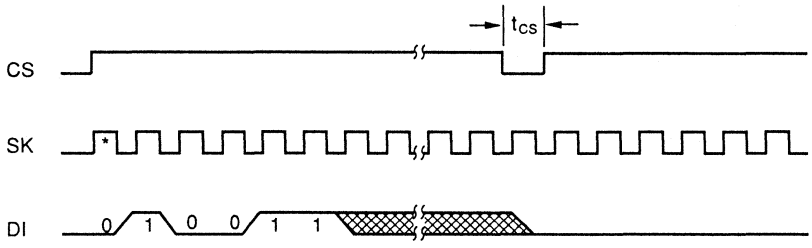
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

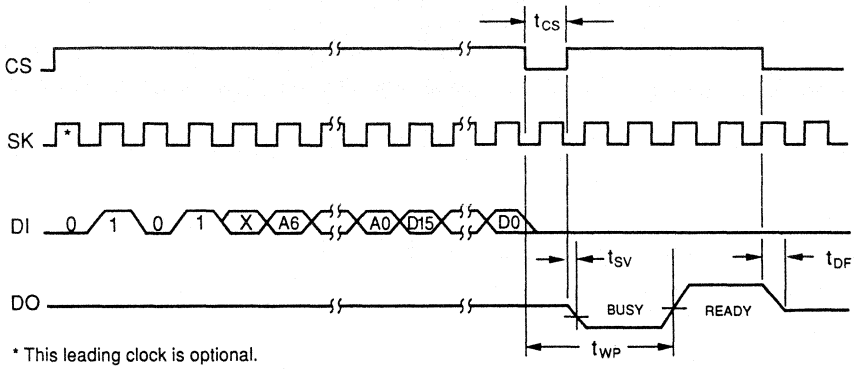


FIGURE 5. WRITE CYCLE TIMING

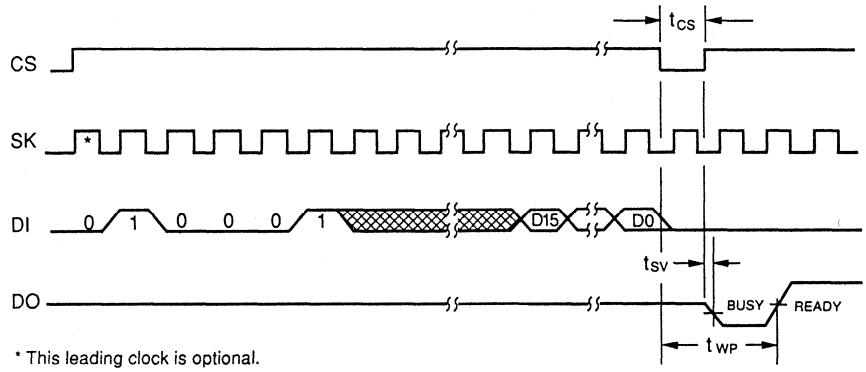


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

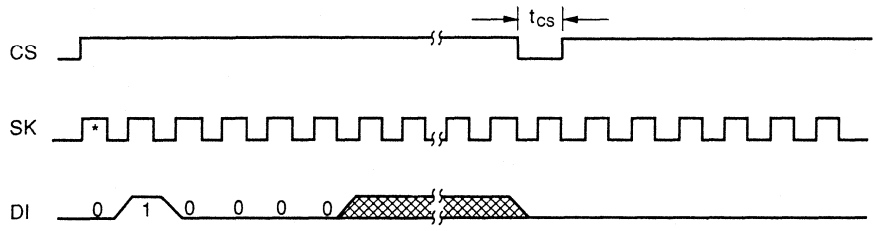


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

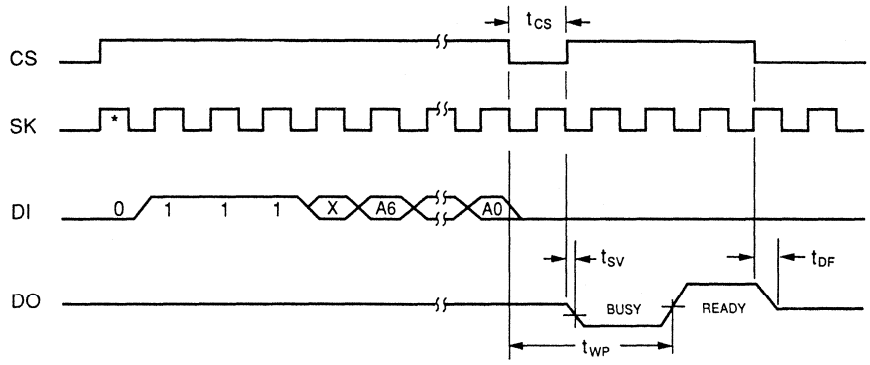
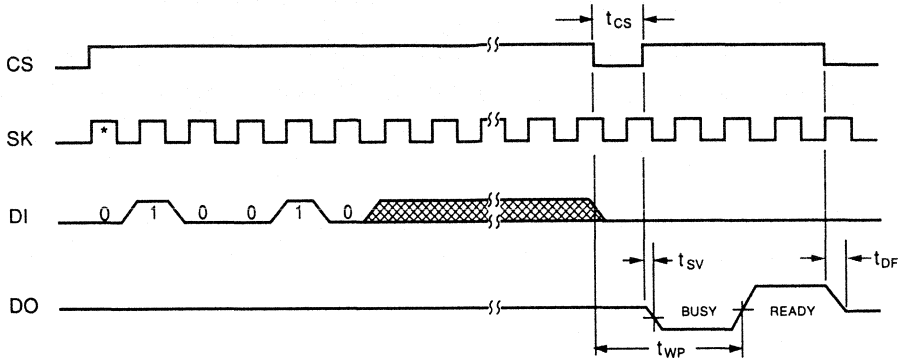


FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

XL93LC56-3

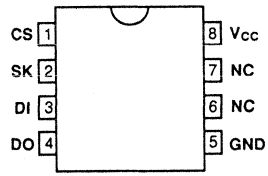
2,048-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

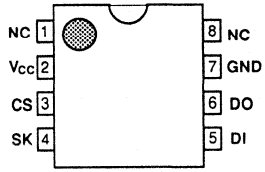
- **State-of-the-Art Architecture**
  - — Nonvolatile data storage
  - — 3V to 5V operation
  - — Fully TTL compatible inputs and outputs
  - — Auto increment for efficient data dump
- **Hardware and Software Write Protection**
  - — Defaults to write-disabled state at power up
  - — Software instructions for write-enable/disable
- **Low Power Consumption**
  - — 1mA active (typical)
  - — 1µA standby (typical)
- **Low Voltage Read Operations**
  - — Reliable read operations down to 2.0 volts
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - — Self-timed programming cycle
  - — Automatic erase-before-write
  - — Programming Status Indicator
  - — Word and chip erasable
- **Durable and Reliable**
  - — 10-year data retention after 100K write cycles
  - — Minimum of 100,000 write cycles per word
  - — Unlimited read cycles
  - — ESD protection

PIN CONFIGURATIONS

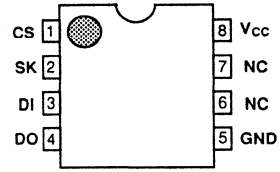
Plastic Dual-In-line "P" Package



EIAJ Small Outline "J" Package



EIAJ Small Outline "JR" Package



PIN NAMES

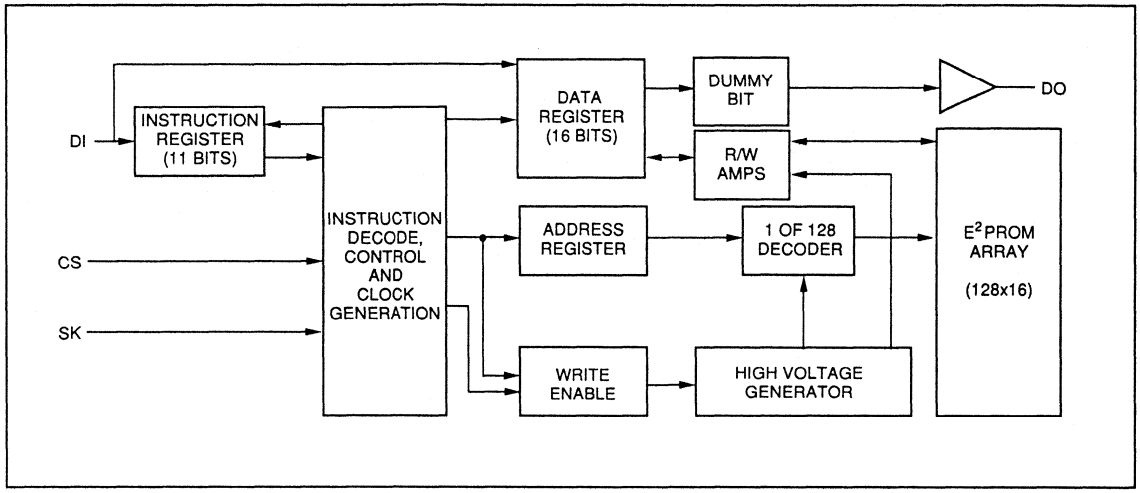
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC56-3 is a low cost 2,048-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC56-3 provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC56-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC56-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC56-3 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC56-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC56-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC56-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** $V_{IL} = 0.1\ V_{CC}$ min., $V_{IH} = 0.9\ V_{CC}$ min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC56-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{BUSY}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{BUSY}$ flag. Therefore, it is important if you want to access the READY/$\overline{BUSY}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A_6-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A_6-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A_6-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC56-3 ..... 0°C to +70°C
XLE93LC56-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56-3 or -40°C to +85°C for the XLE93LC56-3, V_{CC} = 3.0V ±10%

Symbol	Parameter	Conditions	XLS93LC56-3		XLE93LC56-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56-3 or -40°C to +85°C for the XLE93LC56-3, V_{CC} = 3.0V ±10%

Symbol	Parameter	Conditions	XLS93LC56-3		XLE93LC56-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56-3 or -40°C to +85°C for the XLE93LC56-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC56-3		XLE93LC56-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{CC}, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56-3 or -40°C to +85°C for the XLE93LC56-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC56-3		XLE93LC56-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⎍	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⎍	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ⎏	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⎍	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

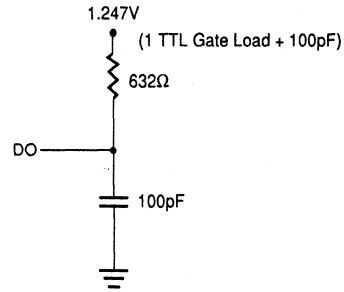
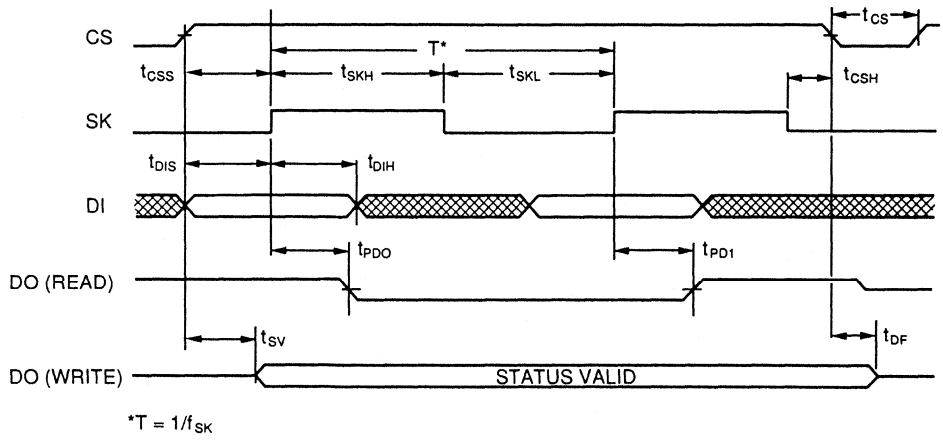
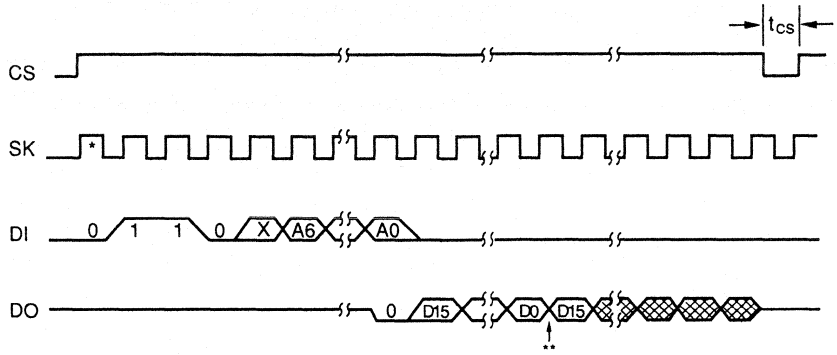


FIGURE 1. AC TEST CONDITIONS



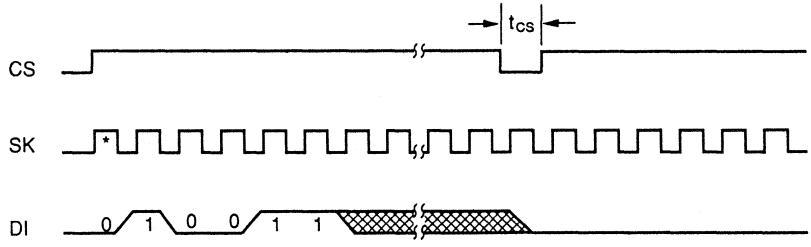
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

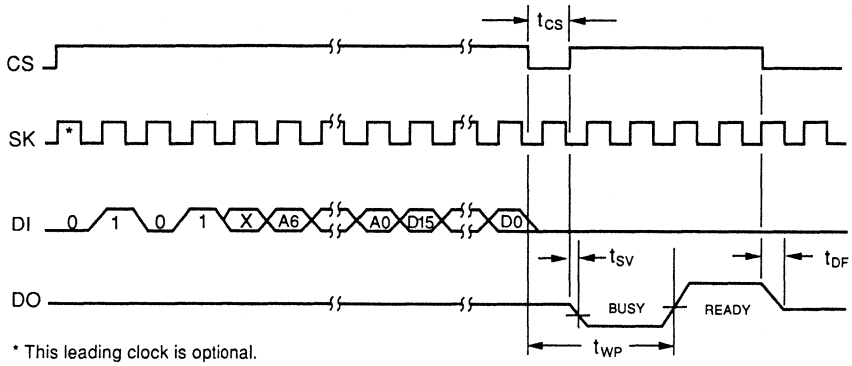


FIGURE 5. WRITE CYCLE TIMING

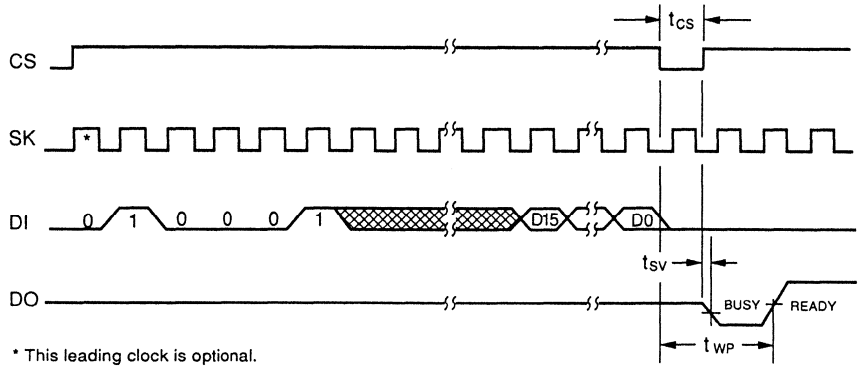
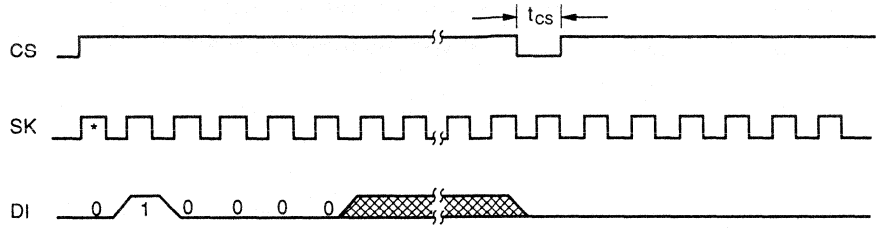


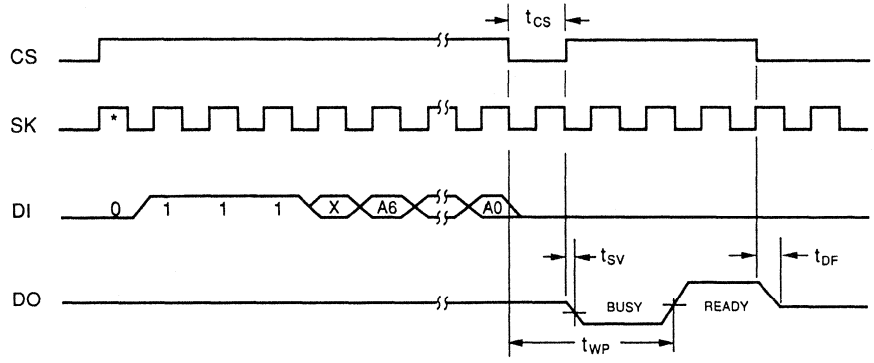
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

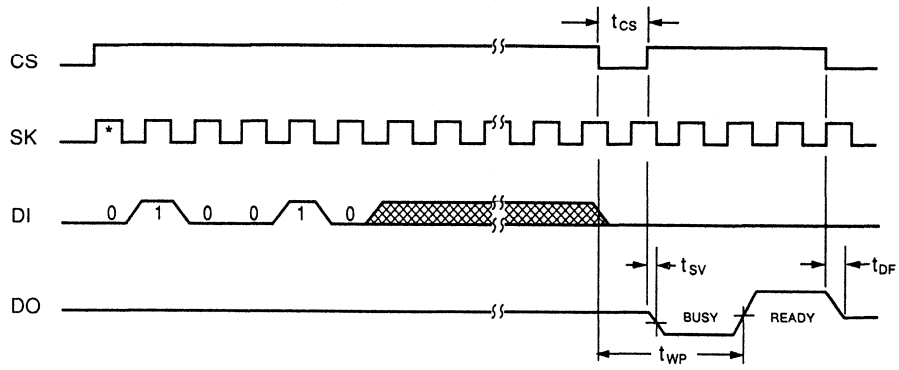
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

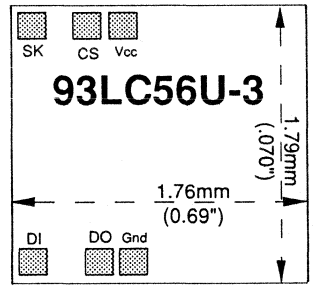
Preliminary

2,048-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

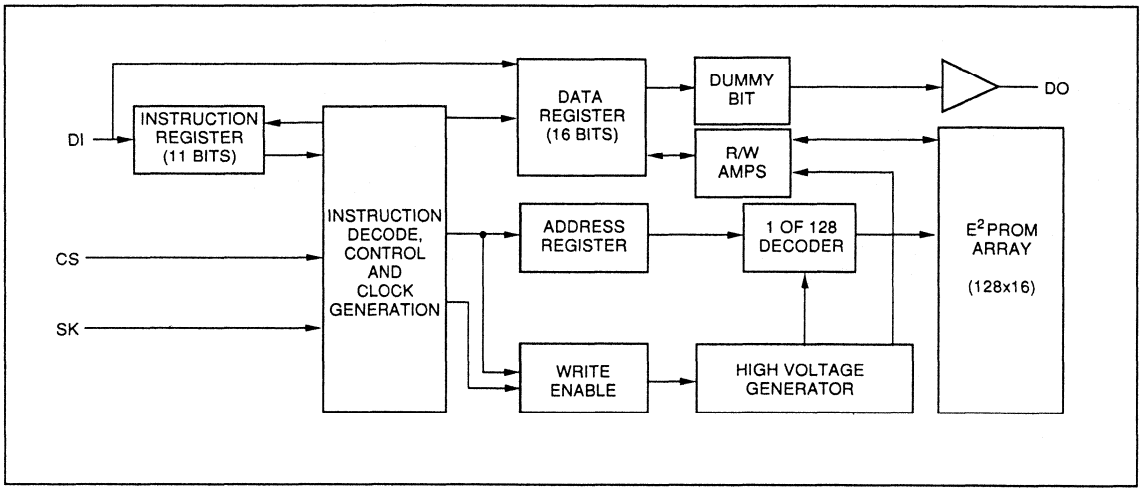
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC56U-3 is a low cost 2,048-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC56U-3 provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC56U-3 dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC56U-3 is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC56U-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC56U-3 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC56U-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC56U-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC56U-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** $V_{IL} = 0.1\ V_{CC}$ min., $V_{IH} = 0.9\ V_{CC}$ min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC56U-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pad indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	X(A_6-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	X(A_6-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	X(A_6-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC56U-3 ..... 0°C to +70°C
XLE93LC56U-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U-3 or -40°C to +85°C for the XLE93LC56U-3, V_{CC} = 3.0V ±10%

Symbol	Parameter	Conditions	XLS93LC56U-3		XLE93LC56U-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U-3 or -40°C to +85°C for the XLE93LC56U-3, V_{CC} = 3.0V ±10%

Symbol	Parameter	Conditions	XLS93LC56U-3		XLE93LC56U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U-3 or -40°C to +85°C for the XLE93LC56U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC56U-3		XLE93LC56U-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC56U-3 or -40°C to +85°C for the XLE93LC56U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC56U-3		XLE93LC56U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

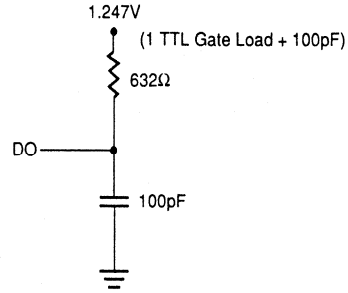
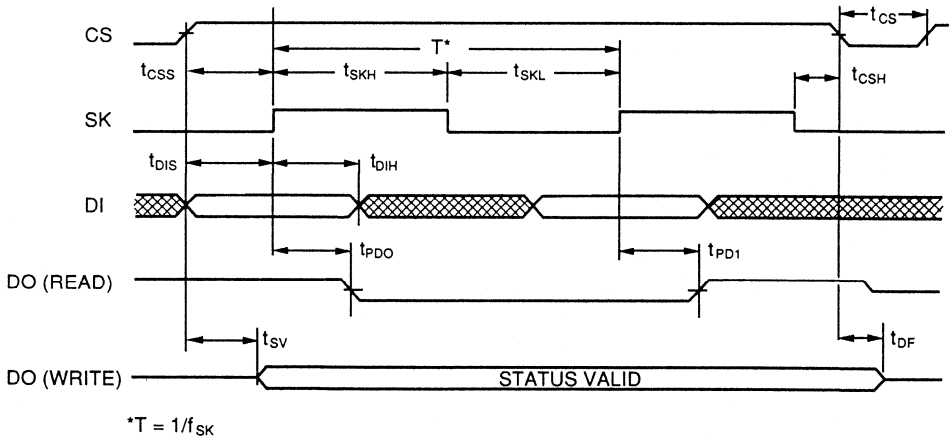
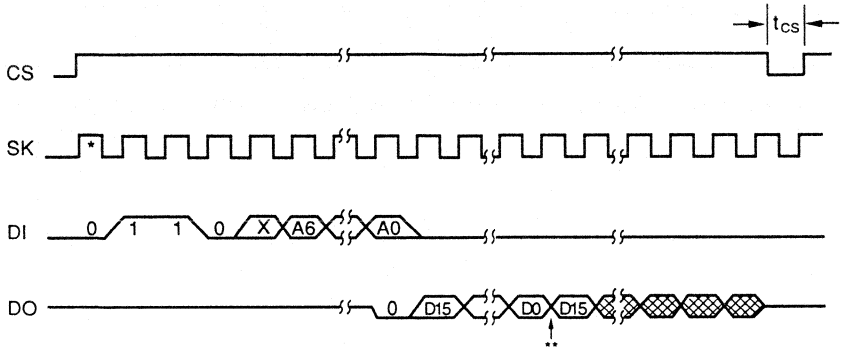


FIGURE 1. AC TEST CONDITIONS



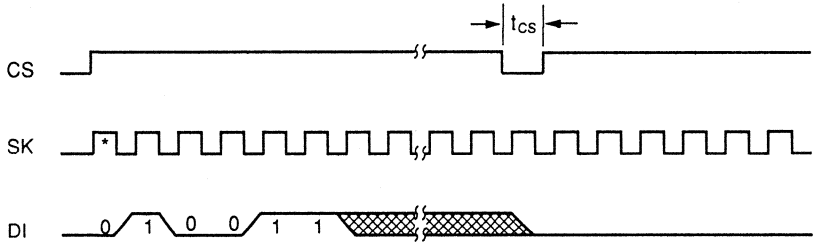
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



* This leading clock is optional.
** Address pointer automatically cycles to the next register.

FIGURE 3. READ CYCLE TIMING



DO = 3-state

* This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

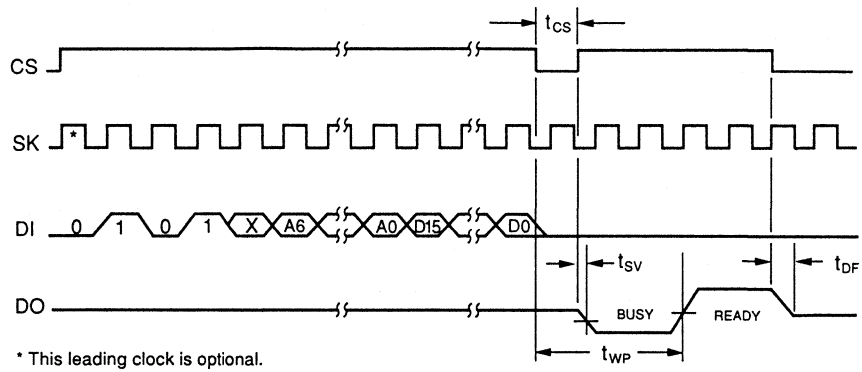


FIGURE 5. WRITE CYCLE TIMING

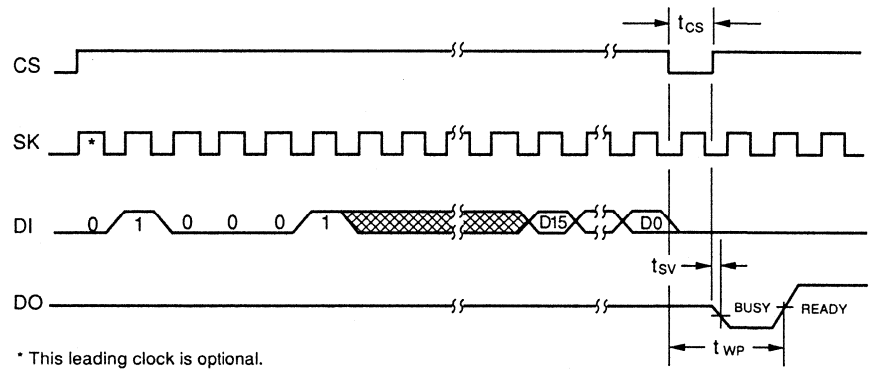
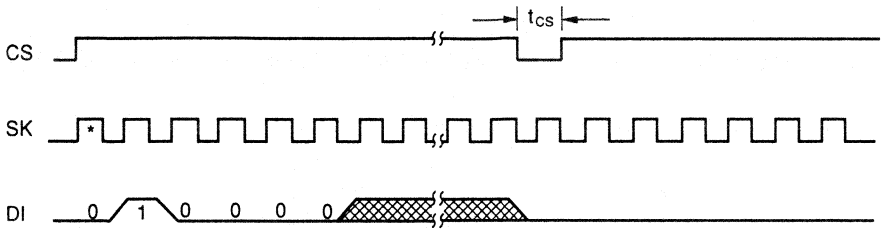


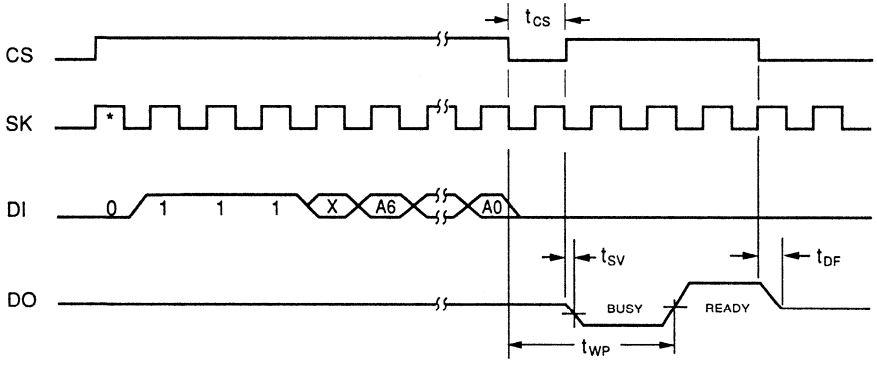
FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



DO = 3-STATE

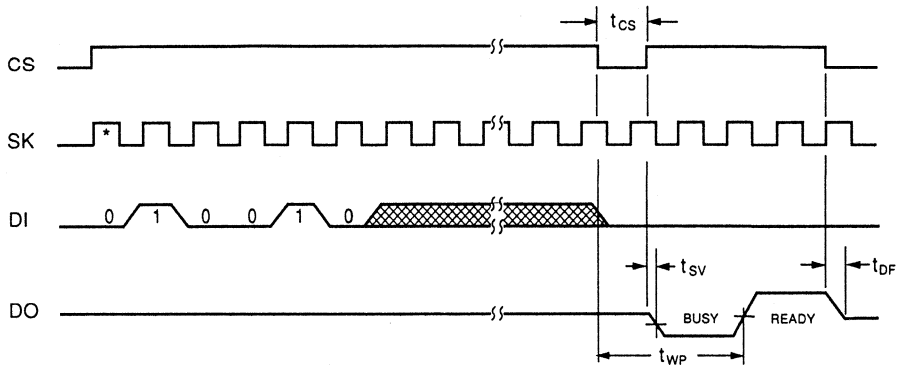
* This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



* This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



* This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

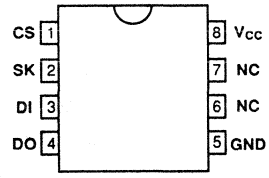
2048-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

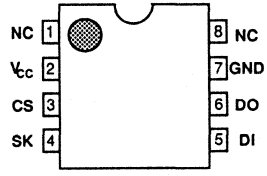
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

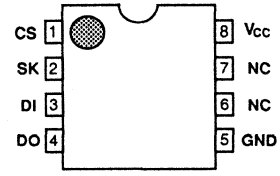
Plastic Dual-In-line
"P" Package



EIAJ Small Outline
"J" Package



EIAJ Small Outline
"JR" Package



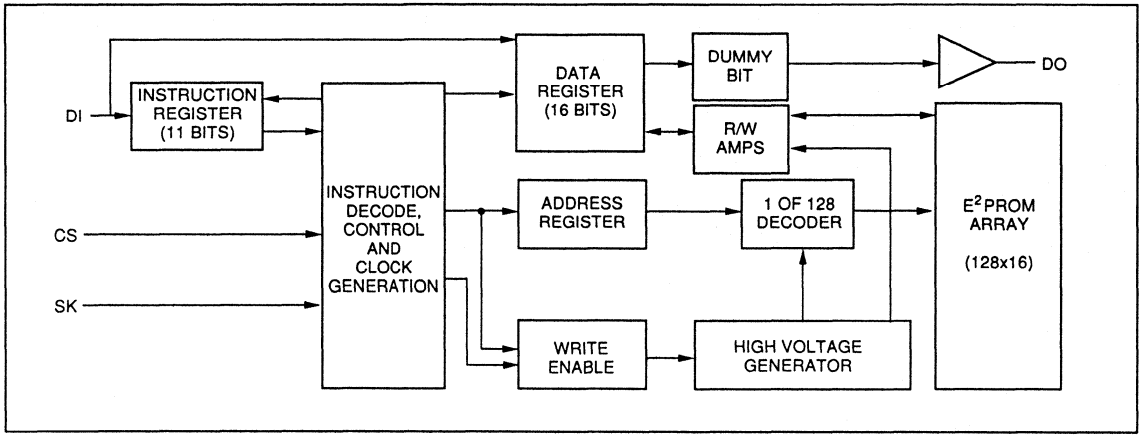
OVERVIEW

The XL93C56 is a low cost 2048-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93C56 provides efficient nonvolatile read/write memory arranged as 128 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

BLOCK DIAGRAM



APPLICATIONS

The XL93C56 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93C56 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93C56 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93C56 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93C56 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93C56 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)

The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. The ERAL operation is required before WRAL operation. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/BUSY status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address	Input Data
READ	01	10	X(A_6-A_0)	
WEN (Write Enable)	01	00	11XXXXXX	
WRITE	01	01	X(A_6-A_0)	D_{15}-D_0
WRALL (Write All Registers)	01	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	01	00	00XXXXXX	
ERASE	01	11	X(A_6-A_0)	
ERAL (Erase All Registers)	01	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93C56 ..... 0°C to +70°C
XLE93C56 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C56 or -40°C to +85°C for the XLE93C56

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz @ 5V SK = 250KHz @ 2V		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz @ 5V SK = 250KHz @ 2V		5		5	mA
I_{SB}	Standby Current (CMOS)	CS = DI = SK =0V		4		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V

AC ELECTRICAL CHARACTERISTICS

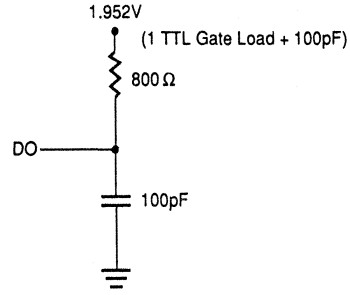
T_A = 0°C to +70°C for the XLS93C56 or -40°C to +85°C for the XLE93C56

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time		250		2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		n/a	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS

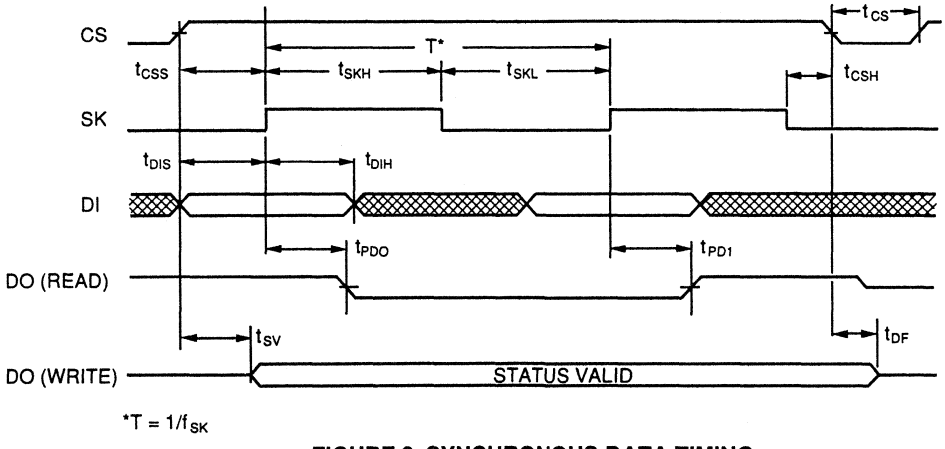


FIGURE 2. SYNCHRONOUS DATA TIMING

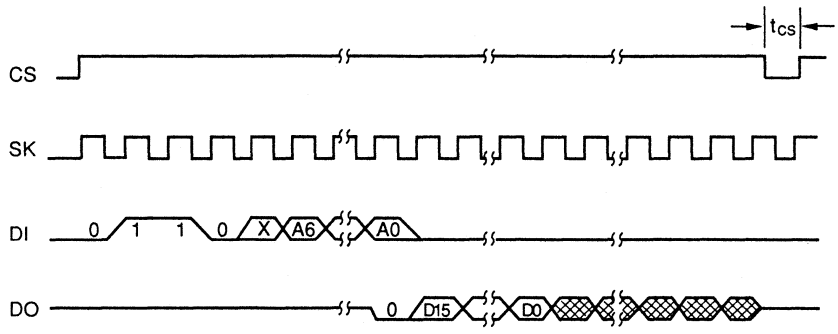


FIGURE 3. READ CYCLE TIMING

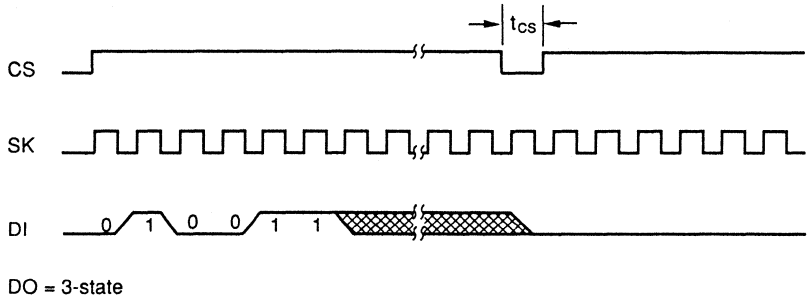


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

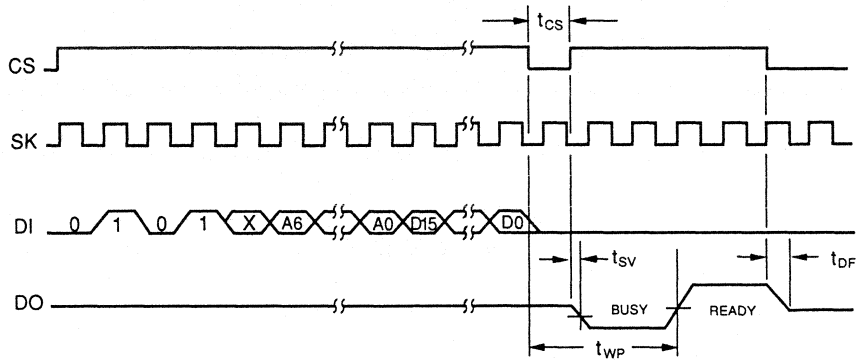


FIGURE 5. WRITE CYCLE TIMING

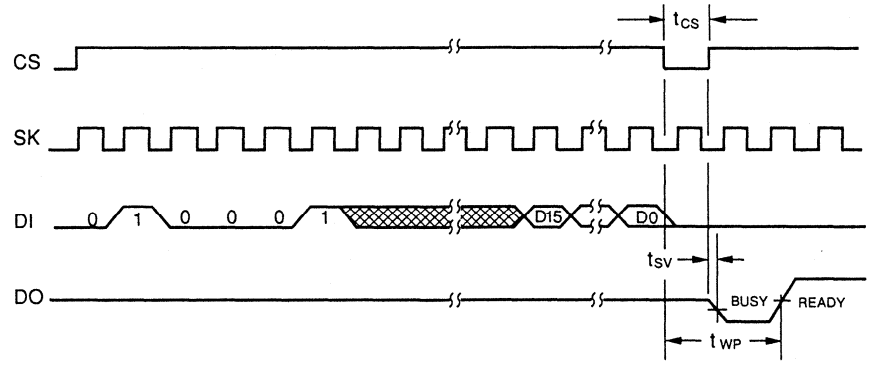


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

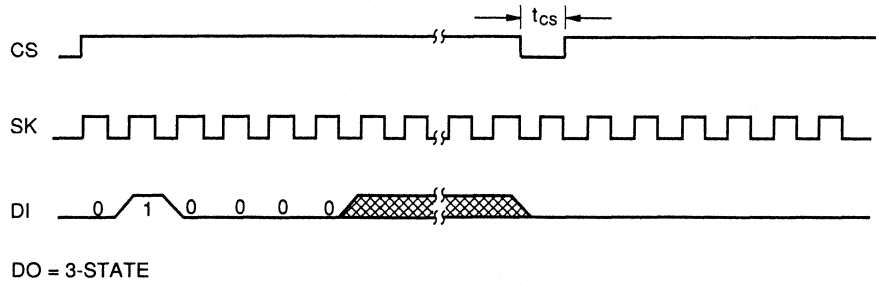


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

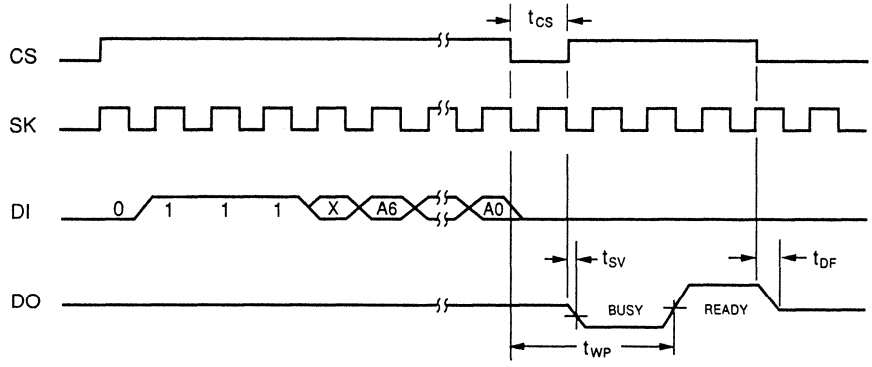


FIGURE 8. ERASE (REGISTER) CYCLE TIMING

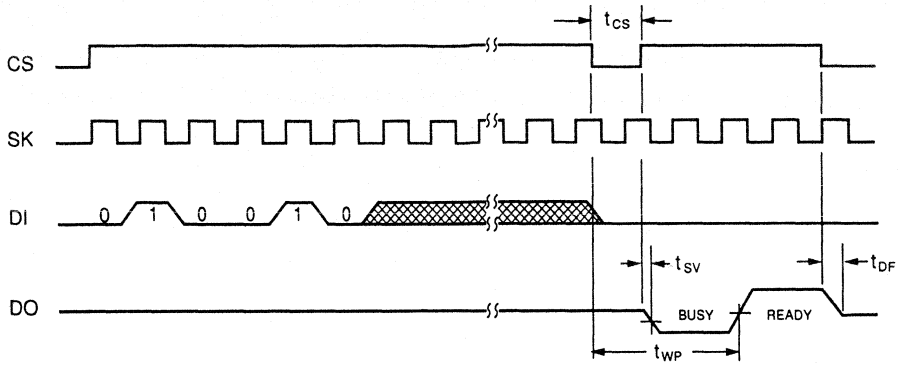


FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

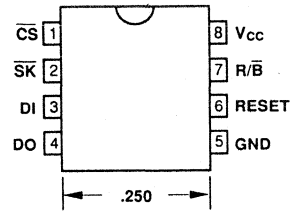
2048-Bit Serial (5V) Electrically Erasable PROM

FEATURES

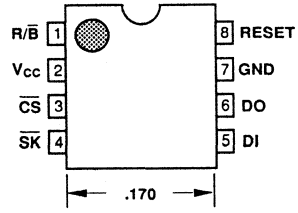
- **2048-bit Serial Architecture**
  - —128 registers, 16 bits each
  - —Nonvolatile data storage
  - —Single 5V supply
- **Versatile, Easy-to-Use Interface**
  - —READY/$\overline{\text{BUSY}}$ status signal
  - —Automatic write cycle time-out
  - —Software controlled write protection
- **Advanced CMOS E²PROM Technology**
- **Low Power Consumption**
  - —3mA max. active
  - —1mA max. standby, TTL
  - —25μA max. standby CMOS
- **Up to 10,000 Erase/Write Cycles Per Register**
- **10 Year Data Retention**

PIN CONFIGURATIONS

Plastic Dual-in-line "P" Package



EIAJ Small Outline "J" Package



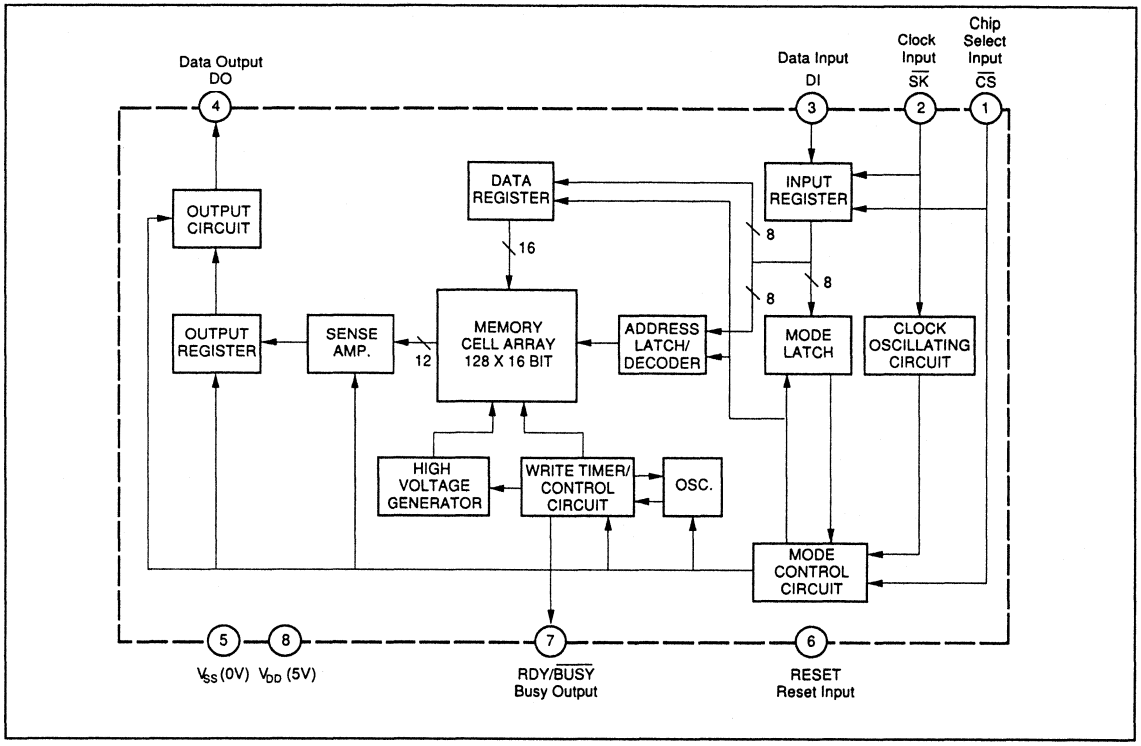
PIN NAMES

$\overline{\text{CS}}$	Chip Select
$\overline{\text{SK}}$	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
RESET	Reset Input
R/$\overline{\text{B}}$	READY/$\overline{\text{BUSY}}$ Output
Vcc	Power Supply

OVERVIEW

The XL90C21 is a 2048-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL90C21 provides external read/write memory arranged as 128 registers of 16 bits each. Five 8-bit instructions control the operation of the device, which include read, write, enable and status functions. The XL90C21 has been designed for applications requiring up to 10,000 erase/write cycles per register. In the standby mode, the XL90C21 reduces power consumption by more than 80%, compared to an NMOS counterpart.

BLOCK DIAGRAM



APPLICATIONS

The XL90C21 is ideal for high volume applications requiring low density data storage. It uses a low cost, space saving 8-pin package, and readily interfaces with standard microprocessors and popular microcontrollers such as the 8048/49/51/96, the COP4XX series, the 6801/05, the TMS1000 and the Z8.

Candidate applications include alarm devices, appliances, computer terminals and smart cards, electronic locks, meters, robotics and telephone, to name just a few.

ENDURANCE AND DATA RETENTION

The XL90C21 is designed for applications requiring up to 10,000 write cycles per bit. It provides 10 years of secure data retention, with or without power applied.

DEVICE OPERATION

The XL90C21 is a clocked serial port compatible E²PROM. Input data is latched on the rising edge of the clock, and data is output on the falling edge of the clock.

Data is grouped in 8-bit bytes. The beginning 8 bits specify the mode, the next 8 bits specify the address, and subsequent 16 bits specify the I/O data.

During the self-timed internal programming cycle that accompanies a write, the $\overline{SK}$ clock is de-activated. It is needed only when instructions or data are being passed to or from the memory.

Any of the six modes (read, write, write enable, write disable, erase all and write all) may be specified. The write time is set by internal timer, and determination of whether a write operation is in progress or not can be made from the status of the READY/$\overline{BUSY}$ pin. When the asynchronous RESET pin is taken HIGH, any ongoing operation is immediately halted.

Read (READ)
The read instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into the output register. The output on DO changes during the HIGH to LOW transition of $\overline{SK}$.

Write (WRITE)
After a write instruction and its address have been decoded, the device expects 16 bits of data. These are to be transferred into the specific memory register which has previously been automatically erased. After the last data bit has been clocked into DI on the 32nd clock edge, the self-timed internal programming cycle is initiated. The write cycle status can be monitored by observing the READY/$\overline{BUSY}$ pin.

Write Enable/Disable — When the XL90C21 is powered up, it comes up in the write disabled state. In order to be programmable, it must receive an enable instruction. The device remains programmable until a disable instruction is entered, or until it is powered down. The disable instruction provides protection against inadvertent writes. Read capability is not affected.

Erase All (ERAL)
Full-chip erase is provided for ease in programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."

Write All (WRAL)
The write all command forces all registers in the memory array to an arbitrary 16-bit pattern. Like the standard write instruction, this instruction is followed by 16-bits of serial data on the DI pin. The erase all command must be entered before forcing write all command.

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address Data	Input
READ	1010	1000	(A_0-A_6)0*	
WRITE	1010	0100	(A_0-A_6)0*	D_0-D_{15}
Erase/Write Enable (EWEN)	1010	0011	XXXXXXXX	
Erase/Write Disable (EWDS)	1010	0000	XXXXXXXX	
Erase All Registers (ERAL)	1010	0010	XXXXXXXX	
Write All Registers (WRAL)	1010	0001	XXXXXXXX	D_0-D_{15}

*If DI is tied to DO, the last bit must be a "0," otherwise, it is "don't care."

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -40°C to +70°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin. ..... -0.3 to Vcc +0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS90C21 or -40°C to +85°C for the XLE90C21, V_{CC} = 5V ±10%

			XLS90C21		XLE90C21		
Symbol	Parameter	Conditions	Min.	Max.	Min.	Max.	Units
I_{CC1}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz CMOS Input Levels		3		3	mA
I_{CC2}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz TTL Input Levels		3		3	mA
I_{CC3}	Standby Current	$\overline{CS}$ = DI = $\overline{SK}$ = PE = Vcc		3/50		3/50	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, $\overline{CS}$, $\overline{SK}$, DI		2		2	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc		2		2	µA
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0		2.0		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL	2.4		2.4		V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL		0.4		0.4	V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

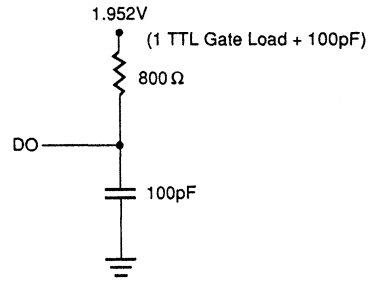
T_A = 0°C to +70°C for the XLS90C21 or -40°C to +85°C for the XLE90C21, V_{CC} = 5V ±10%

			XLS90C21		XLE90C21		
Symbol	Parameter	Conditions	Min.	Max.	Min.	Max.	Units
f_{SK}	$\overline{SK}$ Clock Frequency			1		1	MHz
t_{SKH}	$\overline{SK}$ HIGH Time		450		450		ns
t_{SKL}	$\overline{SK}$ LOW Time		450		450		ns
t_{CS}	Minimum $\overline{CS}$ HIGH Time		1		1		µs
t_{CSS}	$\overline{CS}$ Setup Time	Relative to $\overline{SK}$ ⌝	200		200		ns
t_{DIS}	DI Setup Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to $\overline{SK}$ ⌟	0		0		ns
t_{DIH}	DI Hold Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{PD1}	Output Delay to "1"	AC Test		350		350	ns
t_{PD0}	Output Delay to "0"	AC Test		350		350	ns
t_{SV}	$\overline{CS}$ to Status Valid	AC Test		1		1	µs
t_{DF}	$\overline{CS}$ to DO in 3-state	$\overline{CS}$ = V_{IL}		400		400	ns
$t_{E/W}$	Write Cycle Time			10		10	ms

CAPACITANCE

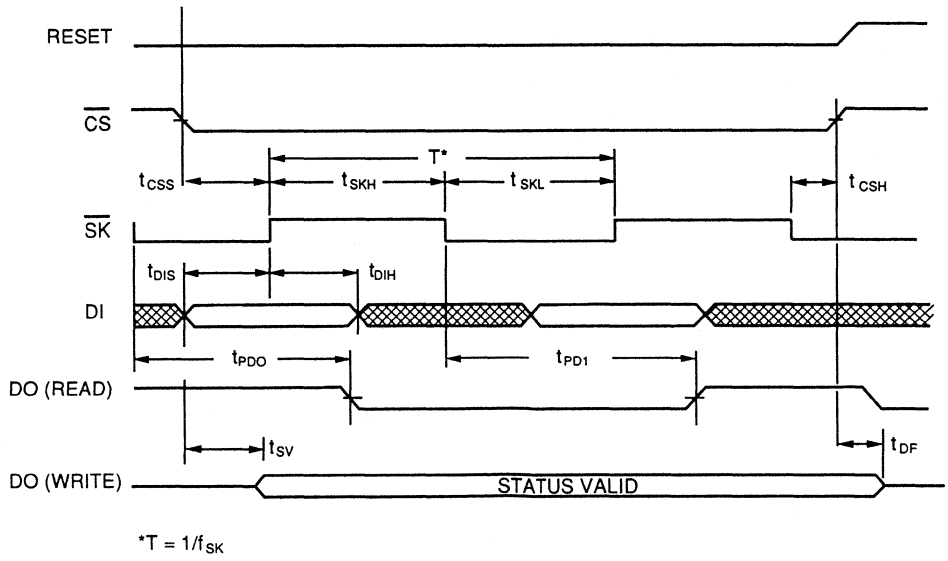
T_A = 25°C, f = 1MHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING

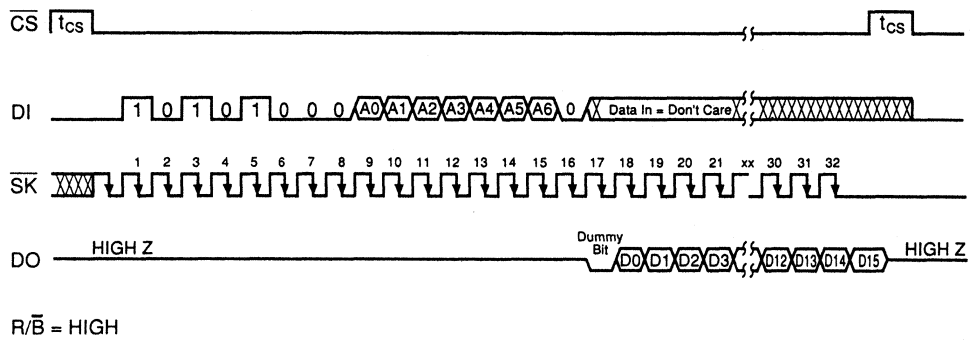


FIGURE 3. READ CYCLE TIMING

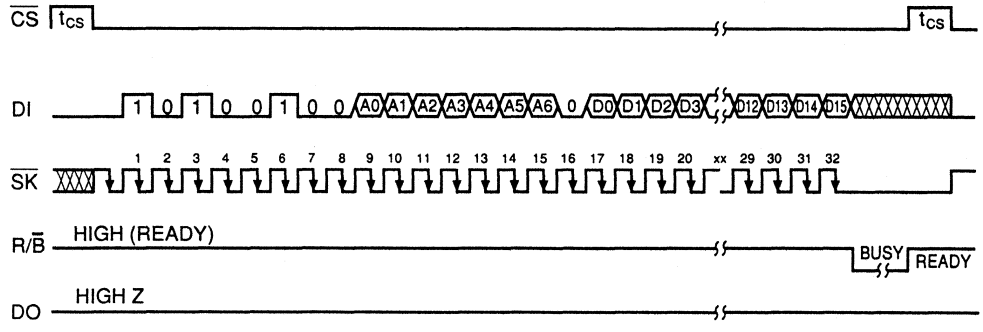


FIGURE 4. WRITE CYCLE TIMING

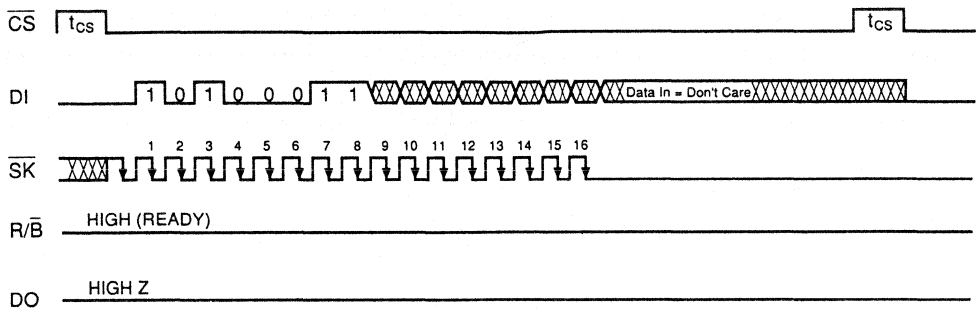


FIGURE 5. WRITE ENABLE (EWEN) CYCLE TIMING

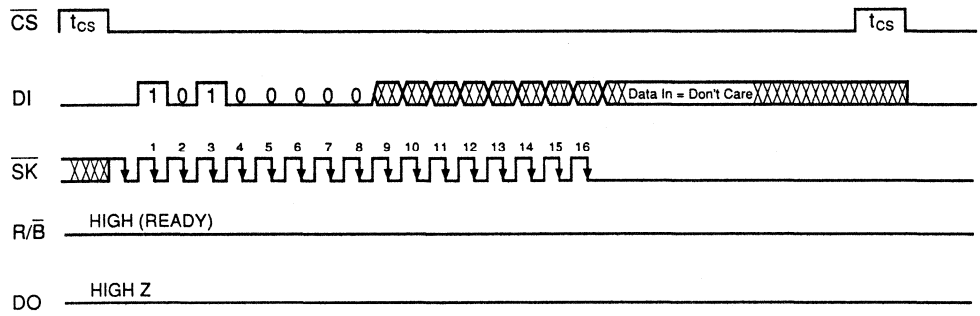


FIGURE 6. WRITE DISABLE (EWDS) CYCLE TIMING

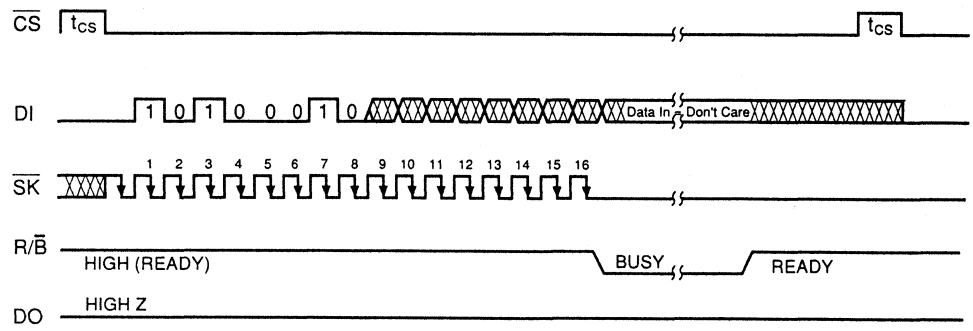


FIGURE 7. ERASE ALL (ERAL) CYCLE TIMING

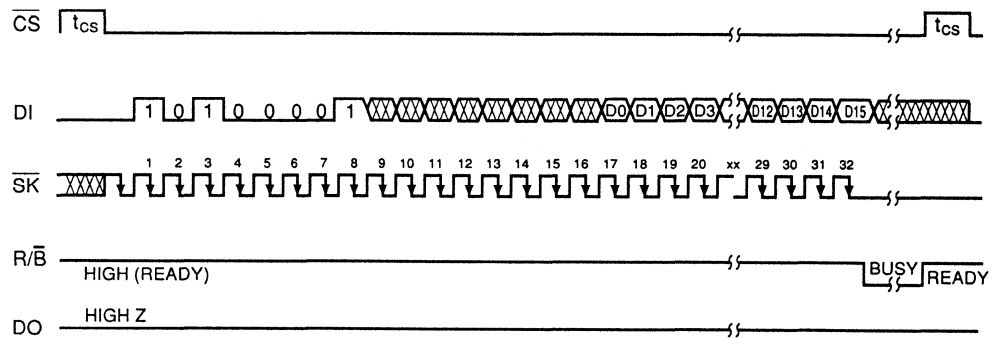


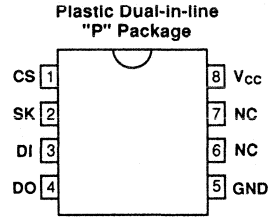
FIGURE 8. WRITE ALL (WRAL) CYCLE TIMING

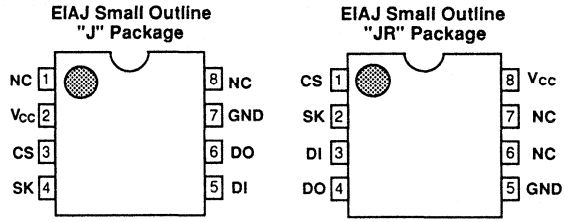
4,096-Bit Serial Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS





PIN NAMES

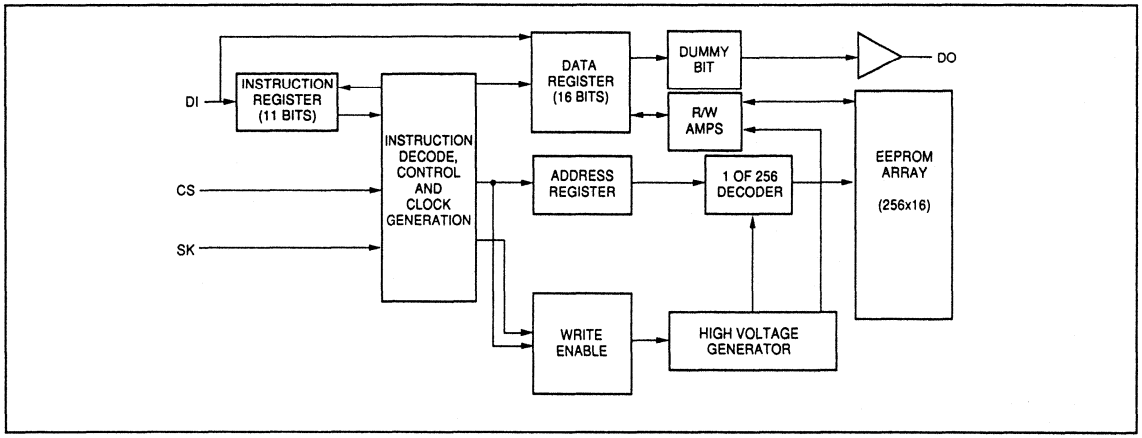
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC66 is a low cost 4,096-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC66 provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC66 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC66 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC66 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC66 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC66 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC66 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5V, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC66 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{BUSY}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{BUSY}$ flag. Therefore, it is important if you want to access the READY/$\overline{BUSY}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{BUSY}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{BUSY}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC66 has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC66 is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_7-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	(A_7-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC66 ..... 0°C to +70°C
XLE93LC66 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66 or -40°C to +85°C for the XLE93LC66

			Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4			V

AC ELECTRICAL CHARACTERISTICS

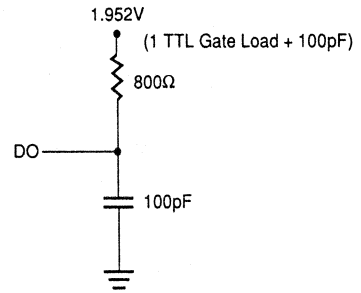
T_A = 0°C to +70°C for the XLS93LC66 or -40°C to +85°C for the XLE93LC66

			Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKH}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10			ms

CAPACITANCE

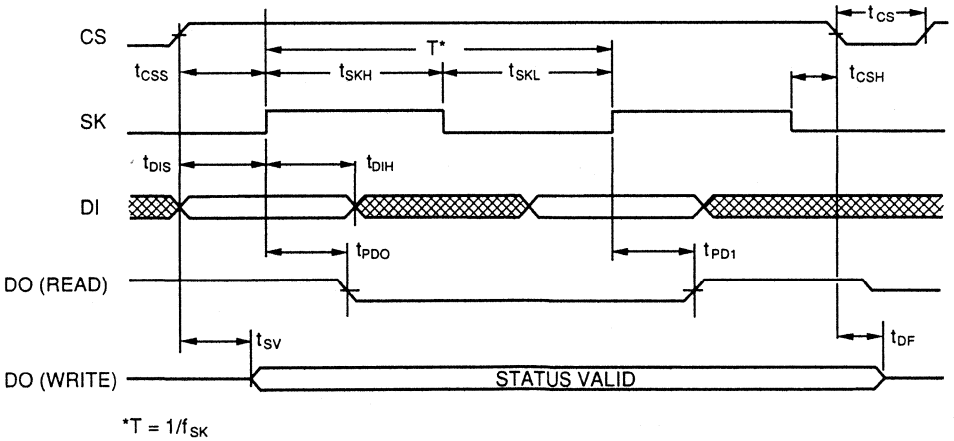
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



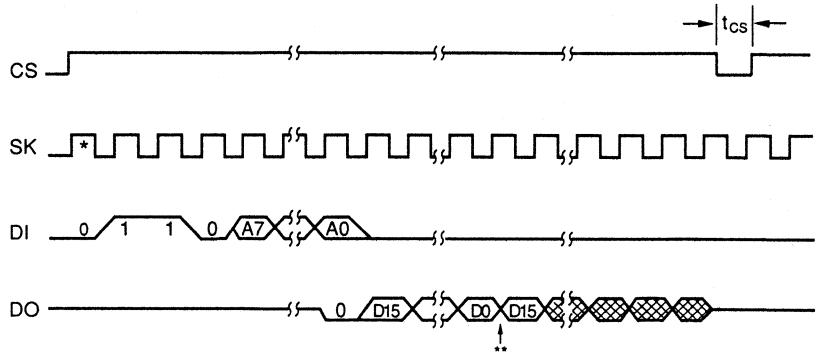
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



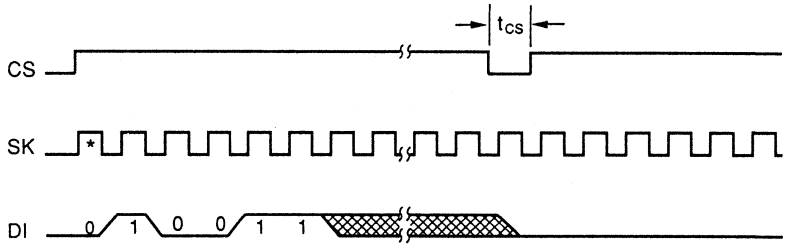
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



*This leading clock is optional.
** Address pointer automatically cycles to the next register.

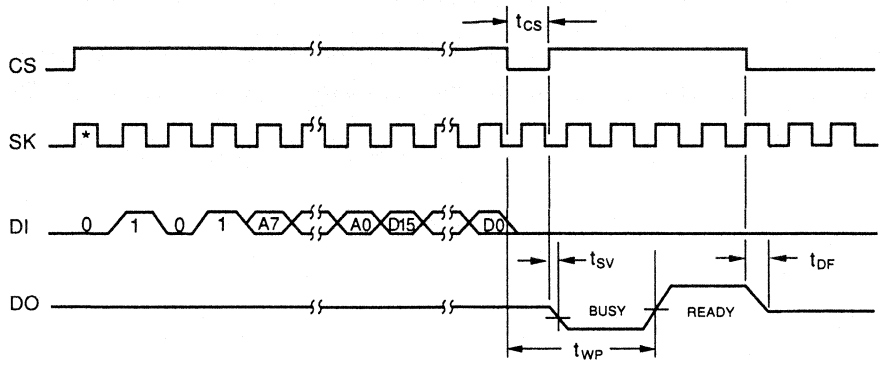
FIGURE 3. READ CYCLE TIMING



DO = 3-state

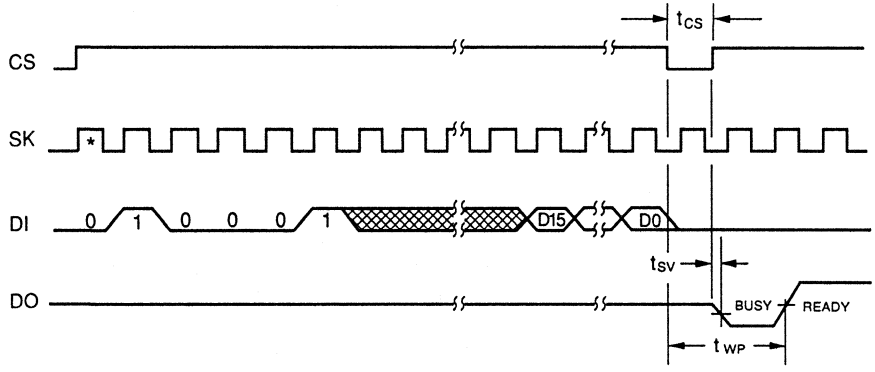
*This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



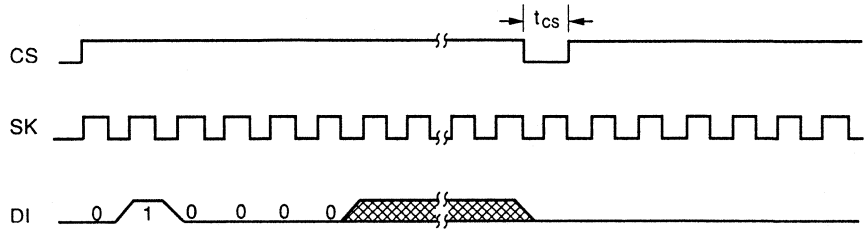
*This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



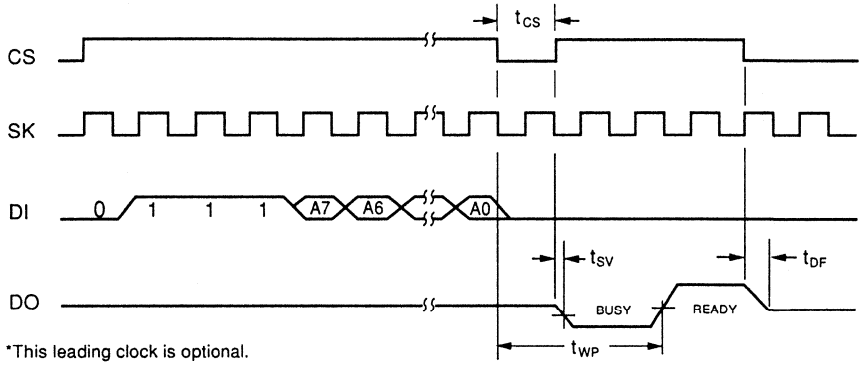
*This leading clock is optional.

FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



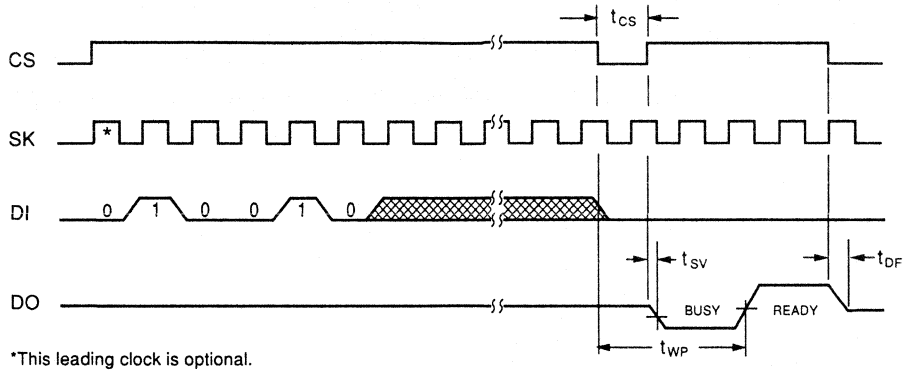
DO = 3-STATE
*This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



*This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



*This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

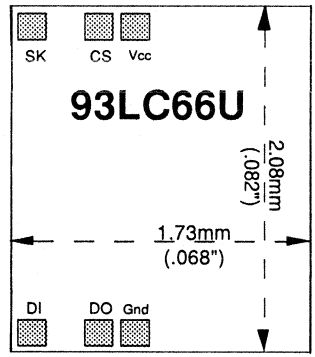
Preliminary

4,096-Bit Serial Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
  - **— V_{CC} lockout inadvertent write protection**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E^2PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

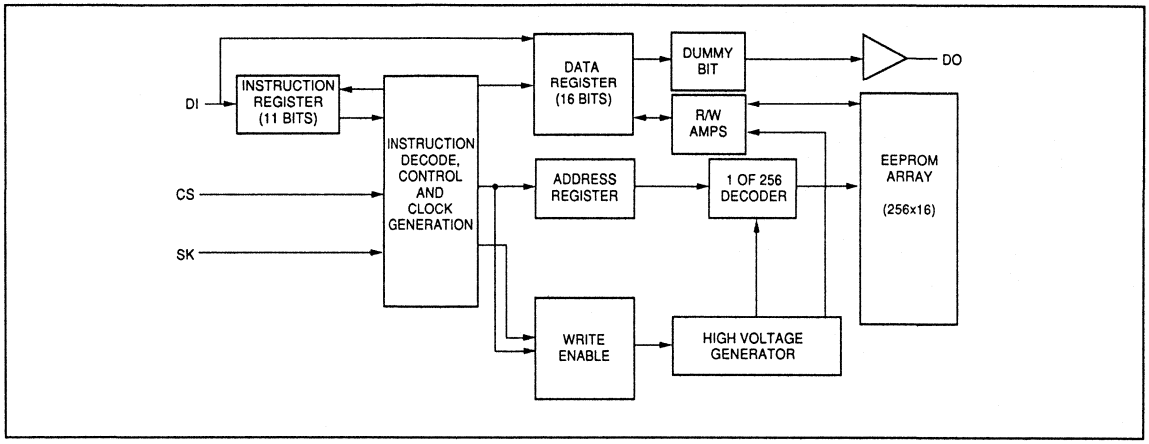
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC66U is a low cost 4,096-bit, nonvolatile, serial E^2PROM. It is fabricated using EXEL's advanced CMOS E^2PROM technology. The XL93LC66U provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC66U dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

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ENDURANCE AND DATA RETENTION

The XL93LC66U is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC66U is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC66U will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC66U has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC66U is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 4.5V, the maximum clock frequency is reduced to 250kHz.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC66U has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output until the top of the array is reached at which point the memory pointer rolls over to the bottom of the array. The address will wrap around with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag , not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pad indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

V_{CC} Lockout - Inadvertent Write Protection
To ensure against inadvertent write operations, the XL93LC66U has been equipped with an internal V_{CC} sensor circuit which inhibits data alteration when the supply voltage (V_{CC}) falls below V_{WI}. If the applied V_{CC} is below 3.75V (typical), the XL93LC66U is inhibited from executing write operations thereby protecting the non-volatile data from inadvertent write operations.

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_7-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	(A_7-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC66U ..... 0°C to +70°C
XLE93LC66U ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U or -40°C to +85°C for the XLE93LC66U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V
V_{WI}	Write Inhibit Threshold		2.7	4.4	n/a	n/a	V

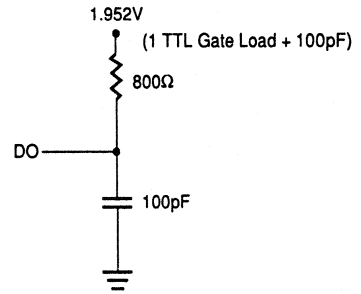
AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U or -40°C to +85°C for the XLE93LC66U

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time	XLS XLE	250 400		2000 2000		ns ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10	n/a	n/a	ms

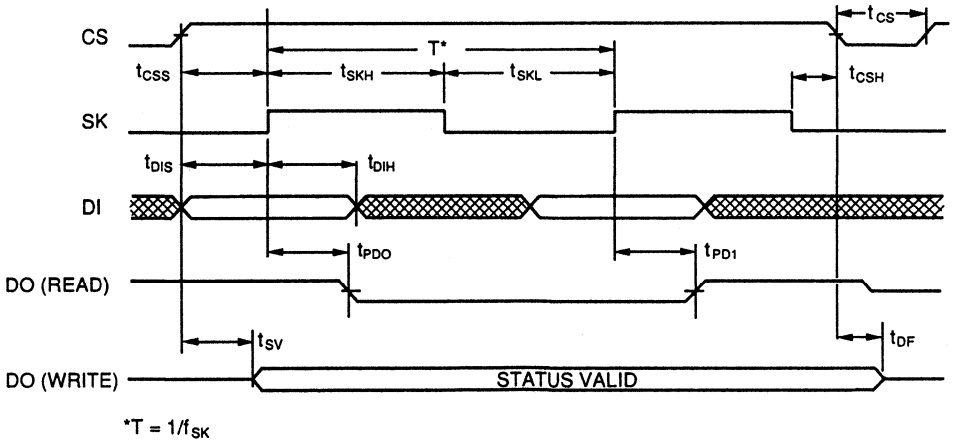
CAPACITANCE
T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



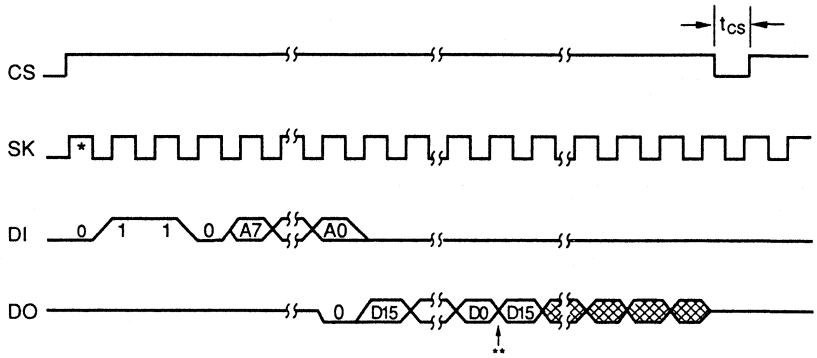
Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



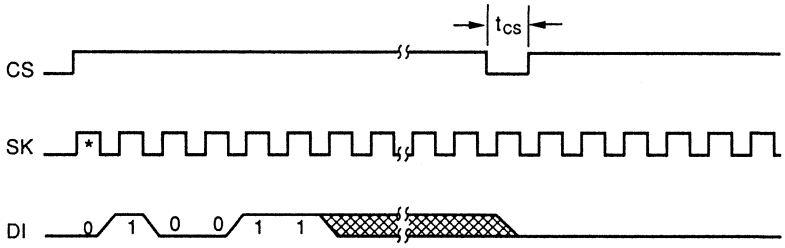
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



*This leading clock is optional.
** Address pointer automatically cycles to the next register.

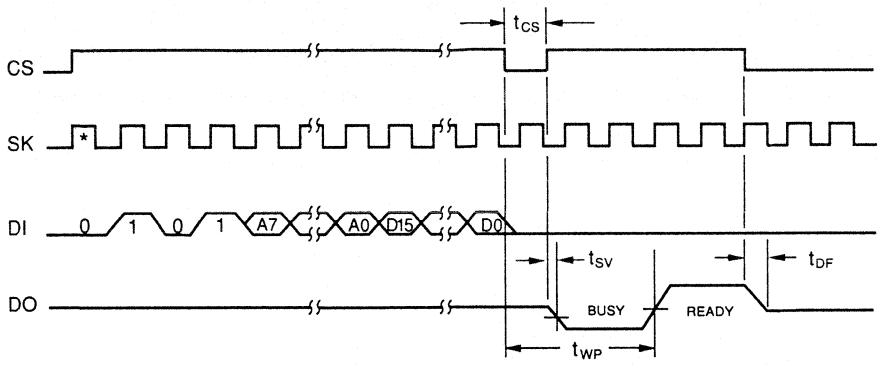
FIGURE 3. READ CYCLE TIMING



DO = 3-state

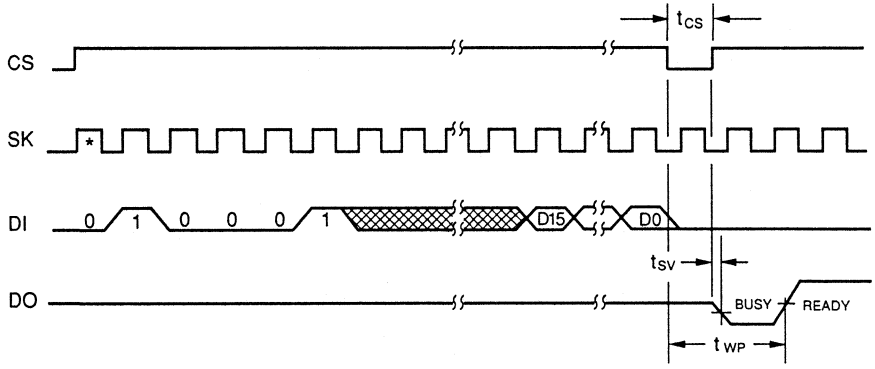
*This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



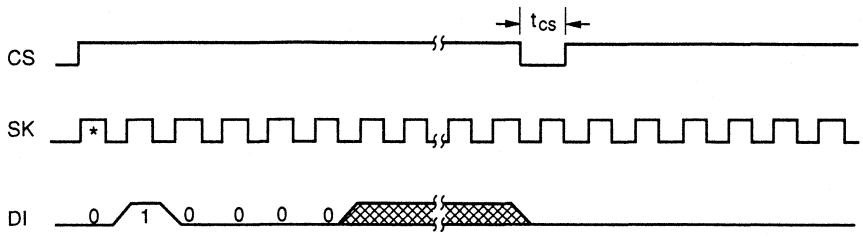
*This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



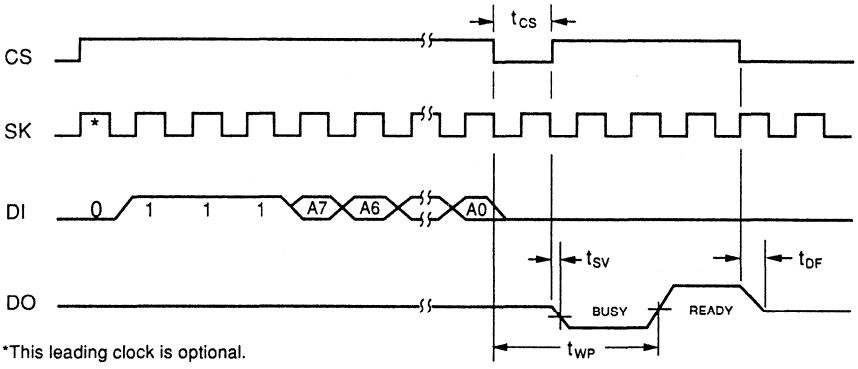
*This leading clock is optional.

FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



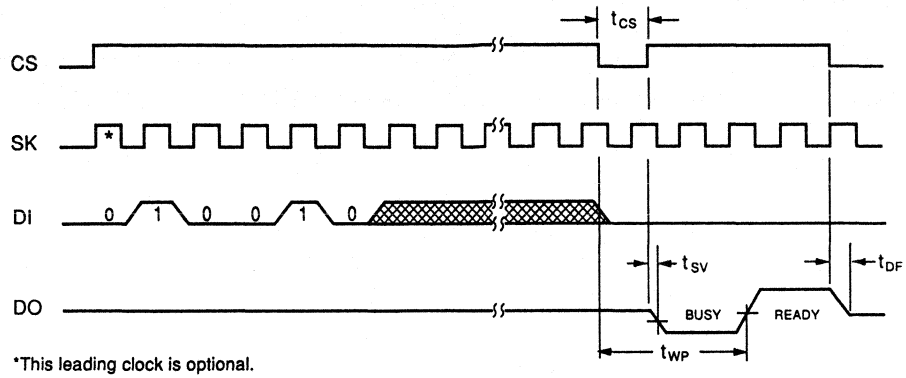
DO = 3-STATE
*This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



*This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



*This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

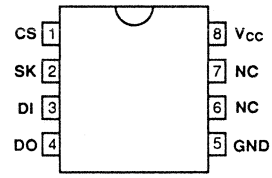
4,096-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

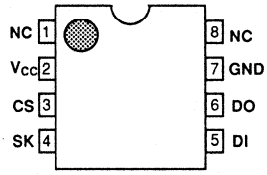
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

PIN CONFIGURATIONS

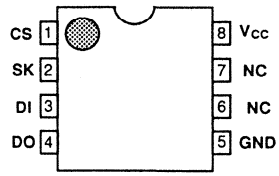
Plastic Dual-in-line "P" Package



EIAJ Small Outline "J" Package



EIAJ Small Outline "JR" Package



PIN NAMES

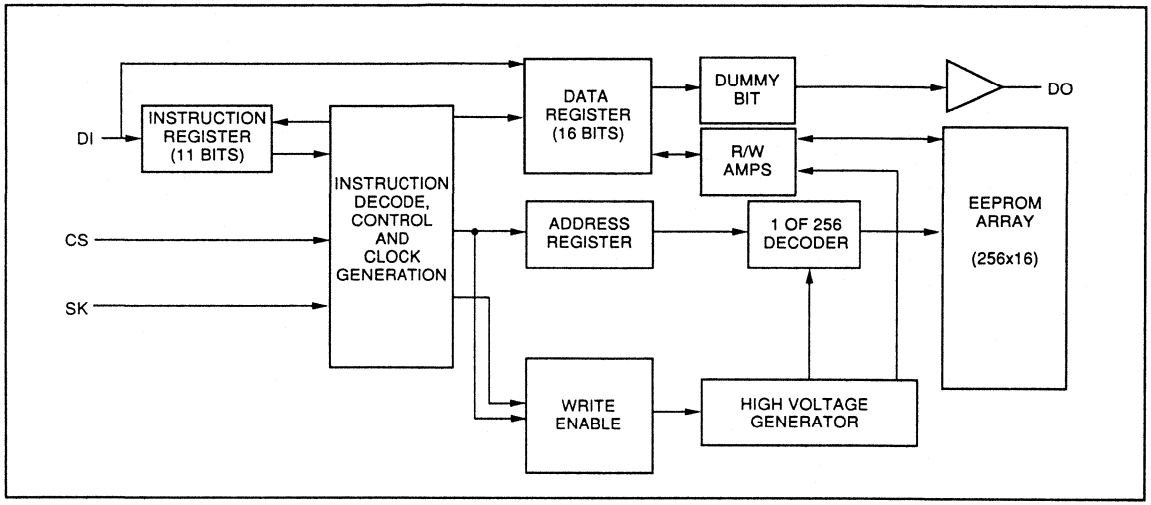
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

OVERVIEW

The XL93LC66-3 is a low cost 4,096-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC66-3 provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC66-3 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC66-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC66-3 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC66-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC66-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC66-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** V_{IL} = 0.1 V_{CC} min., V_{IH} = 0.9 V_{CC} min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC66-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_7-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	(A_7-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC66-3 ..... 0°C to +70°C
XLE93LC66-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66-3 or -40°C to +85°C for the XLE93LC66-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC66-3		XLE93LC66-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66-3 or -40°C to +85°C for the XLE93LC66-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC66-3		XLE93LC66-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⎍	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⎍	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ⎏	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⎍	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66-3 or -40°C to +85°C for the XLE93LC66-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC66-3		XLE93LC66-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{CC} SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66-3 or -40°C to +85°C for the XLE93LC66-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC66-3		XLE93LC66-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

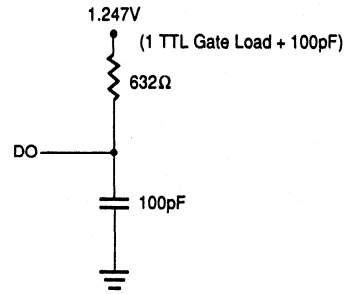


FIGURE 1. AC TEST CONDITIONS

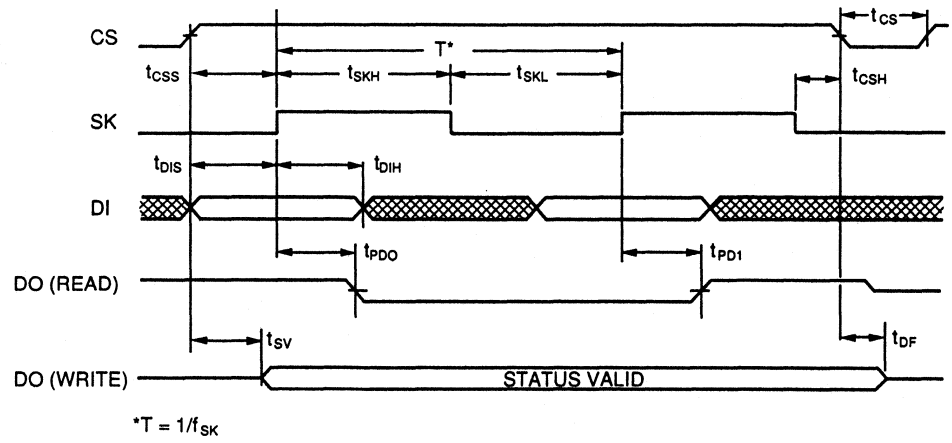
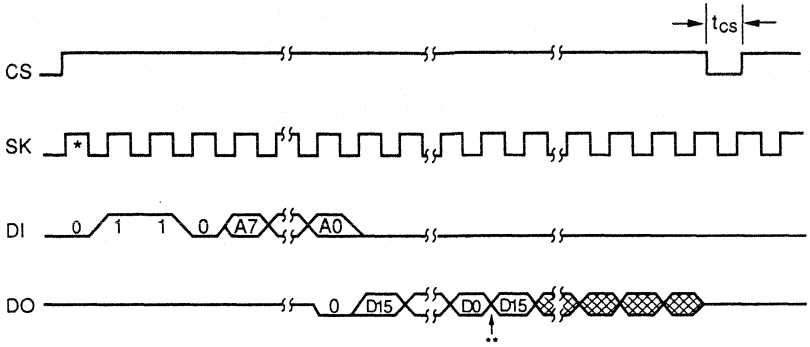


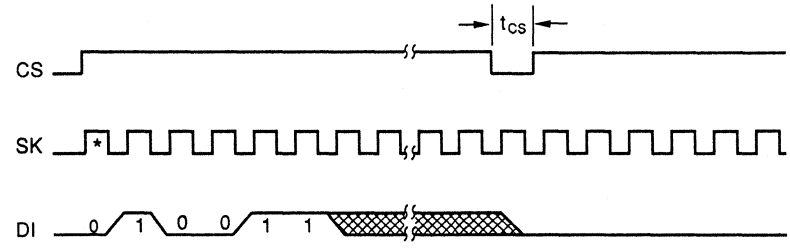
FIGURE 2. SYNCHRONOUS DATA TIMING



*This leading clock is optional.

** Address pointer automatically cycles to the next register.

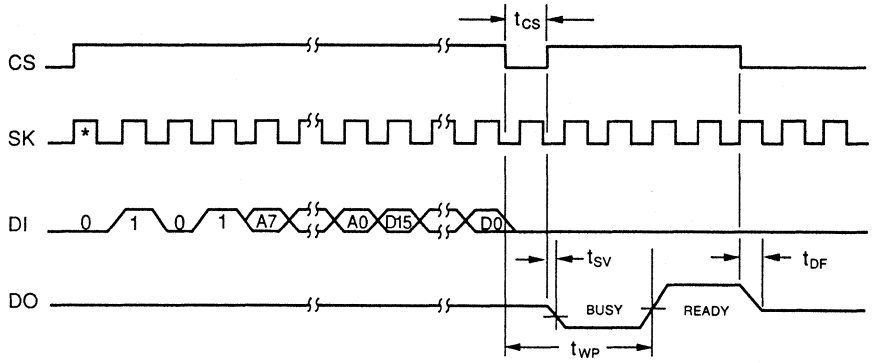
FIGURE 3. READ CYCLE TIMING



DO = 3-state

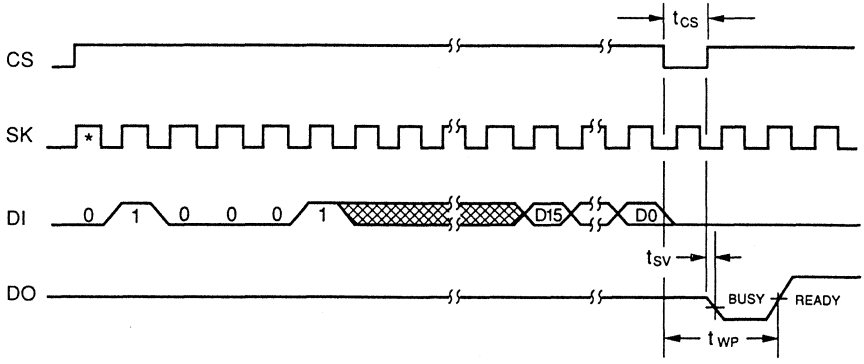
*This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



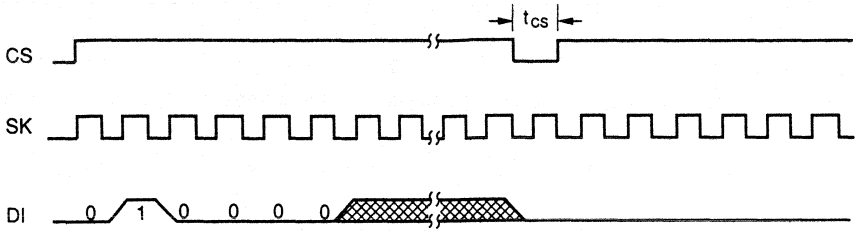
*This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



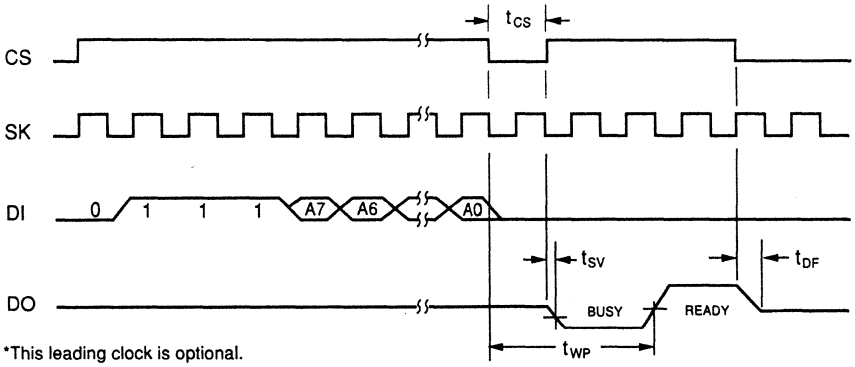
*This leading clock is optional.

FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



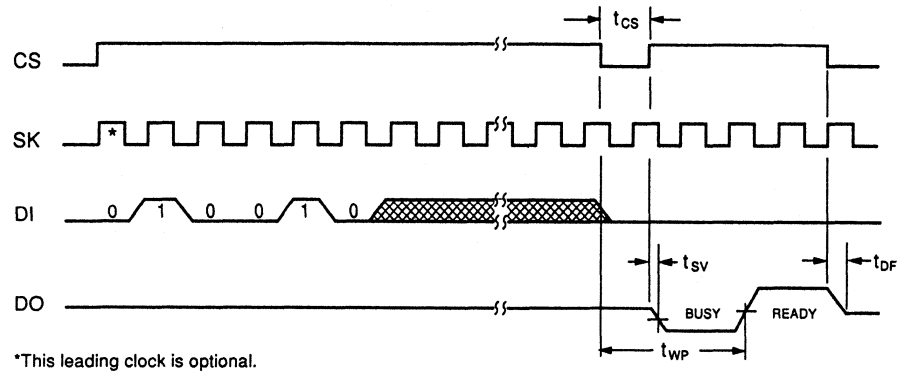
DO = 3-STATE
*This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



*This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



*This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

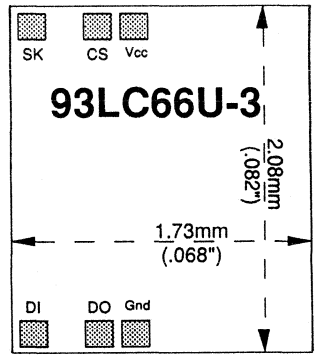
Preliminary

4,096-Bit Serial (3V to 5V) Electrically Erasable PROM with 2V Read Capability

FEATURES

- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— 3V to 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— Auto increment for efficient data dump**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

DIE CONFIGURATION



PAD NAMES

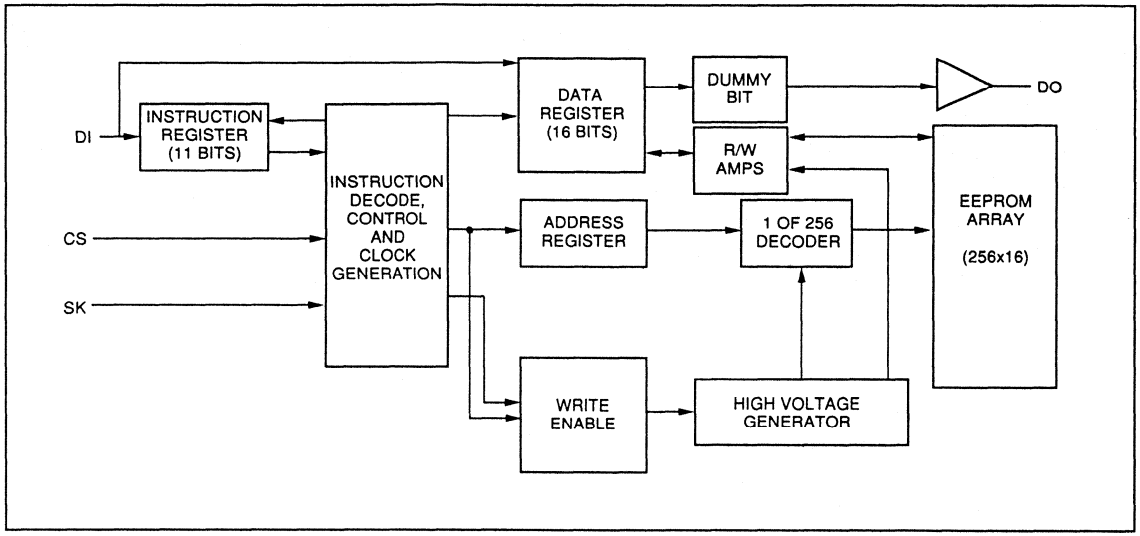
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply

OVERVIEW

The XL93LC66U-3 is a low cost 4,096-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93LC66U-3 provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pad (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The XL93LC66U-3 dice are available in either wafer or waffle-pack form.

The self-timed write cycle includes an automatic erase-before-write capability. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pad will indicate the READY/$\overline{\text{BUSY}}$ status of the chip.

BLOCK DIAGRAM



APPLICATIONS

The XL93LC66U-3 is ideal for high volume applications requiring low power and low density storage. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93LC66U-3 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93LC66U-3 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pad. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93LC66U-3 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pad. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93LC66U-3 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93LC66U-3 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V. (Note: When V_{CC} falls below 2.7V, the normal 3V specs apply, except for the following: **DC:** V_{IL} = 0.1 V_{CC} min., V_{IH} = 0.9 V_{CC} min.; **AC:** t_{SKH} = 2µs min., t_{SKL} = 2µs min.)

Auto Increment Read Operations

In the interest of memory transfer operation applications, the XL93LC66U-3 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS HIGH until the Chip Select control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pad indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_7-A_0)	
WEN (Write Enable)	1	00	11XXXXXX	
WRITE	1	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXXXX	
ERASE	1	11	(A_7-A_0)	
ERAL (Erase All Registers)	1	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93LC66U-3 ..... 0°C to +70°C
XLE93LC66U-3 ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pad ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U-3 or -40°C to +85°C for the XLE93LC66U-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC66U-3		XLE93LC66U-3		Units
			Min	Max	Min	Max	
I_{CC}	Operating Current CMOS Input Levels	CS = Vcc, SK = 250KHz		2		2	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.15 Vcc	-0.1	0.15 Vcc	V
V_{IH}	Input High Voltage		0.8 Vcc	Vcc+0.2	0.8 Vcc	Vcc+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U-3 or -40°C to +85°C for the XLE93LC66U-3, V_{CC} = 3V ±10%

Symbol	Parameter	Conditions	XLS93LC66U-3		XLE93LC66U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	250	0	250	KHz
t_{SKH}	SK High Time		1		1		µs
t_{SKL}	SK Low Time		1		1		µs
t_{CS}	Minimum CS Low Time		1		1		µs
t_{CSS}	CS Setup Time	Relative to SK ⌐	200		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	400		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	400		400		ns
t_{PD1}	Output Delay to "1"	AC Test		2		2	µs
t_{PD0}	Output Delay to "0"	AC Test		2		2	µs
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		2		2	µs
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		400		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		20		25	ms

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U-3 or -40°C to +85°C for the XLE93LC66U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC66U-3		XLE93LC66U-3		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current	CS = DI = SK =0V		2		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc (CS, SK, DI)	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.8	V
V_{IH}	Input High Voltage		2	Vcc	2	Vcc	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		2.4		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93LC66U-3 or -40°C to +85°C for the XLE93LC66U-3, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	XLS93LC66U-3		XLE93LC66U-3		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1	0	1	MHz
t_{SKH}	SK High Time		250		400		ns
t_{SKL}	SK Low Time		250		250		ns
t_{CS}	Minimum CS Low Time		250		250		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		50		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		100		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		100		ns
t_{PD1}	Output Delay to "1"	AC Test		500		500	ns
t_{PD0}	Output Delay to "0"	AC Test		500		500	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		500	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		100	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		10	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

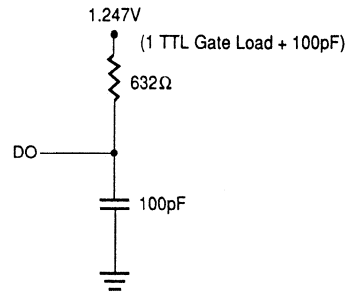
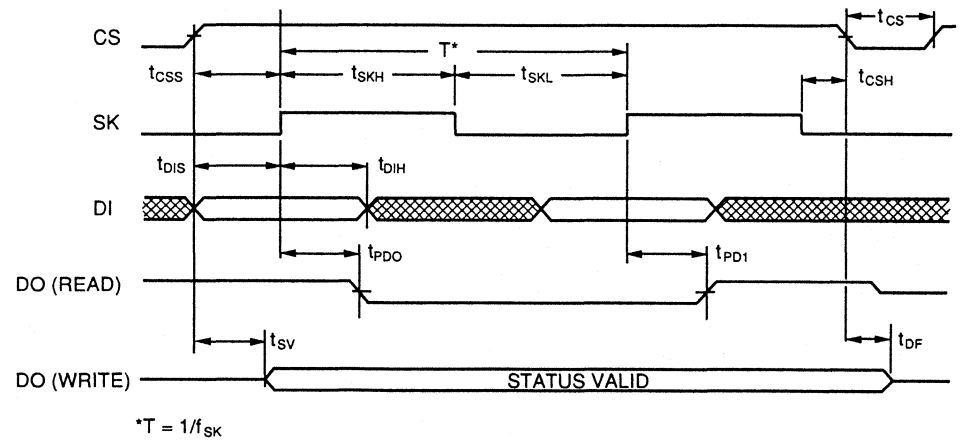
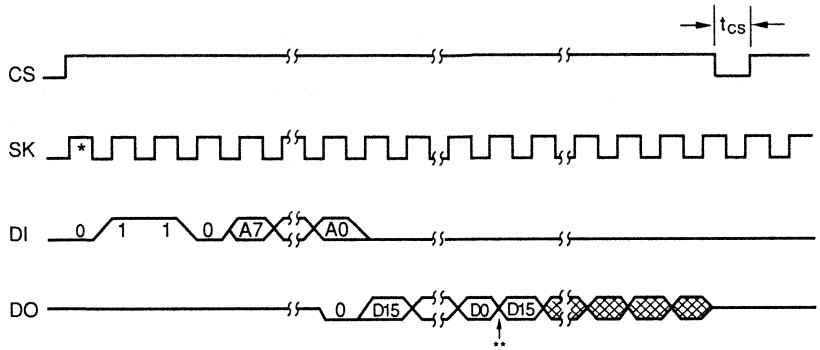


FIGURE 1. AC TEST CONDITIONS



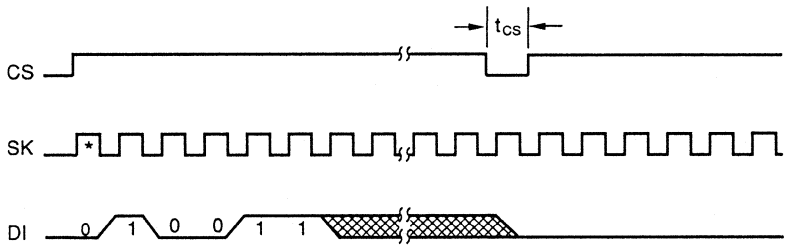
*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING



*This leading clock is optional.
** Address pointer automatically cycles to the next register.

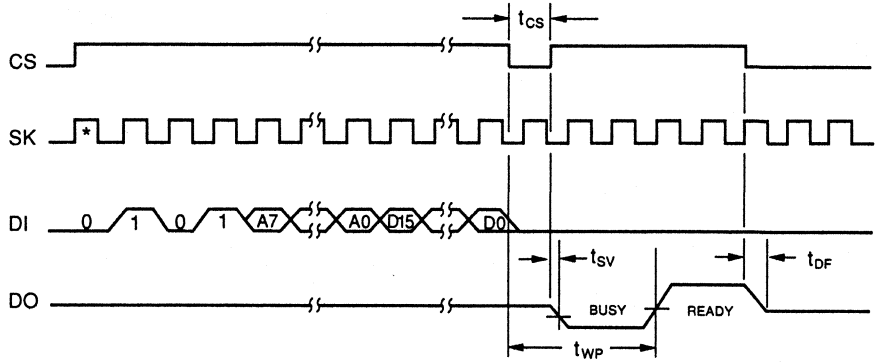
FIGURE 3. READ CYCLE TIMING



DO = 3-state

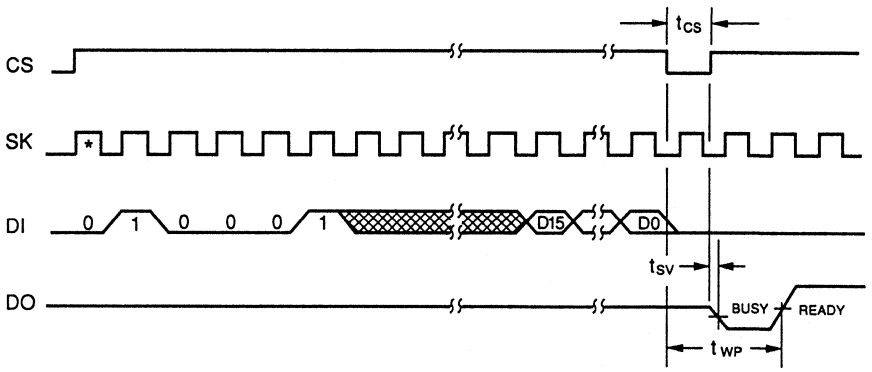
*This leading clock is optional.

FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING



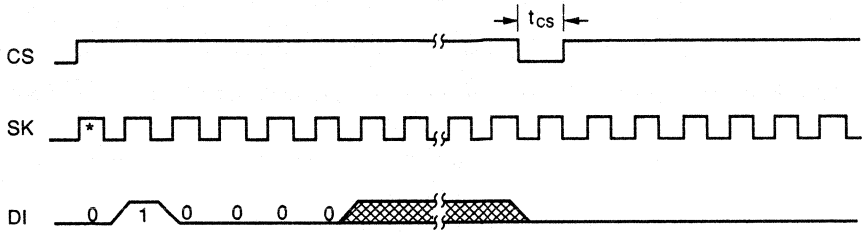
*This leading clock is optional.

FIGURE 5. WRITE CYCLE TIMING



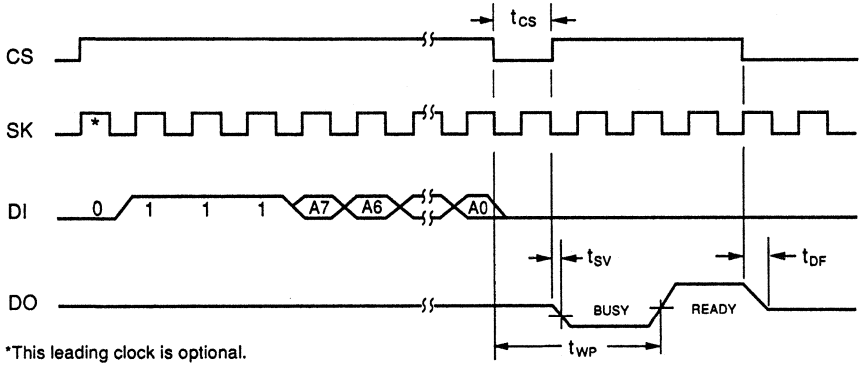
*This leading clock is optional.

FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING



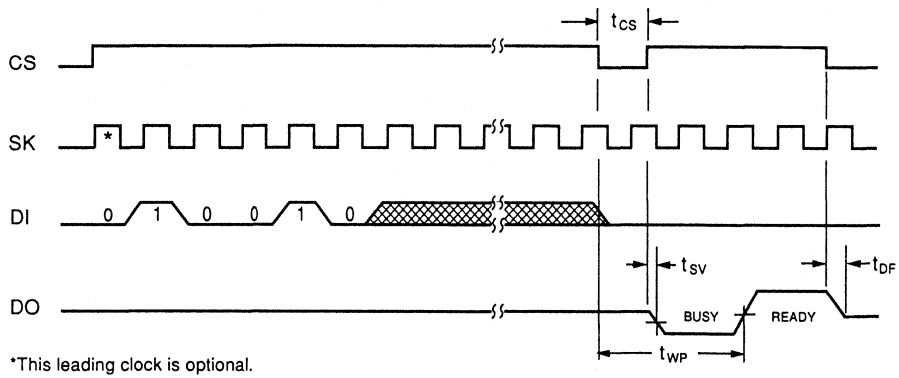
DO = 3-STATE
*This leading clock is optional.

FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING



*This leading clock is optional.

FIGURE 8. ERASE (REGISTER) CYCLE TIMING



*This leading clock is optional.

FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

4,096-Bit Serial Electrically Erasable PROM
with 2V Read Capability

FEATURES

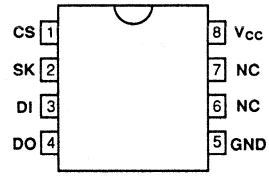
- **State-of-the-Art Architecture**
  - **— Nonvolatile data storage**
  - **— Single supply - 5V operation**
  - **— Fully TTL compatible inputs and outputs**
  - **— 1MHz operation**
- **Hardware and Software Write Protection**
  - **— Defaults to write-disabled state at power up**
  - **— Software instructions for write-enable/disable**
- **Low Power Consumption**
  - **— 1mA active (typical)**
  - **— 1µA standby (typical)**
- **Low Voltage Read Operations**
  - **— Reliable read operations down to 2.0 volts**
- **Advanced Low Voltage CMOS E²PROM Technology**
- **Versatile, Easy-to-Use Interface**
  - **— Self-timed programming cycle**
  - **— Automatic erase-before-write**
  - **— Programming Status Indicator**
  - **— Word and chip erasable**
- **Durable and Reliable**
  - **— 10-year data retention after 100K write cycles**
  - **— Minimum of 100,000 write cycles per word**
  - **— Unlimited read cycles**
  - **— ESD protection**

OVERVIEW

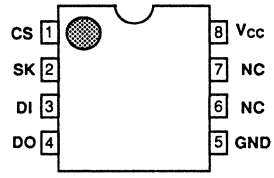
The XL93C66 is a low cost 4,096-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL93C66 provides efficient nonvolatile read/write memory arranged as 256 registers of 16 bits each. Seven 11-bit instructions control the operation of the device, which include read, write, and mode enable functions. The data output pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle.

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



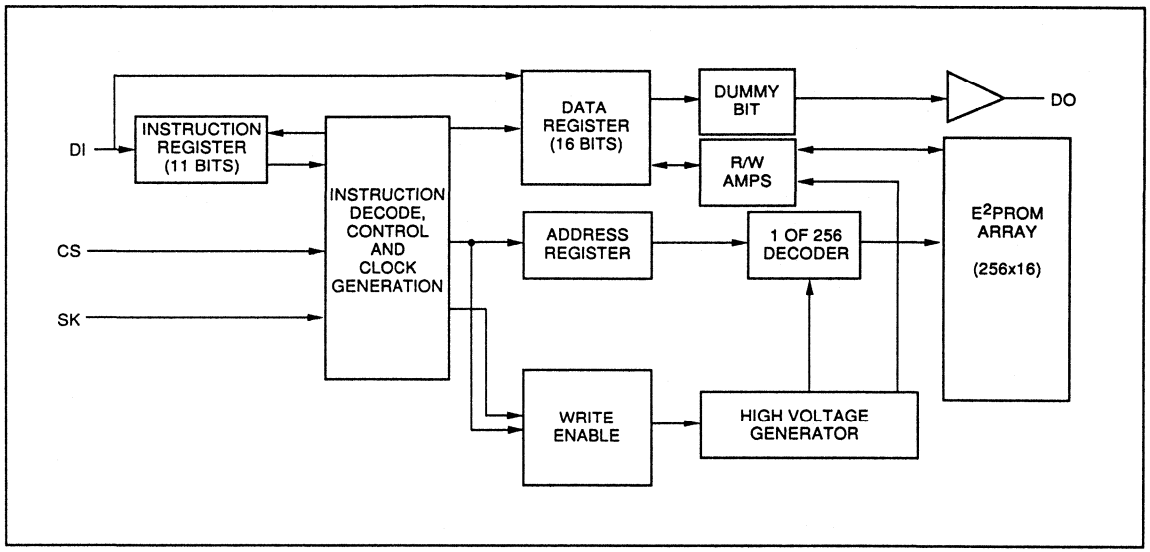
EIAJ Small Outline "JR" Package



PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
NC	Not Connected

BLOCK DIAGRAM



APPLICATIONS

The XL93C66 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Candidate applications include robotics, alarm devices, electronic locks, meters and instrumentation settings.

ENDURANCE AND DATA RETENTION

The XL93C66 is designed for applications requiring up to 100,000 write cycles per bit. It provides 10 years of secure data retention without power after the execution of 100,000 write cycles for each location.

DEVICE OPERATION

The XL93C66 is controlled by seven 11-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (8 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the XL93C66 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)

The READ instruction is the only instruction that results in serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 16-bit output data string.) The output on DO changes during the low-to-high transitions of SK. (See Figure 3.)

Low Voltage Read

The XL93C66 has been designed to ensure that data read operations are reliable in low voltage environments. The XL93C66 is guaranteed to provide accurate data during read operations with V_{CC} as low as 2.0V.

Write Enable (WEN)

The write enable (WEN) instruction must be executed before any device programming can be done. When V_{CC} is applied, this device powers up in the write disabled state. The device then remains in a write disabled state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until V_{CC} is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 4.)

Write (WRITE)
The WRITE instruction includes 16 bits of data to be written into the specified register. After the last data bit has been clocked into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" means programming is still in progress; logical "1" means the selected register has been written, and the part is ready for another instruction. (See Figure 5.) (NOTE: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Before a WRITE instruction can be executed, the device must be write enabled (see WEN).

Write All (WRALL)
The write all (WRALL) instruction programs all registers with the data pattern specified in the instruction.(See Figure 6.) The ERAL operation is required before WRAL operation. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the chip. (See Figure 6.)

Write Disable (WDS)
The write disable (WDS) instruction disables all programming capabilities. This protects the entire memory array against accidental modification of data until a WEN instruction is executed. (When V_{CC} is applied, this part powers up in the write disabled state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (See Figure 7.)

Erase Register
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after a minimum of t_{CS}, will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: a logical "0" indicates programming is still in progress; a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (See Figure 8.)

Erase All (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1." (See Figure 9.)

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address	Input Data
READ	01	10	(A_7-A_0)	
WEN (Write Enable)	01	00	11XXXXXX	
WRITE	01	01	(A_7-A_0)	D_{15}-D_0
WRALL (Write All Registers)	01	00	01XXXXXX	D_{15}-D_0
WDS (Write Disable)	01	00	00XXXXXX	
ERASE	01	11	(A_7-A_0)	
ERAL (Erase All Registers)	01	00	10XXXXXX	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias: XLS93C66 ..... 0°C to +70°C
XLE93C66 ..... -40°C to +85°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3 to Vcc +0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS93C66 or -40°C to +85°C for the XLE93C66

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
I_{CC1}	Operating Current CMOS Input Levels	CS = Vcc, SK = 1MHz		2		2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH}, SK = 1MHz		5		5	mA
I_{SB}	Standby Current (CMOS)	CS = DI = SK =0V		4		2	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, CS, SK, DI	-1	1	-1	1	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc, CS = 0V	-1	1	-1	1	µA
V_{IL}	Input Low Voltage		-0.1	0.8	-0.1	0.1 Vcc	V
V_{IH}	Input High Voltage		2	Vcc	0.9 Vcc	Vcc + 0.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL		0.4		n/a	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL	2.4		n/a		V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc - 0.2		V

AC ELECTRICAL CHARACTERISTICS

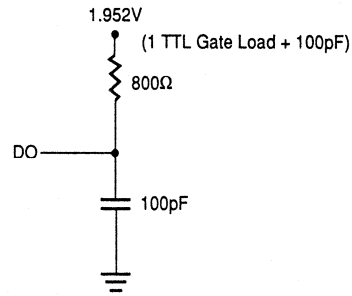
T_A = 0°C to +70°C for the XLS93C66 or -40°C to +85°C for the XLE93C66

Symbol	Parameter	Conditions	Vcc = 5V ± 10%		Vcc=2.0V (Read Only)		Units
			Min	Max	Min	Max	
f_{SK}	SK Clock Frequency		0	1000	0	250	KHz
t_{SKH}	SK High Time		250		2000		ns
t_{SKL}	SK Low Time		250		2000		ns
t_{CS}	Minimum CS Low Time		250		1000		ns
t_{CSS}	CS Setup Time	Relative to SK ⌐	50		200		ns
t_{DIS}	DI Setup Time	Relative to SK ⌐	100		400		ns
t_{CSH}	CS Hold Time	Relative to SK ¬	0		0		ns
t_{DIH}	DI Hold Time	Relative to SK ⌐	100		400		ns
t_{PD1}	Output Delay to "1"	AC Test		500		2000	ns
t_{PD0}	Output Delay to "0"	AC Test		500		2000	ns
t_{SV}	CS to Status Valid	AC Test C_L = 100pF		500		2000	ns
t_{DF}	CS to DO in 3-state	CS = Low to DO = Hi-Z		100		400	ns
t_{WP}	Write Cycle Time	CS = Low to DO = Ready		10		n/a	ms

CAPACITANCE

T_A = 25°C, f = 250KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS

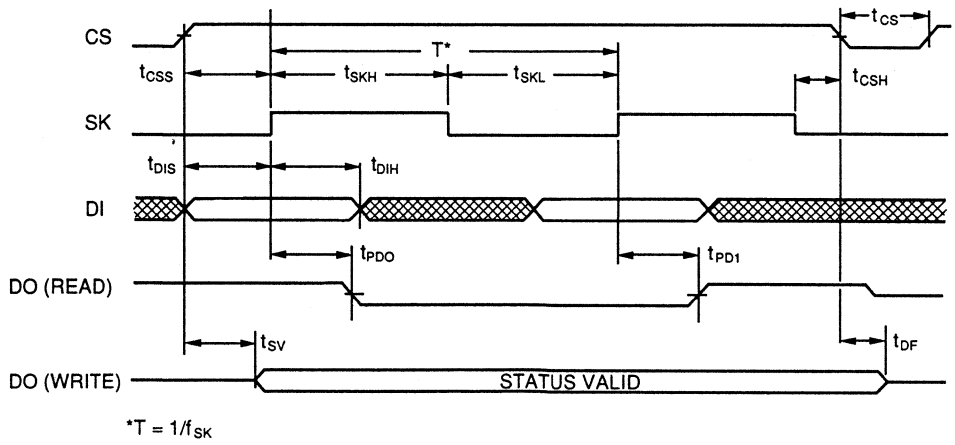


FIGURE 2. SYNCHRONOUS DATA TIMING

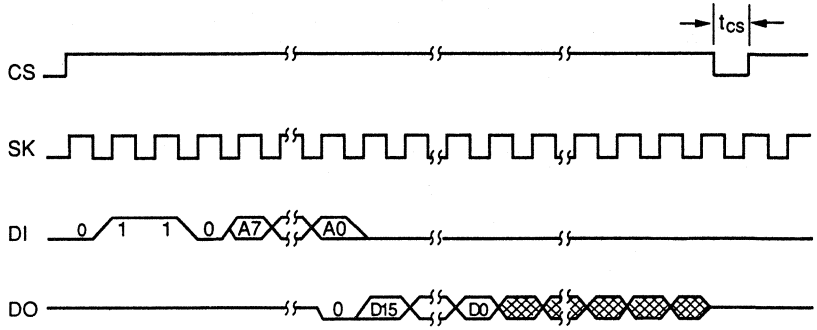


FIGURE 3. READ CYCLE TIMING

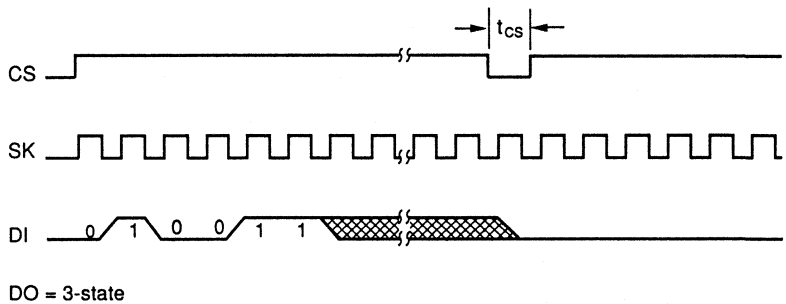


FIGURE 4. WRITE ENABLE (WEN) CYCLE TIMING

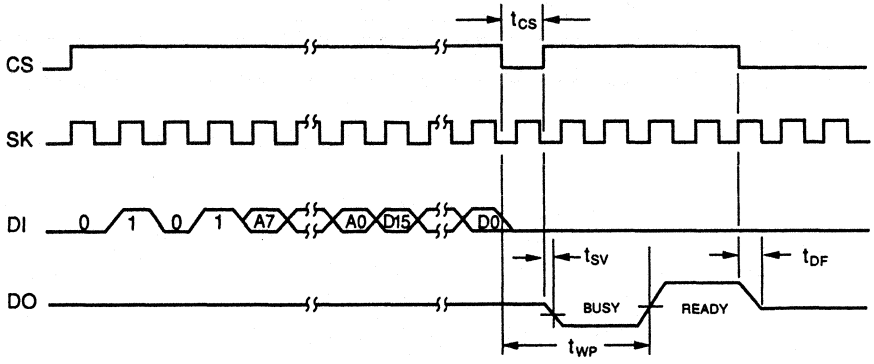


FIGURE 5. WRITE CYCLE TIMING

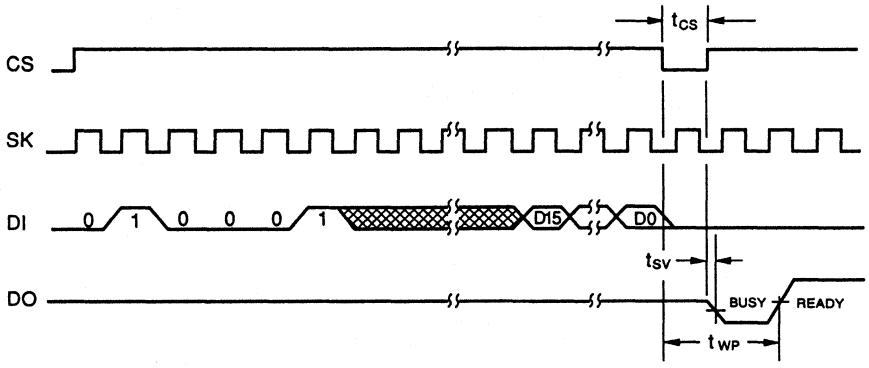


FIGURE 6. WRITE ALL (WRALL) CYCLE TIMING

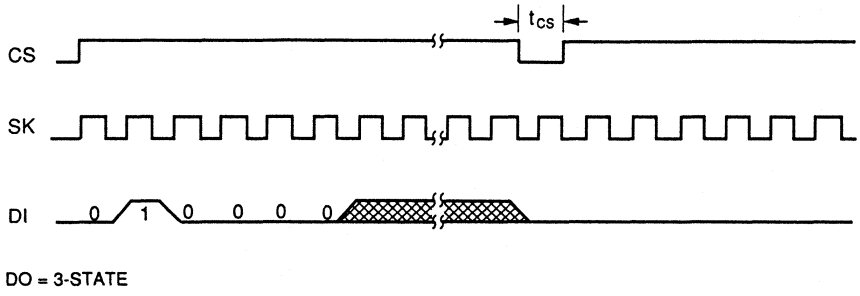


FIGURE 7. WRITE DISABLE (WDS) CYCLE TIMING

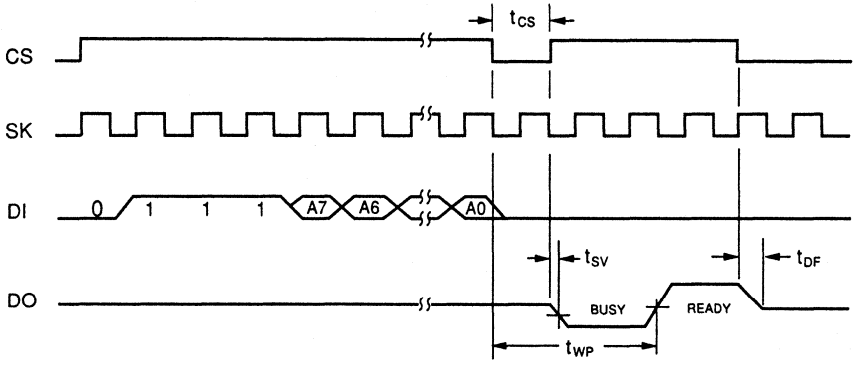


FIGURE 8. ERASE (REGISTER) CYCLE TIMING

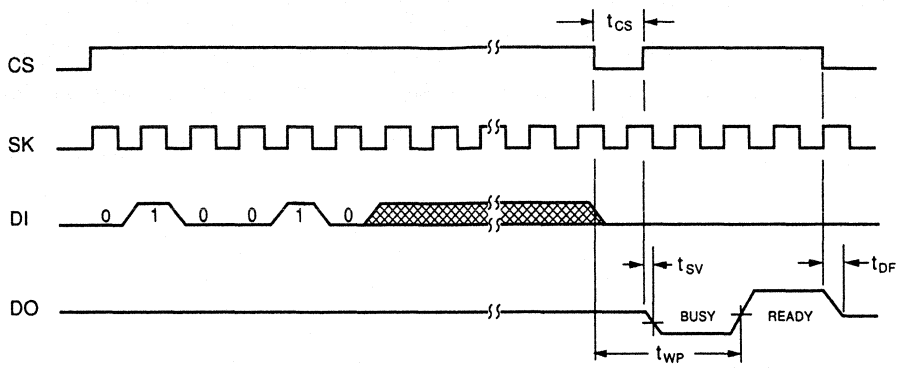


FIGURE 9. ERASE ALL (ERAL) CYCLE TIMING

PRELIMINARY

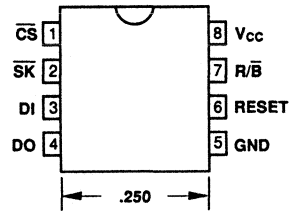
4096-Bit Serial (5V) Electrically Erasable PROM

FEATURES

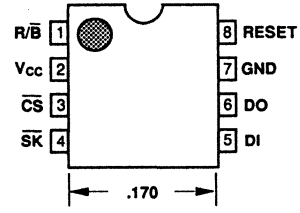
- **4096-bit Serial Architecture**
  - **—256 registers, 16 bits each**
  - **—Nonvolatile data storage**
  - **—Single 5V supply**
- **Versatile, Easy-to-Use Interface**
  - **—READY/$\overline{\text{BUSY}}$ status signal**
  - **—Automatic write cycle time-out**
  - **—Software controlled write protection**
- **Advanced CMOS E²PROM Technology**
- **Low Power Consumption**
  - **—3mA max. active**
  - **—1mA max. standby, TTL**
  - **—25µA max. standby CMOS**
- **Up to 10,000 Erase/Write Cycles Per Register**
- **10 Year Data Retention**

PIN CONFIGURATIONS

Plastic Dual-In-line "P" Package



EIAJ Small Outline "J" Package



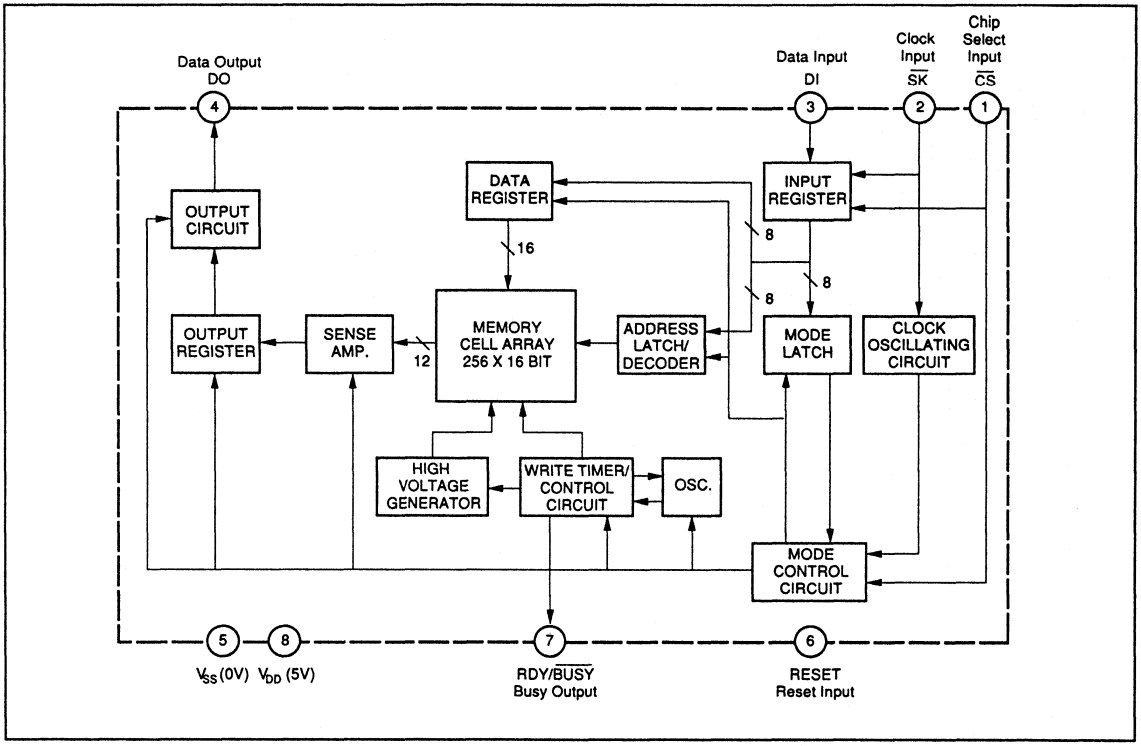
OVERVIEW

The XL90C41 is a 4096-bit, nonvolatile, serial E²PROM. It is fabricated using EXEL's advanced CMOS E²PROM technology. The XL90C41 provides external read/write memory arranged as 256 registers of 16 bits each. Five 8-bit instructions control the operation of the device, which include read, write, enable and status functions. The XL90C41 has been designed for applications requiring up to 10,000 erase/write cycles per register. In the standby mode, the XL90C41 reduces power consumption by more than 80%, compared to an NMOS counterpart.

PIN NAMES

$\overline{\text{CS}}$	Chip Select
$\overline{\text{SK}}$	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
RESET	Reset Input
R/$\overline{\text{B}}$	READY/$\overline{\text{BUSY}}$ Output
Vcc	Power Supply

BLOCK DIAGRAM



APPLICATIONS

The XL90C41 is ideal for high volume applications requiring low density data storage. It uses a low cost, space saving 8-pin package, and readily interfaces with standard microprocessors and popular microcontrollers such as the 8048/49/51/96, the COP4XX series, the 6801/05, the TMS1000 and the Z8.

Candidate applications include alarm devices, appliances, computer terminals and smart cards, electronic locks, meters, robotics and telephone, to name just a few.

ENDURANCE AND DATA RETENTION

The XL90C41 is designed for applications requiring up to 10,000 write cycles per bit. It provides 10 years of secure data retention, with or without power applied.

DEVICE OPERATION

The XL90C41 is a clocked serial port compatible E²PROM. Input data is latched on the rising edge of the clock, and data is output on the falling edge of the clock.

Data is grouped in 8-bit bytes. The beginning 8 bits specify the mode, the next 8 bits specify the address, and subsequent 16 bits specify the I/O data.

During the self-timed internal programming cycle that accompanies a write, the $\overline{SK}$ clock is de-activated. It is needed only when instructions or data are being passed to or from the memory.

Any of the six modes (read, write, write enable, write disable, erase all and write all) may be specified. The write time is set by internal timer, and determination of whether a write operation is in progress or not can be made from the status of the READY/$\overline{BUSY}$ pin. When the asynchronous RESET pin is taken HIGH, any ongoing operation is immediately halted.

Read (READ)
The read instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into the output register. The output on DO changes during the HIGH to LOW transition of $\overline{SK}$.

Write (WRITE)
After a write instruction and its address have been decoded, the device expects 16 bits of data. These are to be transferred into the specific memory register which has previously been automatically erased. After the last data bit has been clocked into DI on the 32nd clock edge, the self-timed internal programming cycle is initiated. The write cycle status can be monitored by observing the READY/$\overline{BUSY}$ pin.

Write Enable/Disable (EWEN, EWDS) — When the XL90C41 is powered up, it comes up in the write disabled state. In order to be programmable, it must receive an enable instruction. The device remains programmable until a disable instruction is entered, or until it is powered down. The disable instruction provides protection against inadvertent writes. Read capability is not affected.

Erase All (ERAL)
Full-chip erase is provided for ease in programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1."

Write All (WRAL)
The write all command forces all registers in the memory array to an arbitrary 16-bit pattern. Like the standard write instruction, this instruction is followed by 16-bits of serial data on the DI pin. The erase all command should be entered before forcing write all command.

INSTRUCTION SET

Instruction	Start Bits	OP Code	Address	Input Data
READ	1010	1000	A_0-A_7	
WRITE	1010	0100	A_0-A_7	D_0-D_{15}
Erase/Write Enable (EWEN)	1010	0011	XXXXXXXX	
Erase/Write Disable (EWDS)	1010	0000	XXXXXXXX	
Erase All Registers (ERAL)	1010	0010	XXXXXXXX	
Write All Registers (WRAL)	1010	0001	XXXXXXXX	D_0-D_{15}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -40°C to +70°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin. ..... -0.3 to Vcc + 0.3V
ESD Rating 2000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS90C41 or -40°C to +85°C for XLE90C41, V_{CC} = 5V ±10%

			XLS90C41		XLE90C41		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
I_{CC1}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz CMOS Input Levels		3		3	mA
I_{CC2}	Operating Current	$\overline{CS}$ = V_{IH}, $\overline{SK}$ = 1MHz TTL Input Levels		3		3	mA
I_{CC3}	Standby Current	$\overline{CS}$ = 0V DI = $\overline{SK}$ = PE = Vcc		100, 3*		100, 3*	µA
I_{LI}	Input Leakage	V_{IN} = 0V to Vcc, $\overline{CS}$, $\overline{SK}$, DI		2		2	µA
I_{LO}	Output Leakage	V_{OUT} = 0V to Vcc		2		2	µA
V_{IL}	Input Low Voltage			0.8		0.8	V
V_{IH}	Input High Voltage		2.0		2		V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA TTL	2.4		2.4		V
V_{OH1}	Output High Voltage	I_{OH} = -400µA TTL		0.4		0.4	V
V_{OL2}	Output Low Voltage	I_{OL} = 10µA CMOS		0.2		0.2	V
V_{OH2}	Output High Voltage	I_{OH} = -10µA CMOS	Vcc-0.2		Vcc-0.2		V

* -A = 100µA, -B = 3µA

AC ELECTRICAL CHARACTERISTICS

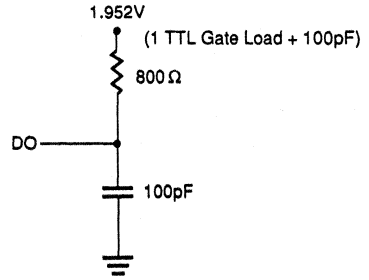
T_A = 0°C to +70°C for the XLS90C41 or -40°C to +85°C for the XLE90C41, V_{CC} = 5V ±10%

			XLS90C41		XLE90C41		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SK}	$\overline{SK}$ Clock Frequency			1		1	MHz
t_{SKH}	$\overline{SK}$ HIGH Time		450		450		ns
t_{SKL}	$\overline{SK}$ LOW Time		450		450		ns
t_{CS}	Minimum $\overline{CS}$ HIGH Time		1		1		µs
t_{CSS}	$\overline{CS}$ Setup Time	Relative to $\overline{SK}$ ⌝	200		200		ns
t_{DIS}	DI Setup Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to $\overline{SK}$ ⌟	0		0		ns
t_{DIH}	DI Hold Time	Relative to $\overline{SK}$ ⌝	150		150		ns
t_{PD1}	Output Delay to "1"	AC Test		350		350	ns
t_{PD0}	Output Delay to "0"	AC Test		350		350	ns
t_{SV}	$\overline{CS}$ to Status Valid	AC Test		1		1	µs
t_{DF}	$\overline{CS}$ to DO in 3-state	$\overline{CS}$ = V_{IL}		400		400	ns
$t_{E/W}$	Write Cycle Time			10		10	ms

CAPACITANCE

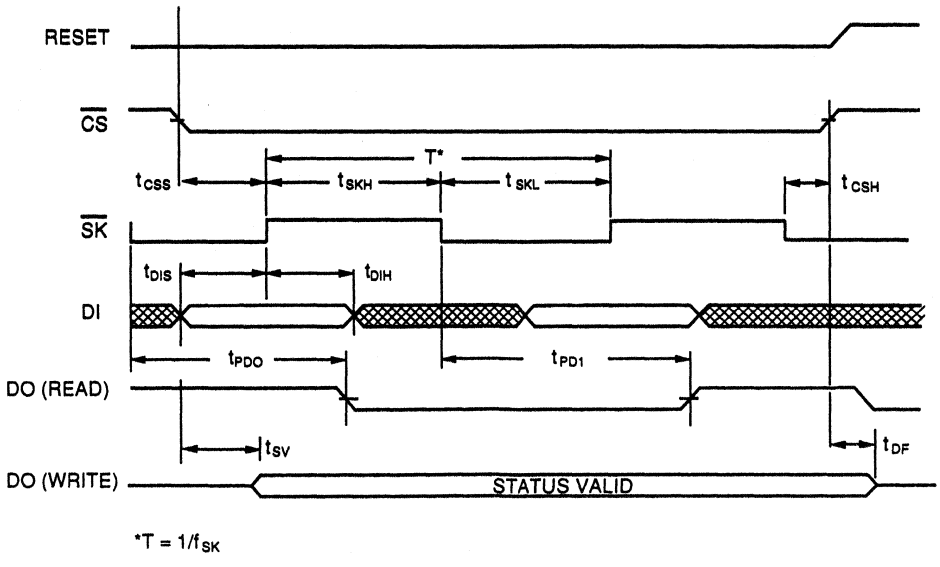
T_A = 25°C, f = 1MHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	5	pF



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

FIGURE 1. AC TEST CONDITIONS



*T = $1/f_{SK}$

FIGURE 2. SYNCHRONOUS DATA TIMING

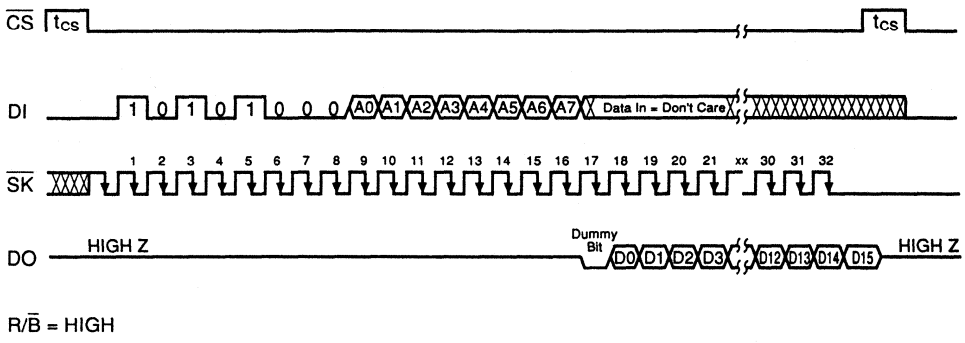


FIGURE 3. READ CYCLE TIMING

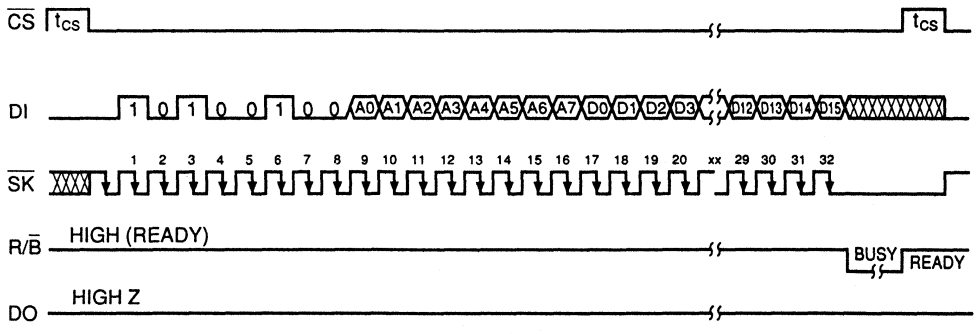


FIGURE 4. WRITE CYCLE TIMING

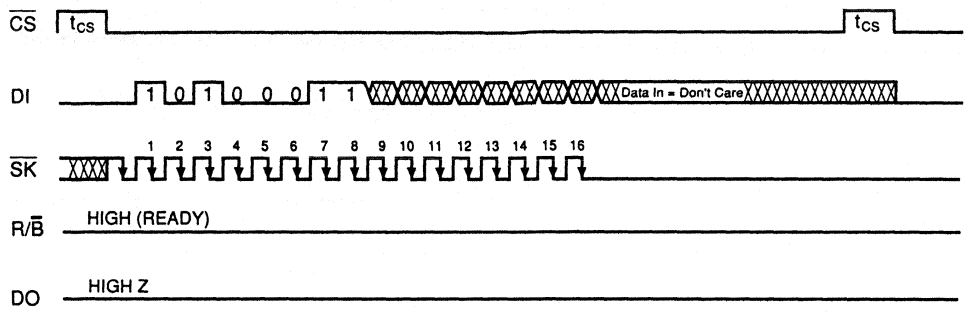


FIGURE 5. WRITE ENABLE (EWEN) CYCLE TIMING

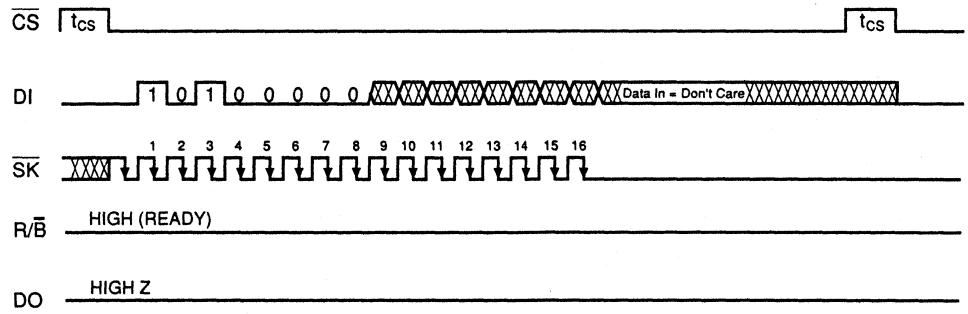


FIGURE 6. WRITE DISABLE (EWDS) CYCLE TIMING

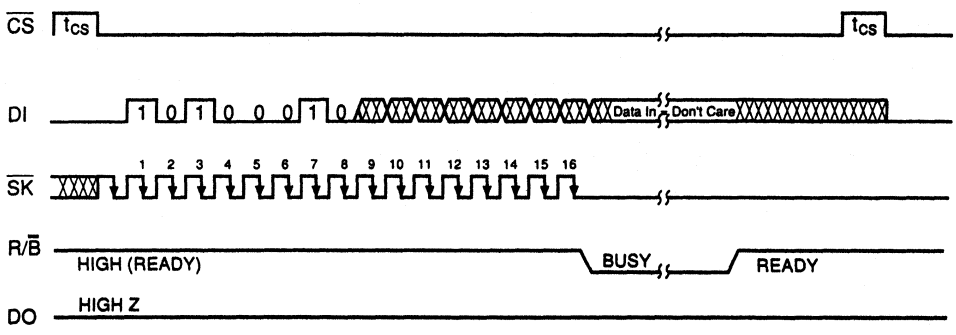


FIGURE 7. ERASE ALL (ERAL) CYCLE TIMING

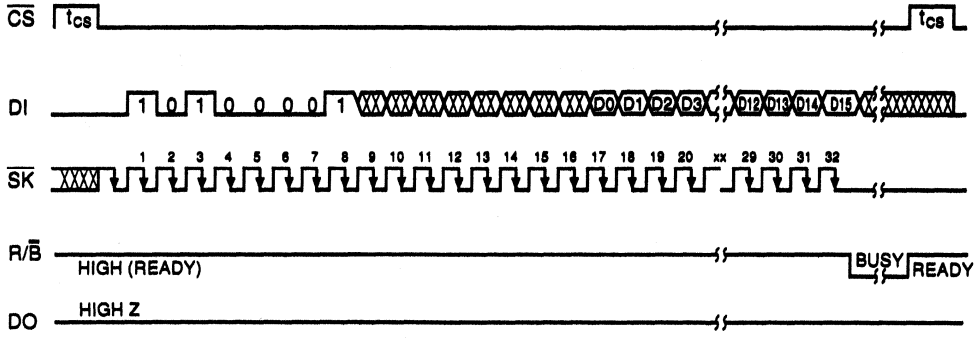


FIGURE 8. WRITE ALL (WRAL) CYCLE TIMING

SECTION 3 Table of Contents

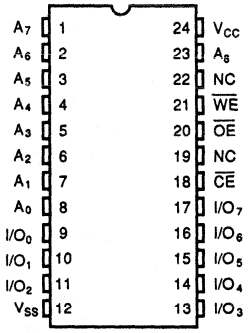
512 X 8 Electrically Erasable PROM

FEATURES

- **Fast Read Access Times**
  — 250ns, 300ns, 350ns, 450ns
- **5 Volt-only Operation**
  — Including Write
- **Fast Nonvolatile Write Cycle**
  — Internally Latched Data and Address
  — 10ms Nonvolatile Write Cycle
- **Automatic Erase Before Write**
- **Automatic Write Timeout**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**

PIN CONFIGURATION

24 Pin PDIP
Type "P" Package



PIN NAMES

A_0-A_8	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

OVERVIEW

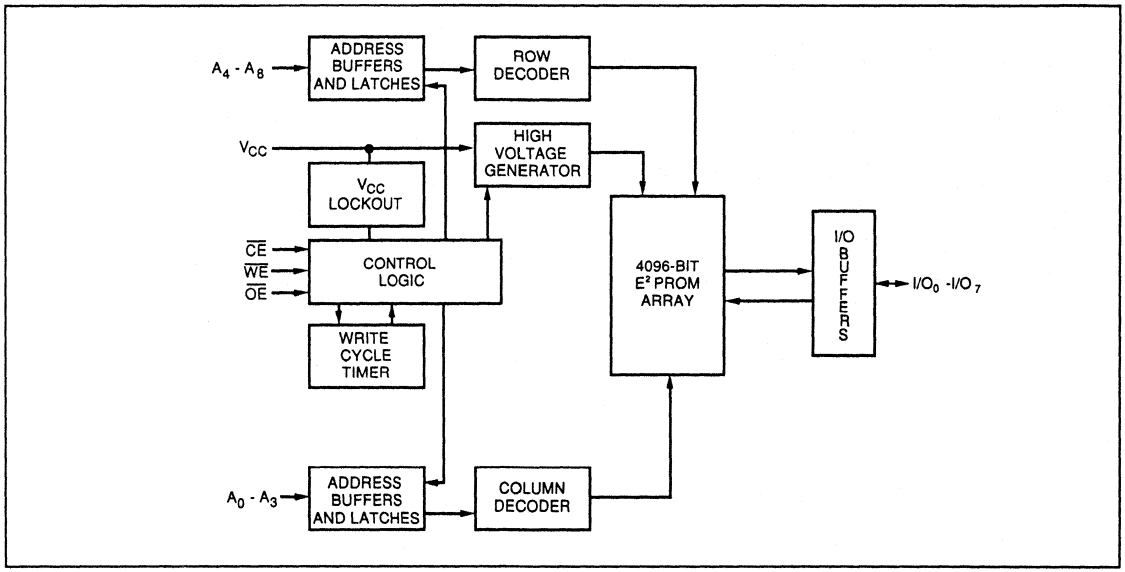
The XL2804A is a full-featured, 512 x 8 bit E^2PROM (Electrically Erasable Programmable Read Only Memory). Read access times are as low as 250ns; standby current, less than 40mA. The device is fully functional with a single 5V power supply, and the XL2804A is manufactured with EXEL's 2.5µ NMOS E^2PROM process.

The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

The XL2804A features $\overline{OE}$ write inhibit logic and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The XL2804A is compatible with industrial standard 512 x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

BLOCK DIAGRAM



APPLICATIONS

The XL2804A provides secure and reliable data storage thoughout your system's lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2804A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2804A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2804A is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION-STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2804A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2804A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode
In the XL2804A the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL2804A will automatically erase the selected byte and write the new data in less than 10ms. The system is therefore freed to proceed with other operations while the XL2804A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress. (See Figures 3 and 4.)

Output Disable Mode
If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a HIGH impedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a HIGH impedance state. Standby power dissipation is less than 40mA with TTL level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding the data on the I/O pins HIGH. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

WRITE PROTECT MECHANISMS

The XL2804A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{OE}$ Write Disable
If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table below.

Noise Protection
Write pulses of less than 20ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓_⊓	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊓_⊓	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IH}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -10°C to +85°C
Storage Temperature ..... -65°C to +120°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.5V to Vcc + 0.3V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V±5% unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		80	mA
I_{SB}	V_{CC} Current-Standby (TTL)	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		40	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.25V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.25V		±10	µA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_H	High Voltage for Chip Erase		15	18	V

CAPACITANCE

T_A = +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C, V_{CC} = 5V±5%, unless otherwise specified.

Symbol	Parameter	XL2804A-250 Limits		XL2804A-300 Limits		XL2804A-350 Limits		XL2804A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		100		120		135		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	70	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)

T_A = 0°C to +70°C, V_{CC} = 5V±5%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	70		ns
t_{CS}	Chip Enable or Write Setup Time	0		ns
t_{CH}	Chip Enable or Write Hold Time	0		ns
t_{CW}	Chip Enable to End of Write Input	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}	Write Enable Pulse Width	150		ns
t_{WPH}	Write Pulse Recovery	50		ns
t_{DV}	Data Valid Time		1	µs
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{INIT}	Power-up Initialization Period		20	ms

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

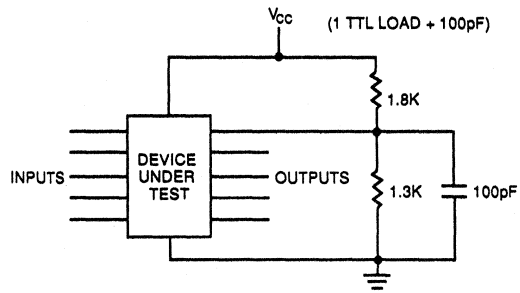


FIGURE 1. AC TEST CONDITIONS

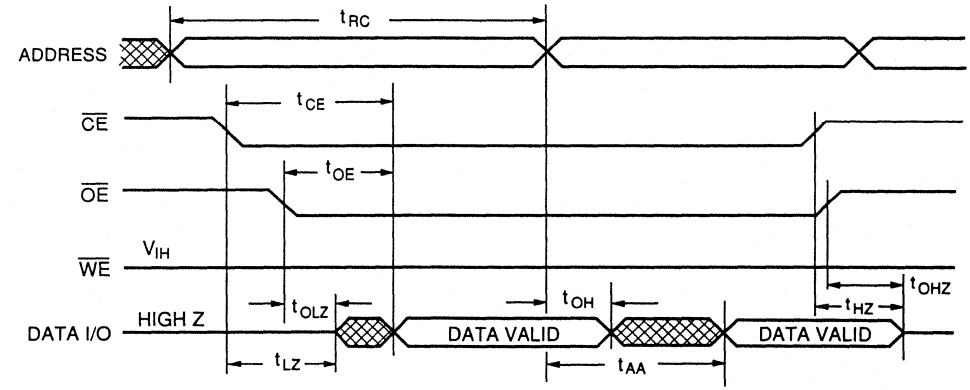


FIGURE 2. READ CYCLE TIMING

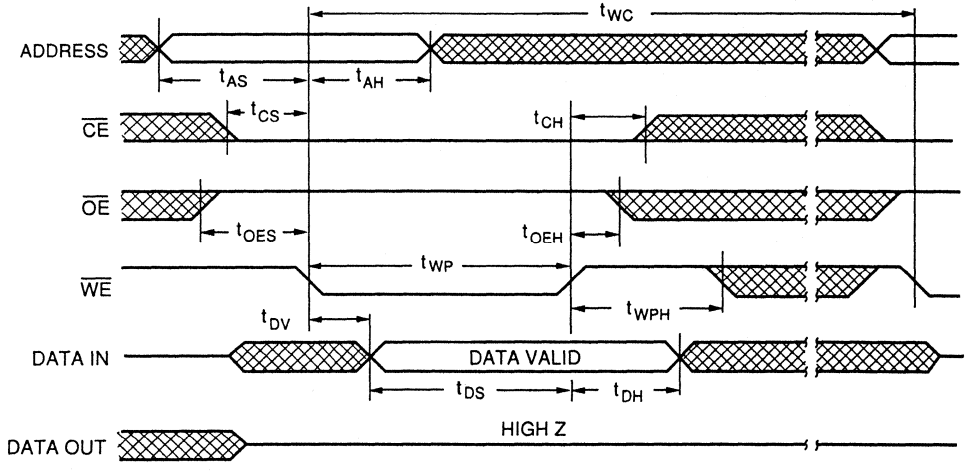


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

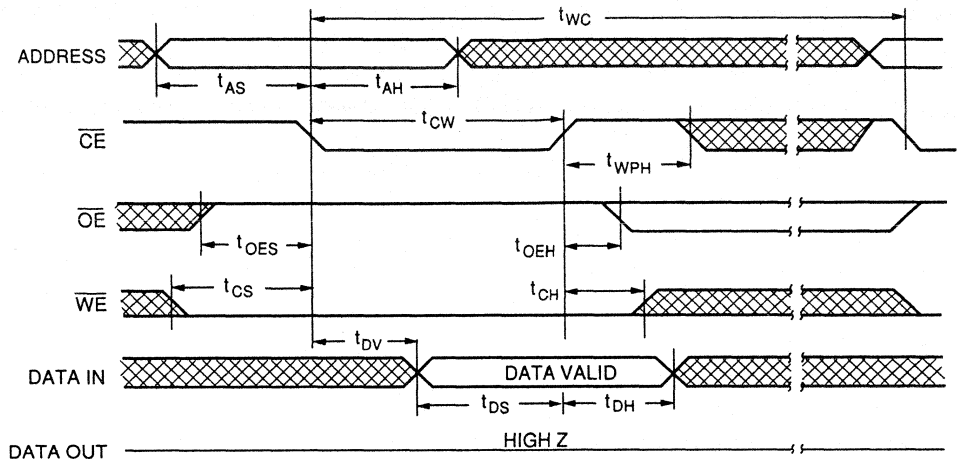


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

2K X 8 Electrically Erasable PROM

FEATURES

- **Fast Read Access Times**
  — 250ns, 300ns, 350ns, 450ns
- **5 Volt-only Operation**
  — Including Write
- **Industrial Temperature Range Available (XLE2816A)**
- **Fast Nonvolatile Write Cycle**
  — Internally Latched Data and Address
  — 10ms Nonvolatile Write Cycle
- **Automatic Erase Before Write**
- **Automatic Write Timeout**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**

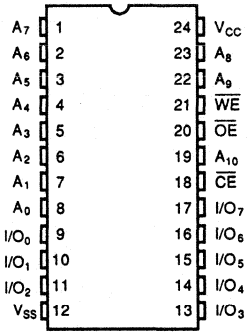
OVERVIEW

The XL2816A is a full-featured, 2K x 8 bit E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices, and it offers improved speed and power efficiency. Read access times are as low as 250ns; standby current, less than 40mA. The device is fully functional with a single 5V power supply, and the XL2816A is manufactured with EXEL's 2.5μ NMOS E²PROM process.

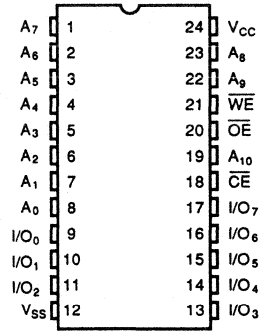
The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

PIN CONFIGURATION

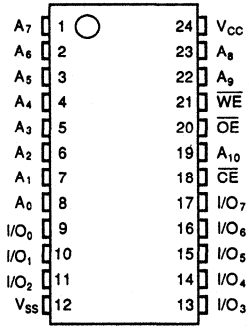
24 Pin PDIP
Type "P" Package



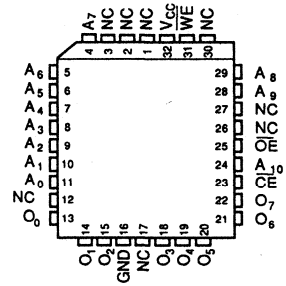
24 Pin CERDIP
Type "C" Package



Small Outline
Type "J" Package



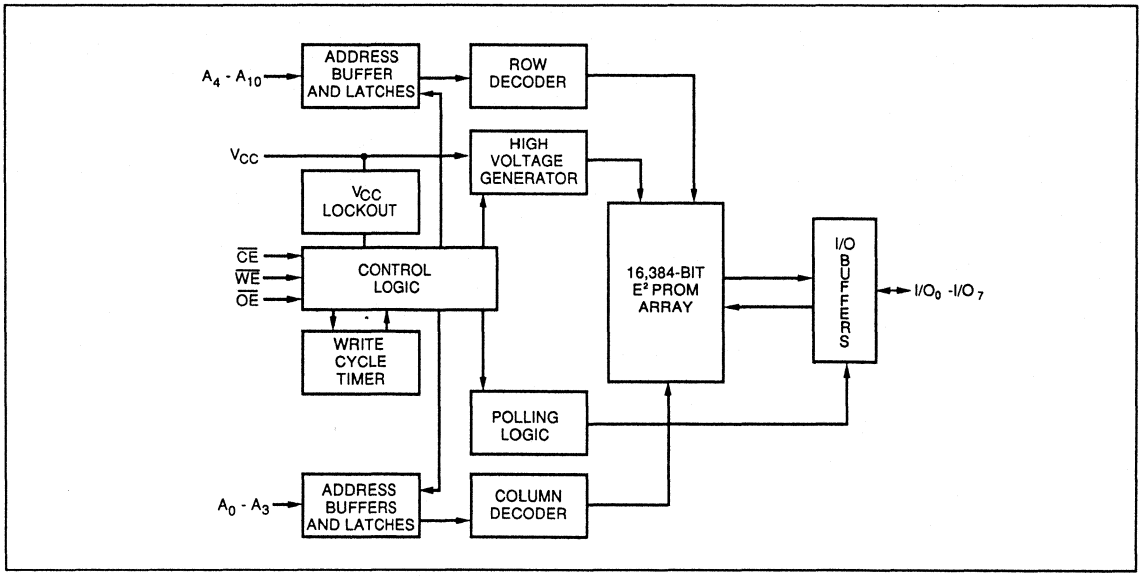
32 Pin PLCC
Type"D" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The XL2816A features $\overline{OE}$ write inhibit logic and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The XL2816A is compatible with industrial standard 2K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL2816A provides secure and reliable data storage thoughout your system's lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2816A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2816A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2816A is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION-STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2816A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2816A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode
In the XL2816A the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL2816A will automatically erase the selected byte and write the new data in less than 10ms. The system is therefore freed to proceed with other operations while the XL2816A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress with the exception of I/O_7 if a read command is asserted. (See monitoring device status in the next column of this page.) (See Figures 3 and 4.)

Output Disable Mode
If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought high, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 40mA with TTL level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding the data on the I/O pins HIGH. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL2816A, a status indicator has been incorporated to provide for the system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL2816A until it determines a simple logical condition.

WRITE PROTECT MECHANISMS

The XL2816A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuit is built in.

$\overline{OE}$ Write Inhibit
If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will be inhibited.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓_⊓	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊓_⊓	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature. ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.5V to +6.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +75°C for the XLS2816A or -40°C to +85°C for the XLE2816A, V_{CC} = 5V±5%

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	V_{CC} Current — Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		110	mA
I_{SB}	V_{CC} Current — Standby (TTL)	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		40	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.25V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.25V		10	µA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_H	High Voltage for Chip Erase		15	18	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +75°C for the XLS2816A or -40°C to +85°C for the XLE2816A, V_{CC} = 5V±5%

Symbol	Parameter	XL2816A-250 Limits		XL2816A-300 Limits		XL2816A-350 Limits		XL2816A-450 Limits		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		100		120		135		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	70	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)

T_A= 0°C to +75°C for the XLS2816A or -40°C to +85°C for the XLE2816A, V_{CC} = 5V±5%

Symbol	Parameter	Min	Max	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	70		ns
t_{CS}	Chip Enable or Write Enable Setup Time	0		ns
t_{CH}	Chip Enable or Write Enable Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}	Write Enable Pulse Width	150		ns
t_{WPH}	Write Recovery Time	50		ns
t_{DV}	Data Valid Time		1	µs
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{INIT}	Power-up Initialization Period		20	ms

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

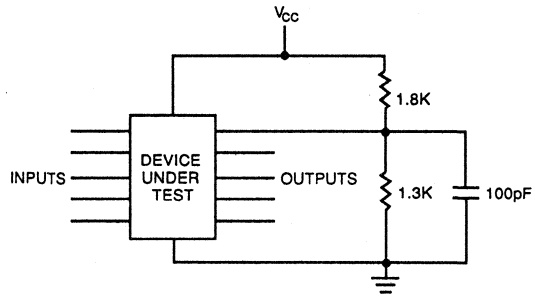


FIGURE 1. AC TEST CONDITIONS

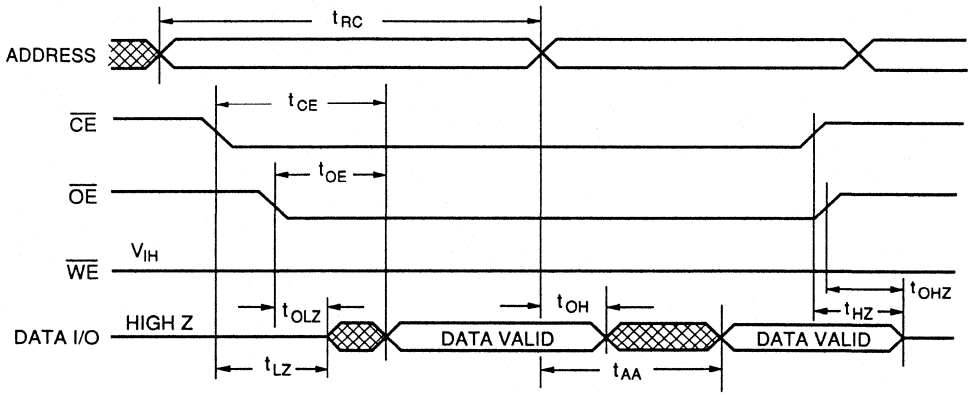


FIGURE 2. READ CYCLE TIMING

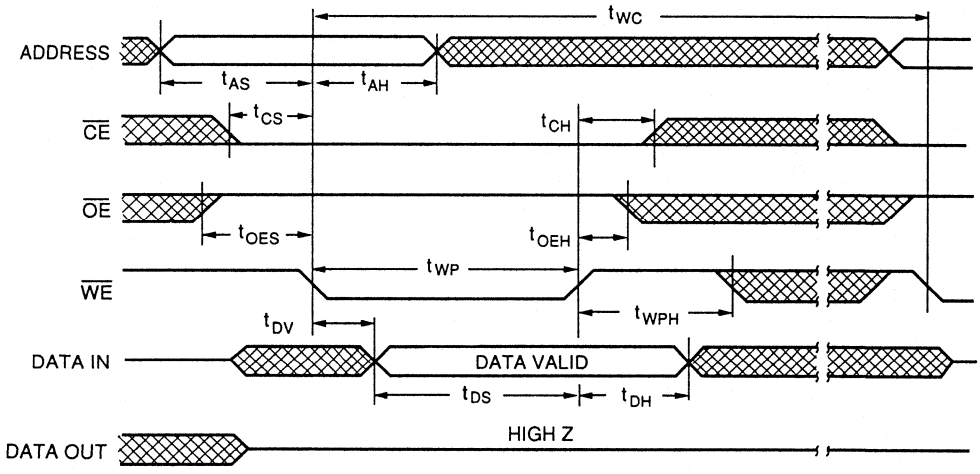


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

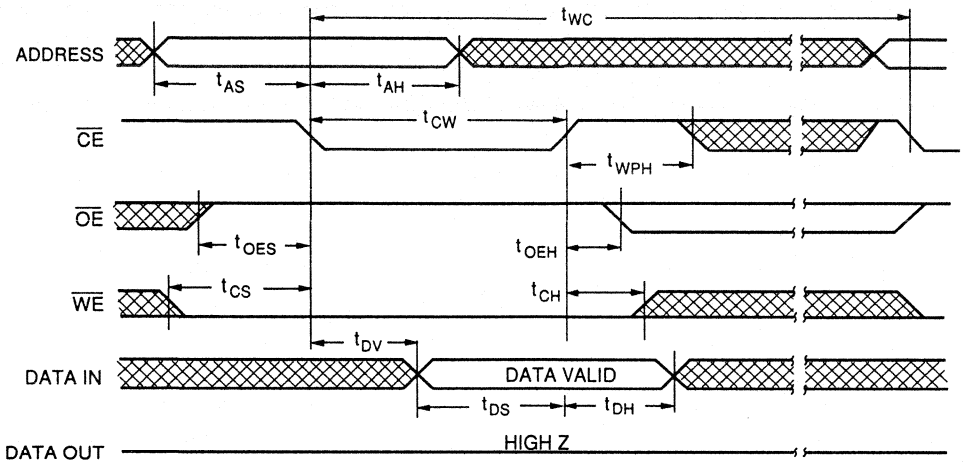


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

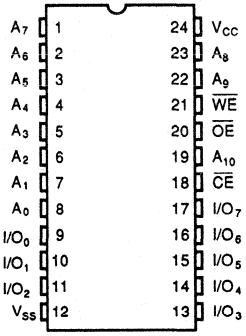
2K X 8 CMOS Electrically Erasable PROM

FEATURES

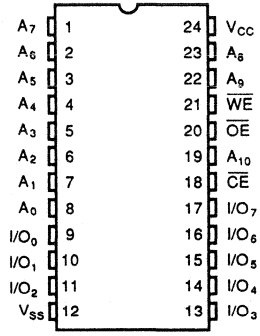
- **Fast Read Access Times**
  - **— 100ns, 150ns, 200ns, 250ns**
- **Low CMOS Power Consumption**
  - **— 30mA active (max.)**
  - **— 100µA standby (max.)**
- **5 Volt-only Operation**
  - **— Including Write**
- **Industrial Temperature Range Available (XLE28C16A)**
- **Fast Nonvolatile Write Cycle**
  - **— Internally Latched Data and Address**
  - **— 5ms Nonvolatile Write Cycle**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling To Minimize Write Cycle Times**
- **Reliable Floating Gate CMOS Technology**

PIN CONFIGURATION

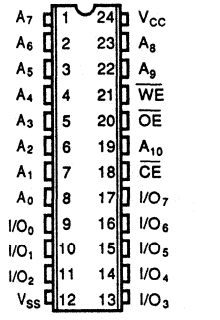
24 Pin PDIP
Type "P" Package



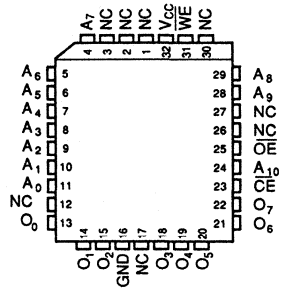
24 Pin CERDIP
Type "C" Package



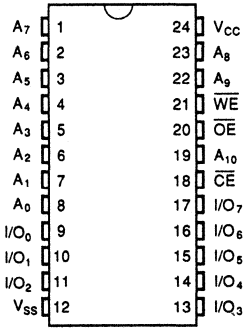
24 Pin Skinny DIP
Type "P3" Package



32 Pin PLCC
Type"D" Package



Small Outline
Type "J" Package



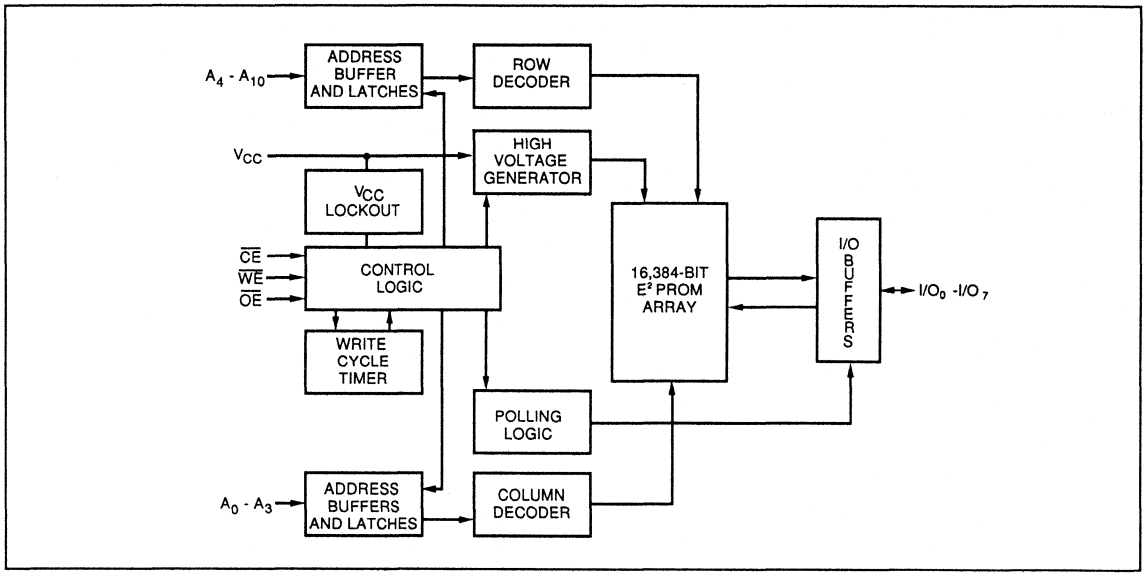
OVERVIEW

The XL28C16A is a full-featured, 2K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices, and it offers improved speed and power efficiency. Read access times are as low as 100ns; standby current, less than 100µA. The device is fully functional with a single 5V power supply, and the XL28C16A is manufactured with EXEL's 1.5m CMOS E²PROM process.

PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.The XL28C16A features V_{CC} lockout, power-on reset and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The XL28C16A is compatible with industrial standard 2K x 8 E²PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E²PROMS as well.

APPLICATIONS

The XL28C16A provides secure and reliable data storage thoughout your system's lifetime, both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL28C16A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL28C16A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C16A is designed for applications requiring up to 10,000 data changes per E²PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION-STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C16A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E²PROM standards.

Read Mode

Data is read from the XL28C16A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode

In the XL28C16A, the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both addresses and data are latched in a brief 90ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL28C16A will automatically erase the selected byte and write the new data in less than 5ms. The system is therefore freed to proceed with other operations while the XL28C16A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress, with the exception of I/O_7, if a read command is asserted. (See monitoring device status in the next column of this page.) (See Figures 3 and 4.)

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Standby Mode

Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 100µA with CMOS level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase

The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O pins high. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL28C16A, a status indicator has been incorporated to provide for the system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL28C16A until it determines a simple logical condition.

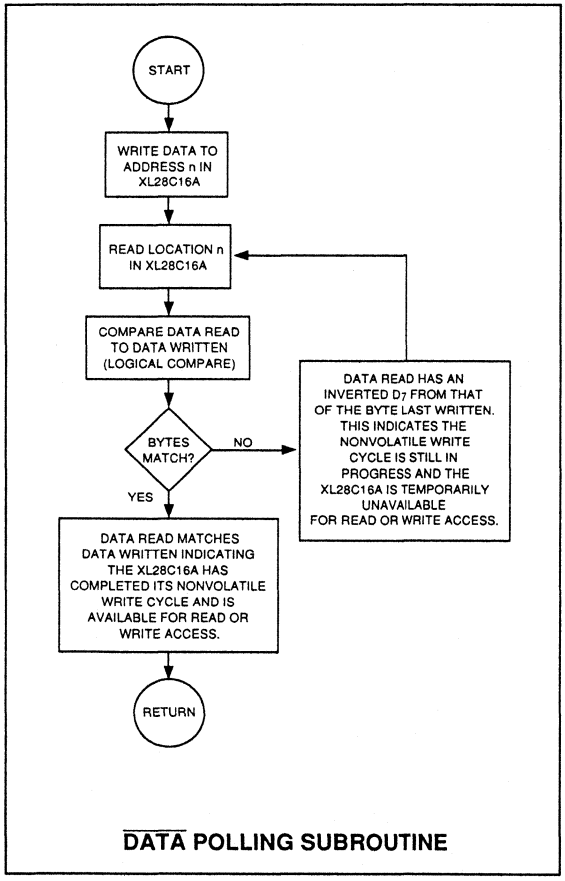
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾_‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾_‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details.

$\overline{\text{DATA}}$ Polling

The XL28C16A provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C16A is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile cycle timing.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C16A. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C16A. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O_7. I/O_7 is set to output the **complement** of the value of the MSB of the last byte written to the XL28C16A when a read command is asserted.

The procedure is quite simple. The system reads the location last written to in the XL28C16A and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C16A is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing eliminating the need to await the 5ms (max.) period specified and enabling accelerated device loading operations.

WRITE PROTECT MECHANISMS

The XL28C16A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{\text{OE}}$ Write Disable

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 20ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.6V to +7.0V
Voltage on $\overline{OE}$ Pin* ..... -0.6V to +15V
ESD Rating 2000V
DC Output Current 5mA

*With respect to ground

NOTE:Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C16A or -40°C to +85°C for the XLE28C16A, V_{CC} = 5V±10%

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	V_{CC} Current-Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} WE = V_{IH} I/O's = open A_0 -A_{12} = toggling f = 5 MHz		30	mA
I_{SB}	V_{CC} Current-Standby (TTL)	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0 -A_{12} = V_{CC}		2	mA
I_{SBC}	V_{CC} Current Standby (CMOS)	$\overline{CE}$ ≥ V_{CC}-0.2 $\overline{OE}$ ≤ 0.2 I/O's = open A_0 -A_{12} ≥V_{CC}-0.2		100	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}	-10	10	µA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA I_{OH} = -10 µA	2.4 V_{CC}-0.1		V V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)
T_A = 0°C to +70°C for the XLS28C16A or -40°C to +85°C for the XLE28C16A, V_{CC} = 5V±10%

Symbol	Parameter	XL28C16A-100 Limits		XL28C16A-150 Limits		XL28C16A-200 Limits		XL28C16A-250 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	100		150		200		250		ns
t_{AA}	Address Access Time		100		150		200		250	ns
t_{CE}	Chip Enable Access Time		100		150		200		250	ns
t_{OE}	Output Enable Access Time		70		80		90		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	0	60	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	50	0	50	0	60	ns
t_{OH}	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 3, 4, 5)
T_A = 0°C to +70°C for the XLS28C16A or -40°C to +85°C for the XLE28C16A, V_{CC} = 5V±10%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
t_{WP}*	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Write Inhibit Period After Power-Up		20	ms

* NOTE: A write pulse of less than 20ns will not initiate a write cycle.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

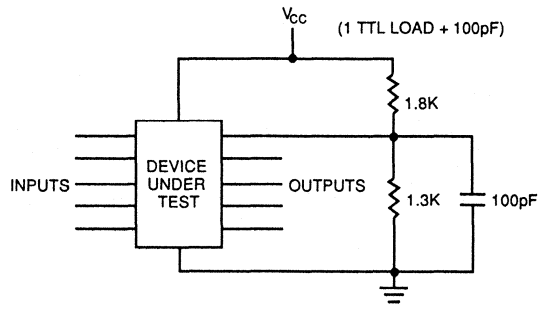


FIGURE 1. AC TEST CONDITIONS

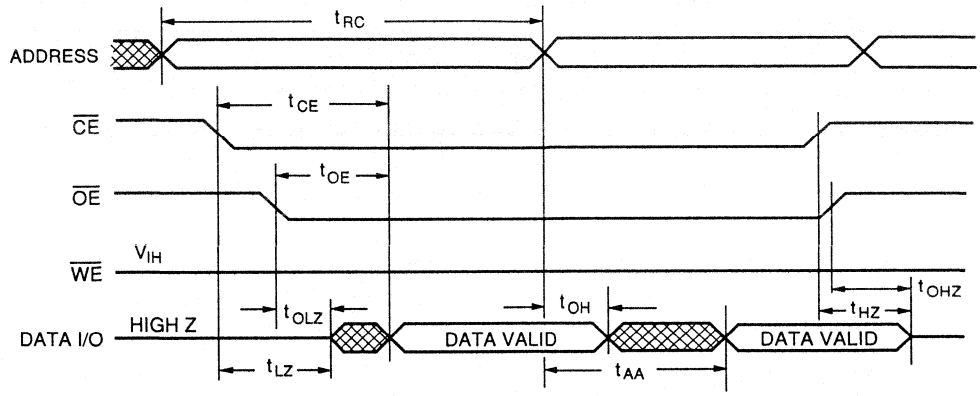


FIGURE 2. READ CYCLE TIMING

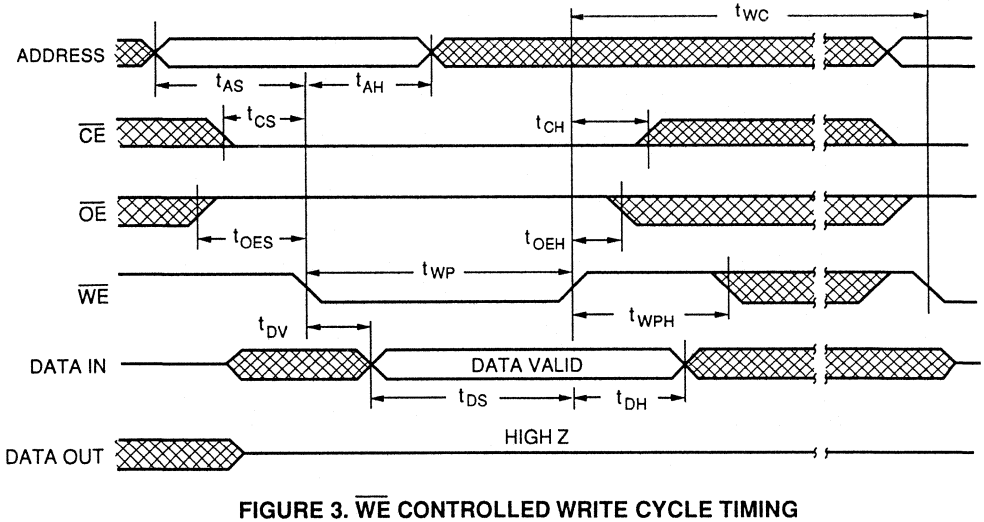


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

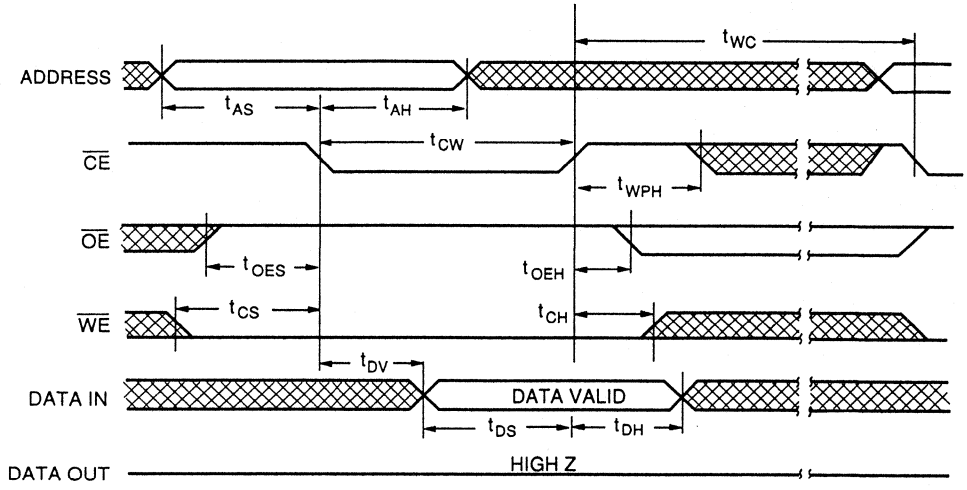
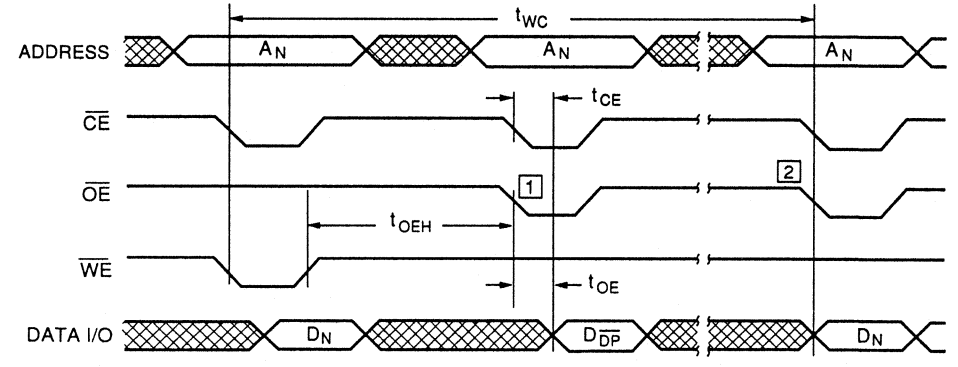


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL28C16A indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

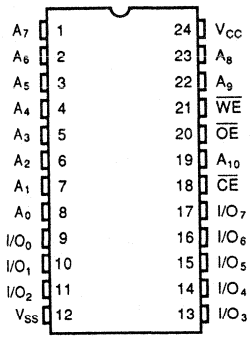
2K X 8 CMOS Electrically Erasable PROM

FEATURES

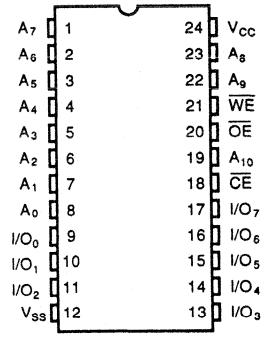
- **Fast Read Access Times**
  - **— 100ns, 150ns, 200ns, 250ns**
- **Low CMOS Power Consumption**
  - **— 30mA active (max.)**
  - **— 100µA standby (max.)**
- **5 Volt-only Operation**
  - **— Including Write**
- **Industrial Temperature Range Available (XLE28C16B)**
- **Fast Nonvolatile Write Cycle**
  - **— Internally Latched Data and Address**
  - **— 120ns Byte-load Cycle**
  - **— 5ms Nonvolatile Write Cycle**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling To Minimize Write Cycle Times**
- **Reliable Floating Gate CMOS Technology**
- **16 Byte Page Mode**

PIN CONFIGURATION

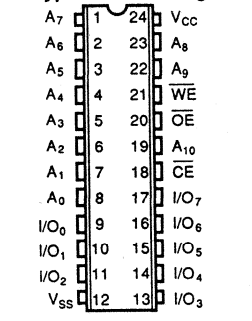
24 Pin PDIP
Type "P" Package



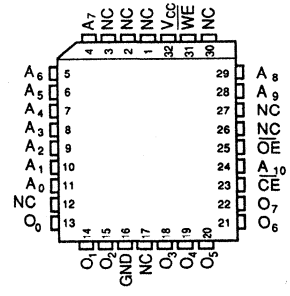
24 Pin CERDIP
Type "C" Package



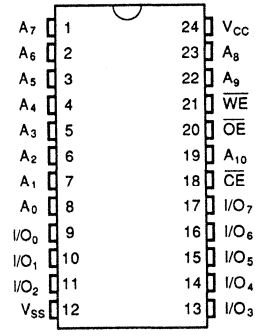
24 Pin Skinny DIP
Type "P3" Package



32 Pin PLCC
Type"D" Package



Small Outline
Type "J" Package



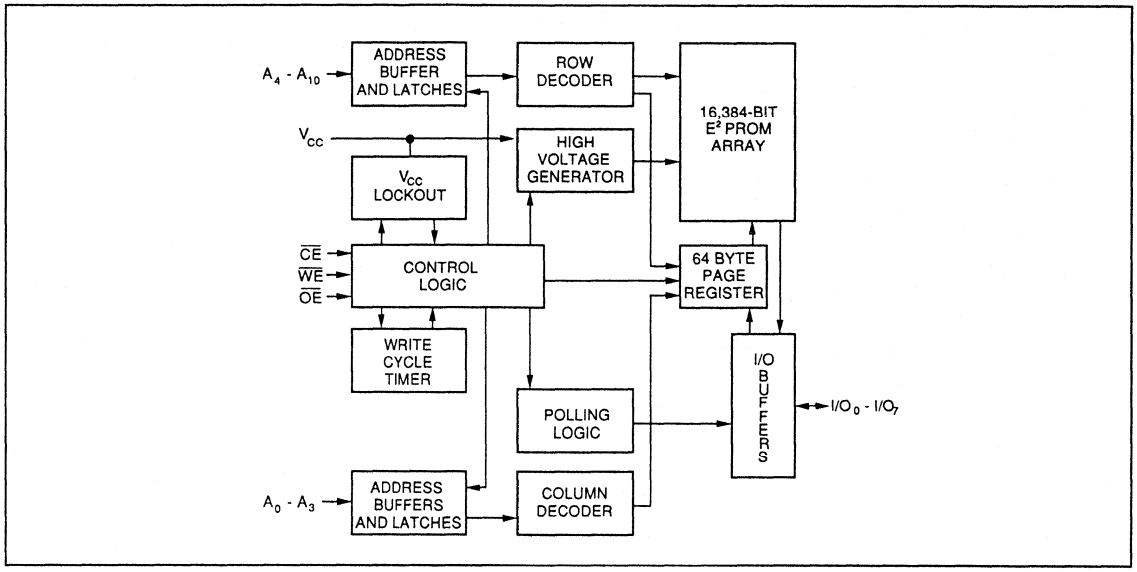
OVERVIEW

The XL28C16B is a full-featured, 2K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices, and it offers improved speed and power efficiency. Read access times are as low as 100ns; standby current, less than 100µA. The device is fully functional with a single 5V power supply, and the XL28C16B is manufactured with EXEL's 1.5µ CMOS E²PROM process.

PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

The XL28C16B features VCC lockout, power-on reset and noise protected $\overline{WE}$, to inhibit inadvertent writes.

The XL28C16B is compatible with industrial standard 2K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL28C16B provides secure and reliable data storage thoughout your system's lifetime, both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL28C16B replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL28C16B is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C16B is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C16B. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode
Data is read from the XL28C16B by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Write Mode
The XL28C16B uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers new entries in the page-buffer to the E^2PROM array.

The XL28C16B contains 128 16-byte pages. Address lines A_4-A_{10} identify the page: lines A_0-A_3 identify the byte within the page. All bytes written within one write cycle must be on the same page (A_4-A_{10} must remain unchanged). Any number of the 16 bytes in the page can be written or re-written, in any order; the last data written is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to trigger the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. A byte-load timer is started on the subsequent rising edge of the controlling line. The timer provides a 75µS window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period. Please note that all write cycles require that $\overline{OE}$ is held HIGH.

When the timer times out, additional byte-load cycles are inhibited and data is automatically transferred from the page buffer to the E^2PROM array during the internal nonvolatile write cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The nonvolatile write cycle is immune to any concurrent control pin activity.

A write-latch is set on the first byte-load of each write cycle. Output pins remain in a high impedance state except during a byte-load (when they contain new input data) or during a $\overline{DATA}$ polling read cycle. When the nonvolatile cycle is completed, the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$). (See Figures 3, 4 and 6.)

Output Disable Mode
If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 100µA with CMOS level inputs. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O inputs high. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL28C16B, a status indicator has been incorporated to provide for the system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL28C16B until it determines a simple logical condition.

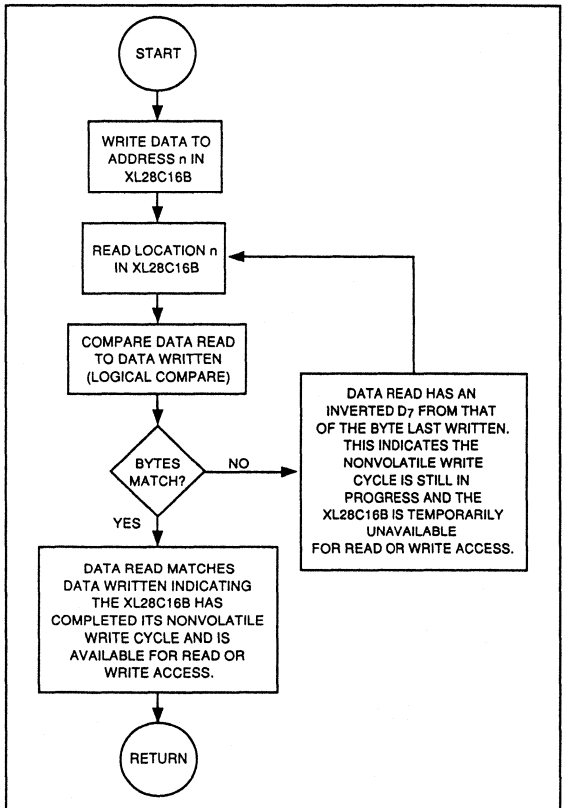
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In=V_{IH}	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL for details

$\overline{\text{DATA}}$ Polling

The XL28C16B provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C16B is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile cycle timing.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C16B. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C16B. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O7. I/O7 is set to output the **complement** of the value of the MSB of the last byte written to the XL28C16B when a read command is asserted.

The procedure is quite simple. The system reads the location last written to in the XL28C16B and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C16B is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing eliminating the need to await the 5ms (max.) period specified and enabling accelerated device loading operations. (See Figure 5.)

WRITE PROTECT MECHANISMS

The XL28C16B features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{\text{OE}}$ Write Inhibit

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -0.6V to +7.0V
Voltage on $\overline{OE}$ Pin* ..... -0.6V to +15V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} WE = V_{IH} I/O's = open A_0-A_{12} = toggling f = 5 MHz		30	mA
I_{SB}	V_{CC} Current-Standby (TTL)	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = V_{CC}		2	mA
I_{SBC}	V_{CC} Current-Standby (CMOS)	$\overline{CE}$ >= V_{CC}-0.2 $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} >= V_{CC}-0.2		100	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}	-10	10	µA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 V_{CC}-0.1		V V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	XL28C16B-100 Limits		XL28C16B-150 Limits		XL28C16B-200 Limits		XL28C16B-250 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	100		150		200		250		ns
t_{AA}	Address Access Time		100		150		200		250	ns
t_{CE}	Chip Enable Access Time		100		150		200		250	ns
t_{OE}	Output Enable Access Time		70		80		90		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	0	60	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	50	0	50	0	60	ns
t_{OH}	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 3, 4, 5 and 6)

T_A = 0°C to +70°C for the XLS28C16B or -40°C to +85°C for the XLE28C16B, V_{CC} = 5V±10%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{BLC}	Byte Load Cycle	.120	100	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
*t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

* Note: A write pulse of less than 10ns will not initiate a write cycle.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

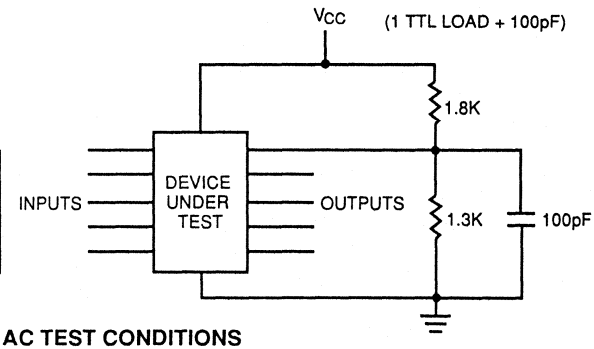


FIGURE 1. AC TEST CONDITIONS

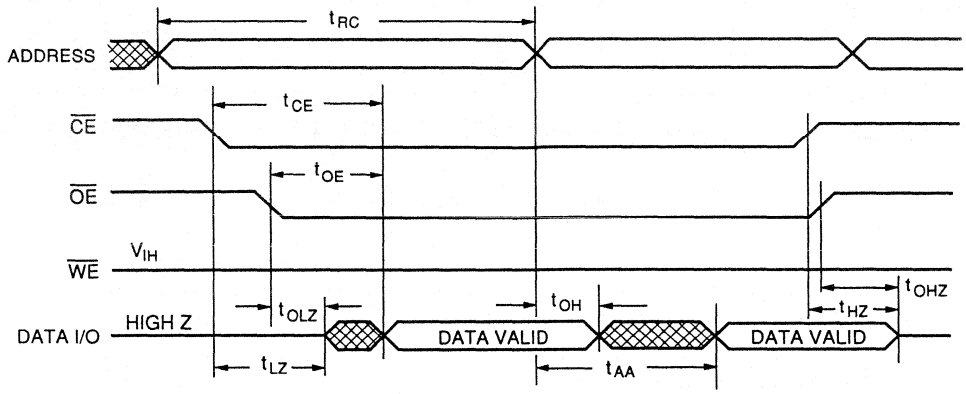


FIGURE 2. READ CYCLE TIMING

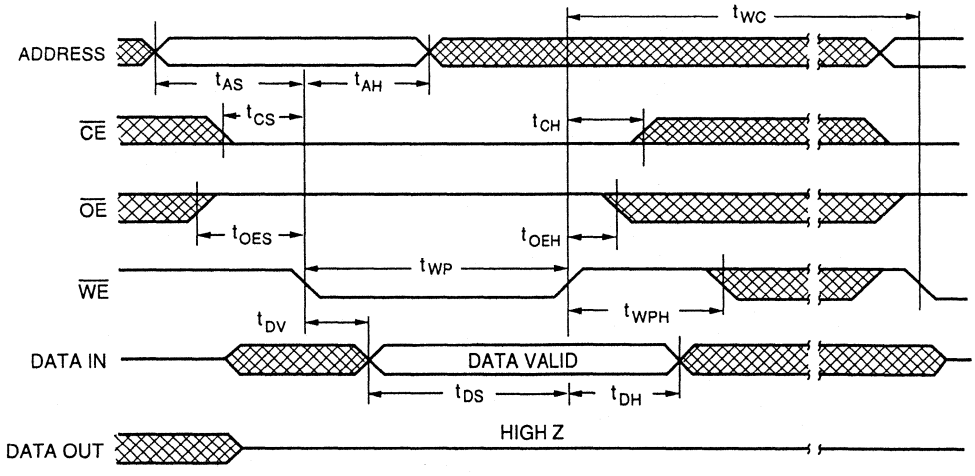


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

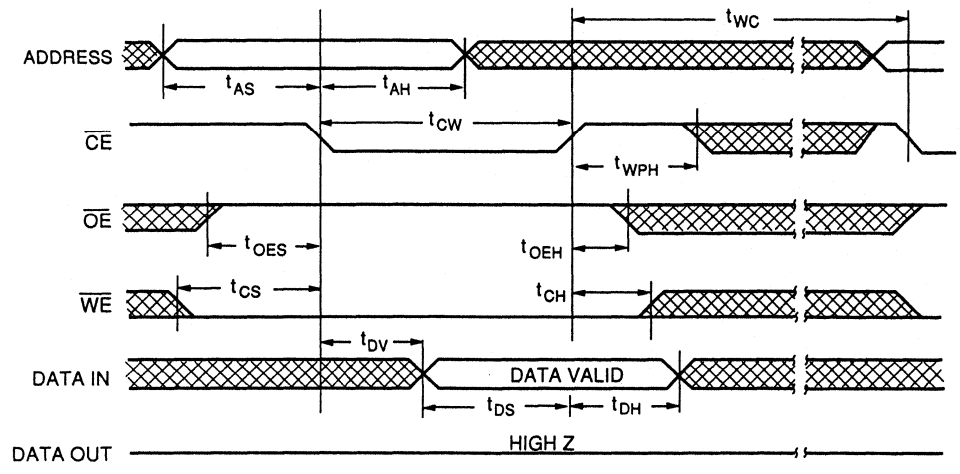
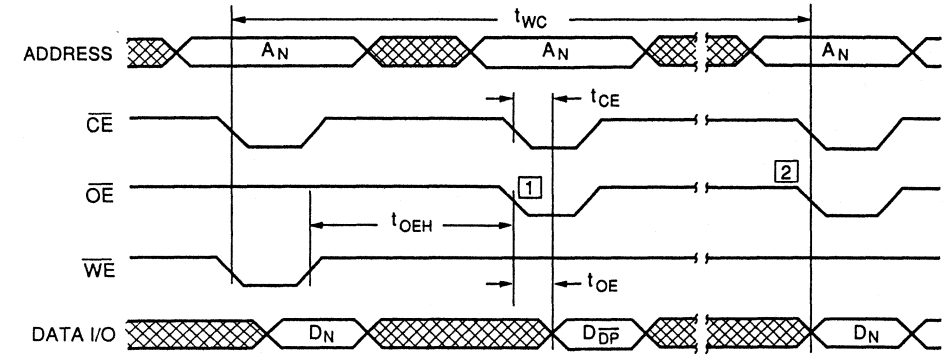


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL28C16B indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

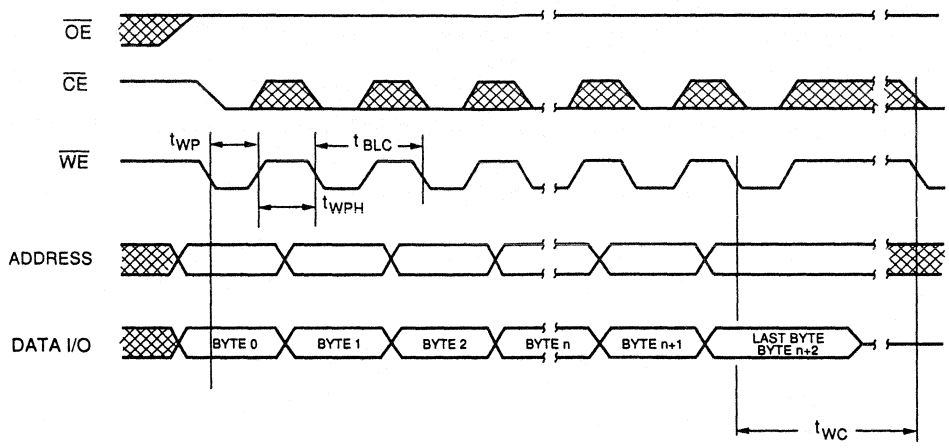


FIGURE 6. PAGE MODE WRITE CYCLE TIMING

2K X 8 High Speed CMOS Electrically Erasable PROM

FEATURES

- 2048 x 8 Bit CMOS E^2PROM
- High Speed Read Access
  - — 55ns, 60ns, 70ns, 85ns
- Bipolar PROM Socket Compatibility
- Electrically Reprogrammable
  - — Program Voltage: 10.8 - 20.5V
- Fast Byte Write: 5ms
- TTL Compatible Inputs and Outputs
- Static — No Clocks Required
- Low Current Requirements
  - — 90mA active (max.)
  - — 45mA standby (max.)
  - — 110mA programming (max.)
- 10 Year Data Retention
- 100% Factory Tested Programmability
- PROM Programmer Support Available

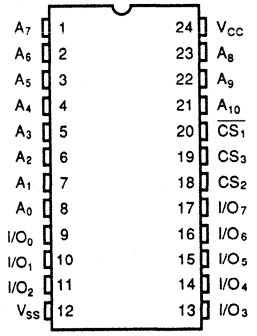
OVERVIEW

The XL46C15 is a 2K x 8 bit CMOS electrically erasable programmable read only memory (E^2PROM) offering unprecedented data access speed. The device is packaged to conform to the JEDEC-approved 24-pin configuration for 2K x 8 bit bipolar PROMs.

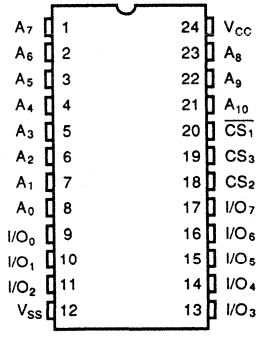
Through the application of revolutionary design techniques, this versatile low power device is able to provide data access times competing with those of bipolar PROMs. Complete PROM compatibility is provided in both read and standby modes allowing this E^2PROM to replace bipolar PROMs in existing sockets. The key user limitations of bipolar PROM technology, such as one-time programmability and high power requirements, are overcome by the XL46C15. In addition to being an attractive PROM replacement in existing systems, the XL46C15 also opens up a whole new domain of design possibilities.

PIN CONFIGURATIONS

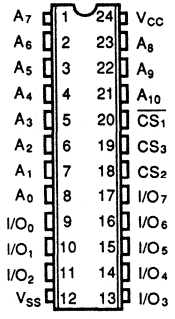
24 Pin PDIP
Type "P" Package



24 Pin CERDIP
Type "C" Package



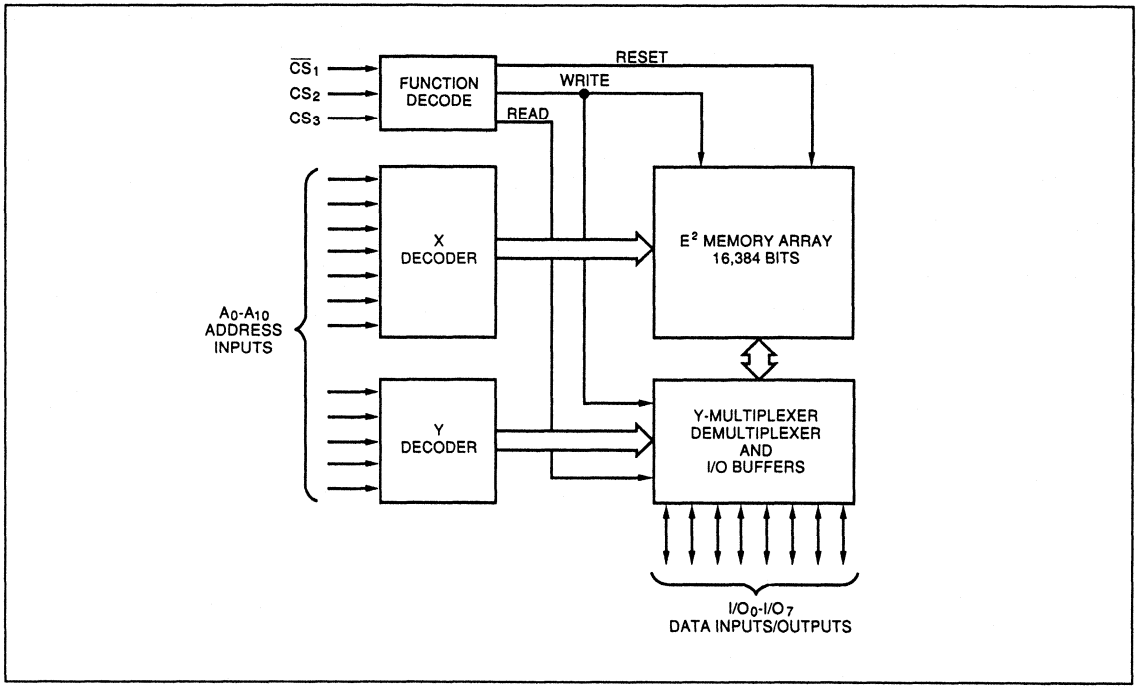
24 Pin Skinny DIP
Type "P3" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CS}_1$, CS_2, CS_3	Chip Select Inputs
V_{CC}	+5V Supply
V_{SS}	Ground

BLOCK DIAGRAM



Unprecedented E²PROM applications are now possible since this CMOS E²PROM combines the advantages of bipolar access speeds, low CMOS power needs and nonvolatile data alterability. Typical applications include high speed process controllers, environmentally adaptive robotics, programmable character generators and user programmable video display pattern generators. EXEL high speed E²PROMs can replace system combinations of high speed static RAM and nonvolatile storage used in read mostly environments.

In existing bipolar PROM applications, the CMOS XL46C15 reduces active and standby power requirements substantially. The reprogrammable nature of E²PROM technology provides the ideal prototyping tool for PROM applications and allows cost effective in-field code updates without requiring the removal and replacement of one time programmable PROMs.

DEVICE OPERATION

Read

Data is read from the XL46C15 with a bipolar PROM compatible read cycle. This read cycle is initiated by applying a LOW to $\overline{CS}_1$, a HIGH to CS_2 and a HIGH to CS_3. Data is available within t_{AA} from the time that the address inputs are valid, or t_{CS} after the last chip select input is asserted, whichever is later. When any of the chip select control inputs are not asserted, the I/O pins remain in a high impedance state to eliminate system bus contention.

Programming Mode

The XL46C15 uses a complementary cell technique to obtain high speed data access. The complementary cells are programmed in a two stage process. The first stage is a chip reset cycle which brings both halves of every cell in the memory to a HIGH level. This cycle completes in a maximum of 50ms. The second stage is the write cycle during which each byte is individually addressed and written.

Both of these cycles are performed with $\overline{CS}_1$ at VPP (10.8V to 20.5V). This ensures high data integrity when the device is used in a 5V-only PROM socket yet allows easy rewrites when the device is placed in a PROM programmer or supplied with a high voltage signal.

Chip Reset Cycle

The chip reset cycle is executed by applying V_{PP} to $\overline{CS}_1$ and a HIGH (V_{IH}) to CS_2 (see Figure 3). During the chip reset cycle both halves of each complementary cell in the memory array are set to a logic "1." Since a bit is read by comparing the voltage difference between the two halves of the cell through a differential amplifier, any data read after a chip reset cycle but before a write cycle to the addressed location will be arbitrary and invalid. Once the chip is reset, the memory is ready to be written.

Byte Write Cycle

A byte may not be rewritten without first resetting the chip. Initially, and after each chip reset operation, all bits are in an indeterminate state and are prepared for programming. A byte write cycle is executed by applying V_{PP} to $\overline{CS}_1$ and a LOW (V_{IL}) to CS_2 while holding valid address and data values constant for a minimum t_{WP} specification (see Figure 4). Since a high voltage supply is required for data alteration, the device will operate as a read only memory in a 5V-only environment.

Standby Mode

Power consumption is reduced by 50% when the device is deselected. Applying a HIGH to $\overline{CS}_1$, a LOW to CS_2, or a LOW to CS_3 puts the device in standby mode. Power consumption is further reduced in a CMOS environment when the address inputs are held at V_{CC} or V_{SS}.

Endurance

The XL46C15 is designed for applications requiring up to 100 write cycles per byte. Contact EXEL for special screening to higher levels of endurance.

PROGRAMMER SUPPORT

Many PROM and EPROM programmer manufacturers are supporting the XL46C15. Please contact EXEL for a list of qualified programmers.

MODE SELECTION

$\overline{CS}_1$	CS_2	CS_3	Mode	I/O Pins
V_{IL}	V_{IH}	V_{IH}	Read	D_{OUT}
<6V	V_{IL}	X	Standby	High Z
V_{IH}	X	X	Standby	High Z
<6V	X	V_{IL}	Standby	High Z
V_{PP}	V_{IL}	X	Byte Write	D_{IN}
V_{PP}	V_{IH}	X	Chip Reset	High Z

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... -1.0V to +7.0V
Voltage on Any Pin (Except $\overline{CS_1}$) ..... -1.0V to (V_{CC} +0.5V)
Voltage on $\overline{CS_1}$ Pin ..... -1.0V to +20.5V
ESD Rating 2000V
DC Output Current ..... -70mA

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions	Limits		Units
			Min.	Max.	
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 6mA; V_{CC} = 4.75V		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -2mA; V_{CC} = 4.75V	2.4		V
V_C	Input Clamp Voltage	I_{IN} = -18mA; V_{CC} = 4.75V		-1.0	V
V_{PP}	Program Voltage on $\overline{CS_1}$		10.8	20.5	V
I_{SC}	Output Short Circuit Current[1]	V_{OUT} = 0V; V_{CC} = 5.25V		-70	mA
I_{PP}	VPP Supply Current	WRITE or RESET modes		1.5	mA
I_{IH}	Input Leakage Current — HIGH	V_{IN} = V_{CC} = 5.25V		10	mA
I_{LI}	Input Leakage Current — LOW	V_{IN} = 0V; V_{CC} = 5.25V		-10	mA
I_{LO}	Output Leakage Current	STANDBY mode; V_{CC} = 5.25V V_{OUT} = 0 to 5.5V;		±10	mA
I_{CC}	V_{CC} Current — Active (TTL)	READ mode; t_{RC} = min.		90	mA
I_{SB}	V_{CC} Current — Standby (TTL)	STANDBY mode		45	mA
I_{SBC}	V_{CC} Current — Standby (CMOS)	$\overline{CS_1}$ V_{CC} - 0.2V; CS_2,CS_3 0.2V ; V_{IN} 0.2V or V_{CC} - 0.2V		35	mA

Note:
1. During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

CAPACITANCE

T_A = +25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Operating Temperature	Test Conditions	Limits		Units
			Min.	Max.	
$C_{I/O}$	Input/Output Capacitance	STANDBY mode; $V_{I/O}$ = 2V		10	pF
C_{IN}	Input Capacitance	V_{OUT} = OV		10	pF

AC CHARACTERISTICS

Read Cycle (See Figures 1 and 2.)
T_A = 0°C to +70°C, V_{CC} = 5V ±5%

Symbol	Parameter	XL46C15-55 Limits		XL46C15-60 Limits		XL46C15-70 Limits		XL46C15-85 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55		60		70		85		ns
t_{AA}	Address Access Time		55		60		70		85	ns
t_{CS}	$\overline{CS_1}$, CS_2 or CS_3 Access Time		35		40		40		45	ns
t_{LZ}	Chip Enable to Output LOW Z	5		5		5		5		ns
t_{HZ}	Chip Disable to Output HIGH Z	0	35	0	40	0	40	0	45	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns

Chip Reset and Byte Write Cycles (See Figures 3 and 4.)
T_A = +20°C to +30°C, V_{CC} = 5V ±5%

Symbol	Parameter	XL46C15 Limits		Units
		Min.	Max.	
t_{RP}	Reset Pulse Width	50		ms
t_{WP}	Write Pulse Width	5		ms
t_{SC}	CS_2 Setup Time	0		ns
t_{HC}	CS_2 Hold Time	0		ns
t_{WR}	Write Recovery Time[1]	10		ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	500		ns
t_{DS}	Data Setup Time	0		ns
t_{DH}	Data Hold Time	0		ns

Note:
1. t_{WR} is defined as the minimum time required after a write pulse before initiating a data read cycle. This parameter is measured from the time at which the falling edge of $\overline{CS_1}$ reaches 5.5V until a valid read cycle is initiated. If a read cycle is initiated earlier than the minimum t_{WR} the output data may be invalid. Subsequent write cycles may be initiated immediately without delaying for t_{WR}.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

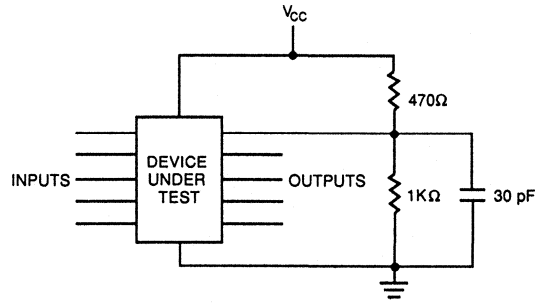


Figure 1. AC TEST CONDITIONS

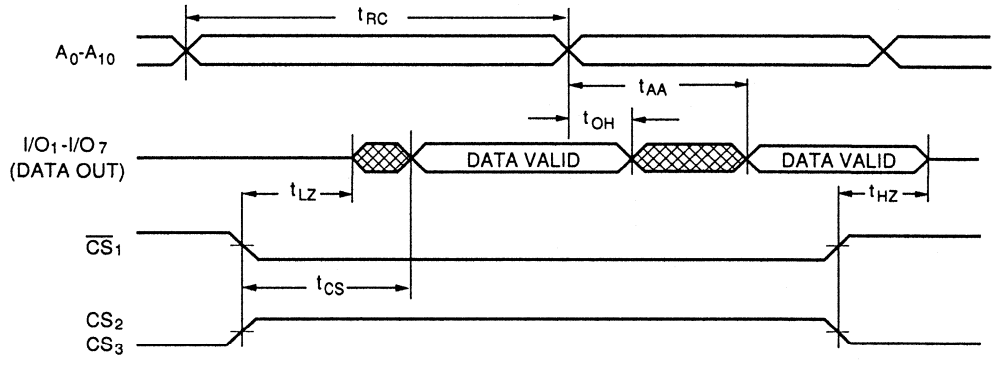


FIGURE 2. READ CYCLE TIMING

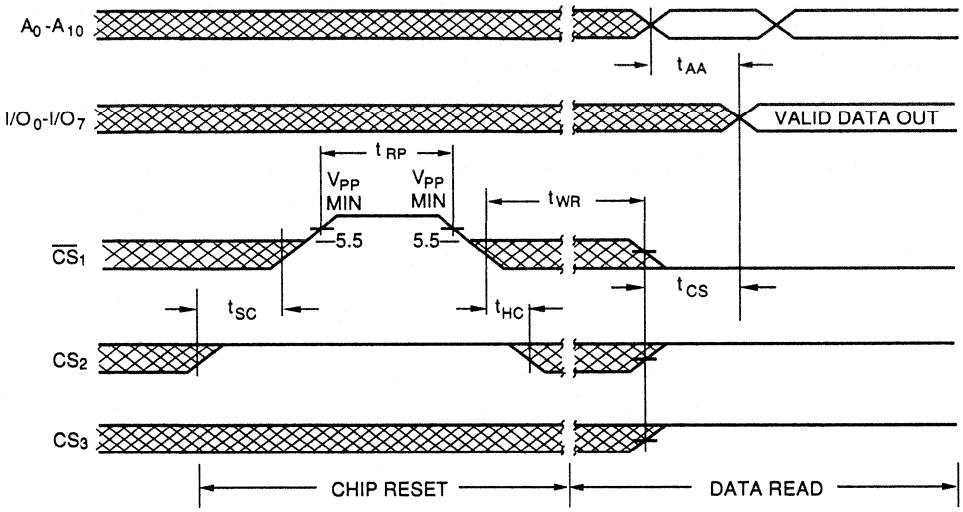


FIGURE 3. CHIP RESET CYCLE

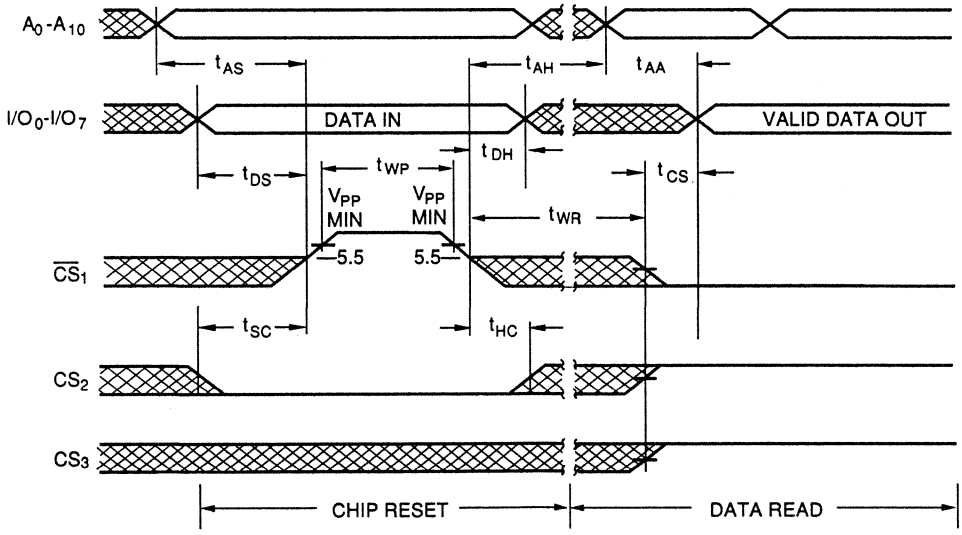


FIGURE 4. BYTE WRITE CYCLE

XL2864A

8K X 8 Electrically Erasable PROM

FEATURES

- **Fast Read Access Times**
  - **— 250ns, 300ns, 350ns, 450ns**
- **5 Volt-only Operation Including Write**
- **Industrial Temperature Range Available (XLE2864A)**
- **Fast Nonvolatile Write Cycle**
  - **— Internally Latched Data and Address**
  - **— 200ns Byte-load Cycle**
  - **— 10ms (max.) Nonvolatile Write Cycle**
  - **— Automatic Erase Before Write**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling To Minimize Write Cycle Times**
- **Automatic Page Write**
  - **— 1 to 32 bytes in 10ms (max.)**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**

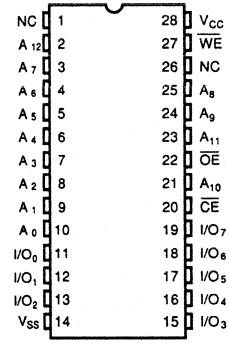
OVERVIEW

The XL2864A is a full-featured, 8K x 8 bit E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices. Read access times are as low as 250ns; standby current, less than 50mA. The device is fully functional with a single 5V power supply, and the XL2864A is manufactured with EXEL's 2.0µ NMOS E²PROM process.

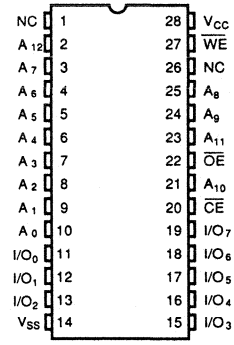
The device is exceptionally system friendly, incorporating a device status indicator and a fully automatic 32-byte page write feature. $\overline{\text{DATA}}$ polling is provided to maximize device versatility and allow the host system to exploit the actual nonvolatile write cycle time. This is a software technique which is used to observe nonvolatile write cycle completion without requiring external hardware.

PIN CONFIGURATION

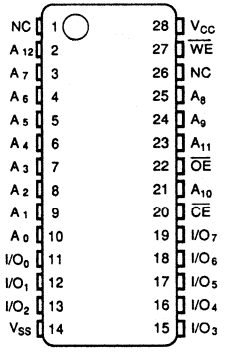
28 Pin PDIP
Type "P" Package



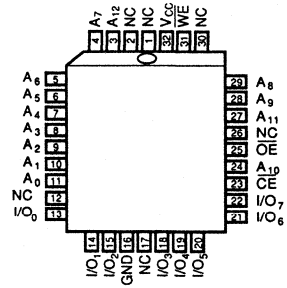
28 Pin CERDIP
Type "C" Package



Small Outline
Type "J" Package



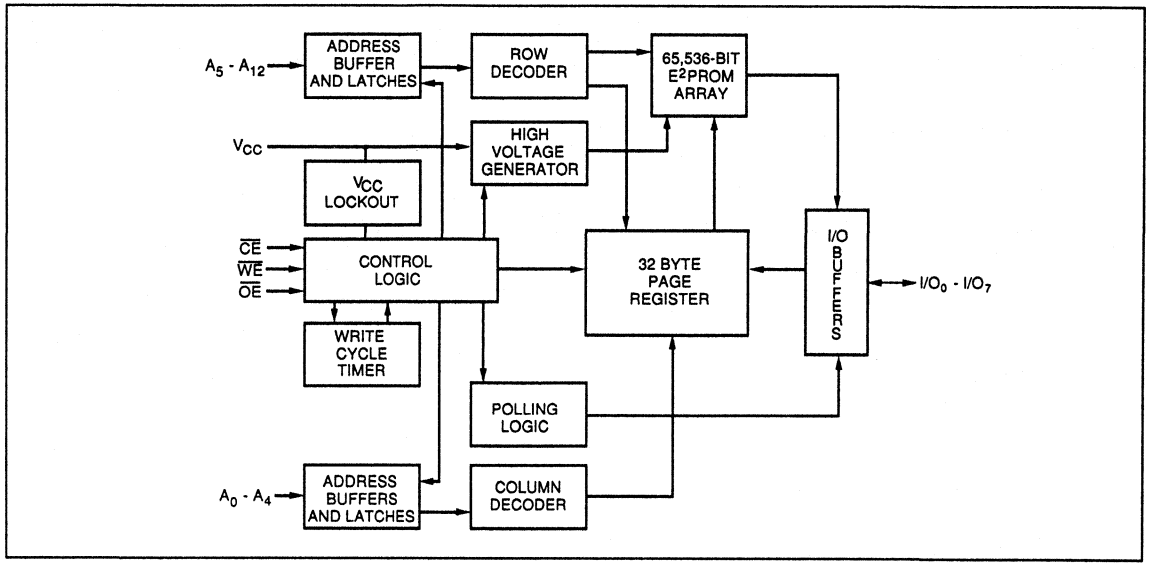
32 Pin PLCC
Type "D" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The automatic page write feature allows the system to program up to 32 bytes during a single nonvolatile write cycle, providing an effective write speed of at most 312ms/byte. The entire 8K byte memory may be programmed in a maximum of 2.6 seconds when the page write mode is employed.

The XL2864A features $\overline{OE}$ write inhibit logic and noise protected $\overline{WE}$ to inhibit inadvertent writes.

The XL2864A is compatible with industrial standard 8K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL2864A provides secure and reliable data storage thoughout your systems lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2864A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2864A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2864A is designed for applications requiring up to 10,000 data writes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

The latches in the automatic page write buffer include corresponding flag bits which are set when a given page location is written. In the event that a nonvolatile write cycle occurs with less than 32-bytes of data, only those bytes in the E^2PROM array corresponding to the locations in the buffer which were actually written will be reprogrammed. This feature eliminates unnecessary cycling and ensures maximum endurance. This is in contrast to some competing E^2PROM devices which reprogram the full page of nonvolatile locations independent of the number of page latches actually written to. This wastes cell cycles and may substantially reduce device endurance and, consequently, system reliability.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2864A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2864A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Write Mode

In the XL2864A, the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both address and data are latched in a brief 150ns interval using a 5V supply and TTL write signals.

Once the data is latched, the XL2864A will automatically erase the selected byte and write the new data in less than 10ms. The host system is therefore freed to proceed with other operations while the XL2864A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress with the exception of I/O_7 if a read command is asserted. (See Monitoring Device Status in the next column of this page.) (See Figures 3 and 4.)

Standby Mode

Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 50mA. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode

The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O pins high. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL2864A, a status indicator has been incorporated to provide for the host system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL2864A until it determines a simple logical condition.

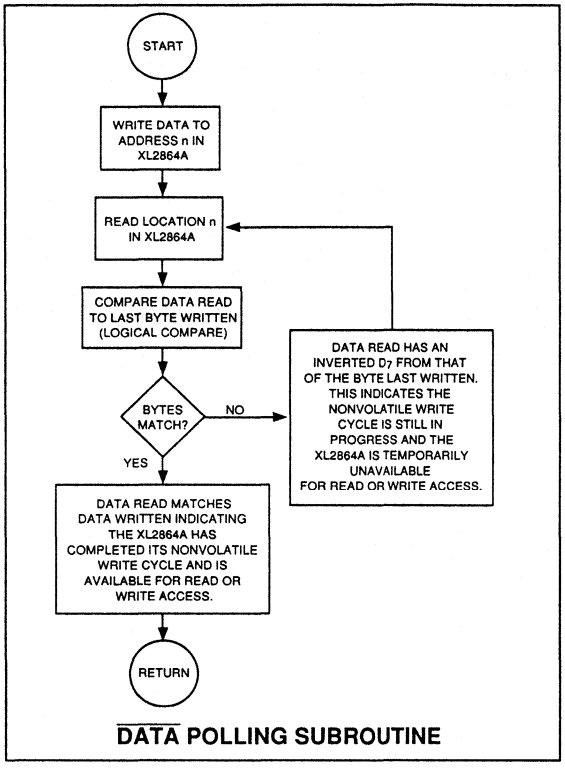
$\overline{DATA}$ Polling

The XL2864A provides a feature named $\overline{DATA}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL2864A is busy executing its nonvolatile write cycle will be interpreted as a $\overline{DATA}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{DATA}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile write cycle timing.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⎍	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⎍	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	⎍	Chip Erase*	$D_{IN} = V_{IH}$	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL Microelectronics for details on the Chip Erase Mode.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL2864A. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL2864A. During the 10ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O_7. I/O_7 is set to output the **complement** of the value of the MSB of the last byte written to the XL2864A when a read command is asserted. (See Figure 5.)

The READY/$\overline{\text{BUSY}}$ test procedure is quite simple. The system simply reads the location last written to in the XL2864A and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL2864A is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to wait the 10ms (max.) period specified and enabling accelerated device loading operations.

Automatic Page Write

The XL2864A contains a 32-byte temporary (volatile) buffer which allows the user to simultaneously program from one to 32 bytes in a page during a single 10ms (max.) nonvolatile write cycle without any special setup or software procedures. This can effectively reduce the byte write time by a factor of 32. The device will begin its nonvolatile write cycle from 300 to 600µs (t_{PL}) after the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). At this point, the device commences a nonvolatile write cycle and copies data from each of the latches which were updated into the designated E^2PROM locations (see Endurance and Data Retention section). Thus, all bytes to be programmed during an automatic page write cycle must be written into the page buffer within t_{PL} minimum to guarantee that they are transferred into the E^2PROM array. (See Figure 6.)

The 32-byte page into which the data will be written is specified by the most significant bits of the address (A_5-A_{12}) presented during the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). The byte within the specified page is identified by the five least significant bits of the address (A_0-A_4) presented during the first and subsequent system write cycles. Bytes may be written into the page in any order. If data is written more than once to the same byte in the temporary buffer during a single page load operation, then the most recently written data will be valid.

If a read operation is attempted during loading of the page buffer, the buffer load cycle is not affected. However, that read cycle will be interpreted as a $\overline{\text{DATA}}$ polling cycle.

WRITE PROTECT MECHANISMS

The XL2864A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{\text{OE}}$ Write Inhibit

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will be inhibited. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 20ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin (except $\overline{OE}$)* ..... -1.0V to +6.5V
Voltage on $\overline{OE}$ Pin* ..... -1.0V to +22.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		110	mA
I_{SB}	V_{CC} Current-Standby	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.25V	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.25V	-10	10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH}= -400µA	2.4		V
V_H	High Voltage for Chip Erase		15	18	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	XL2864A-250 Limits		XL2864A-300 Limits		XL2864A-350 Limits		XL2864A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		80		80		120		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)

T_A = 0°C to +70°C for the XLS2864A or -40°C to +85°C for the XLE2864A, V_{CC} = 5V±5%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	125		ns
t_{CS}	Chip Enable or Write Enable Setup Time	0		ns
t_{CH}	Chip Enable or Write Enable Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}*	Write Enable Pulse Width	150		ns
t_{WPH}	Write Recovery Time	50		ns
t_{DV}	Data Valid Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{PL}	Page Load Time	300	600	µs
t_{BLC}	Byte Load Cycle	0.2	25	µs

* NOTE: A write pulse of less than 20ns will not initiate a write cycle.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

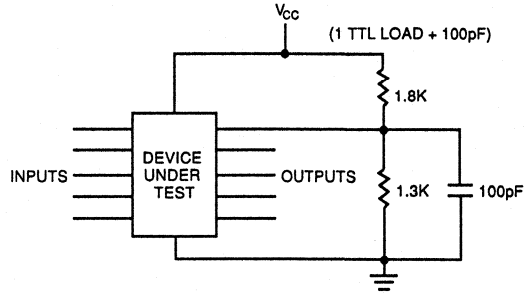


FIGURE 1. AC TEST CONDITIONS

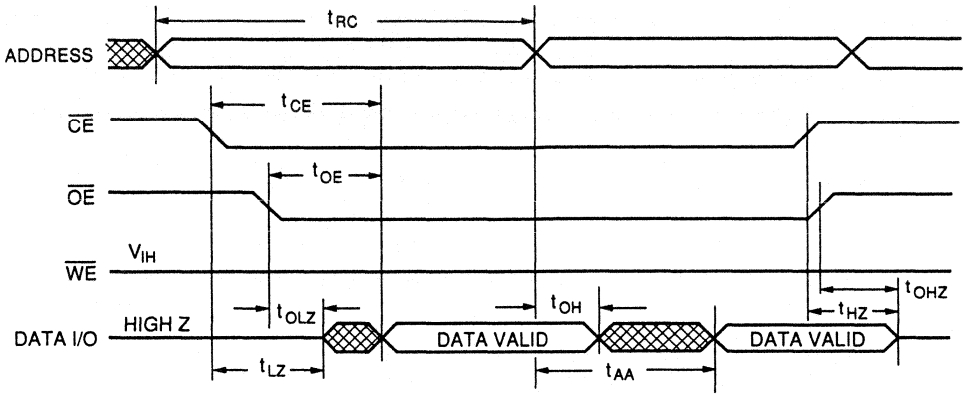


FIGURE 2. READ CYCLE TIMING

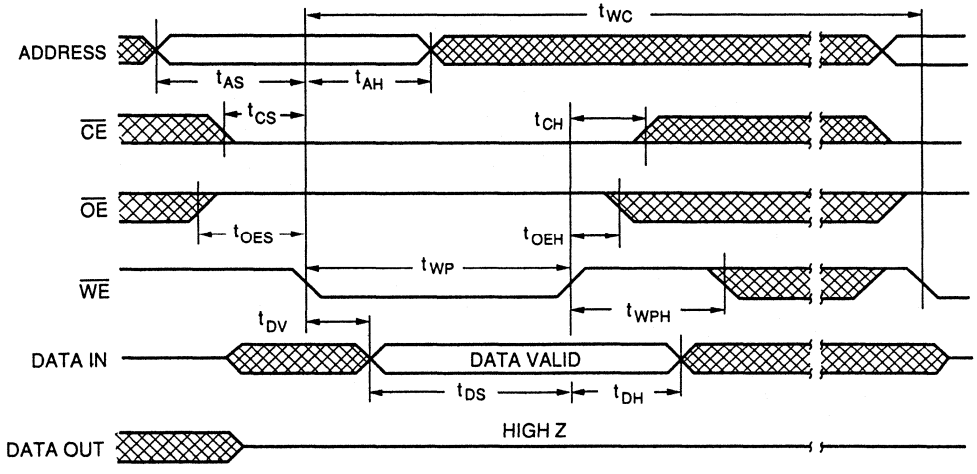


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

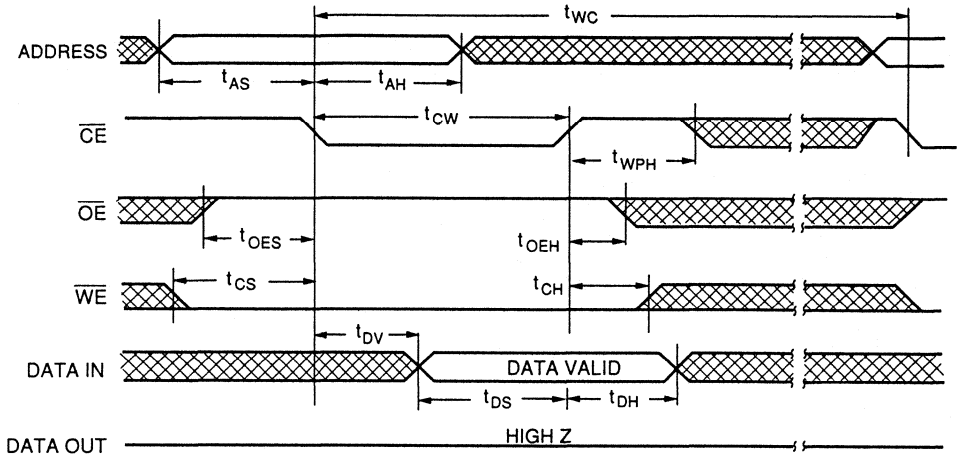
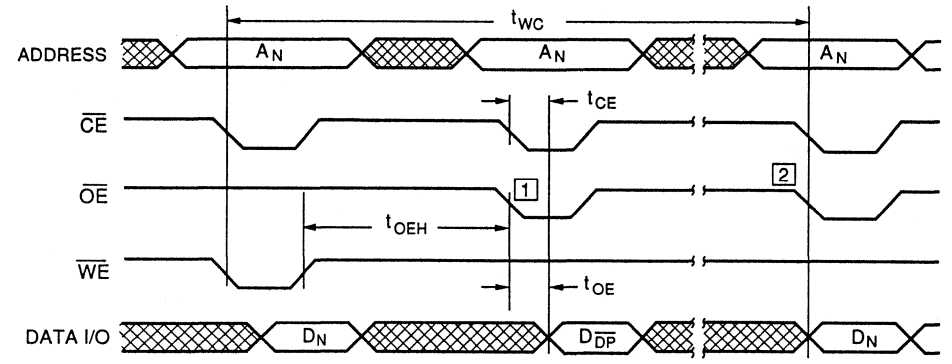


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL2864A indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

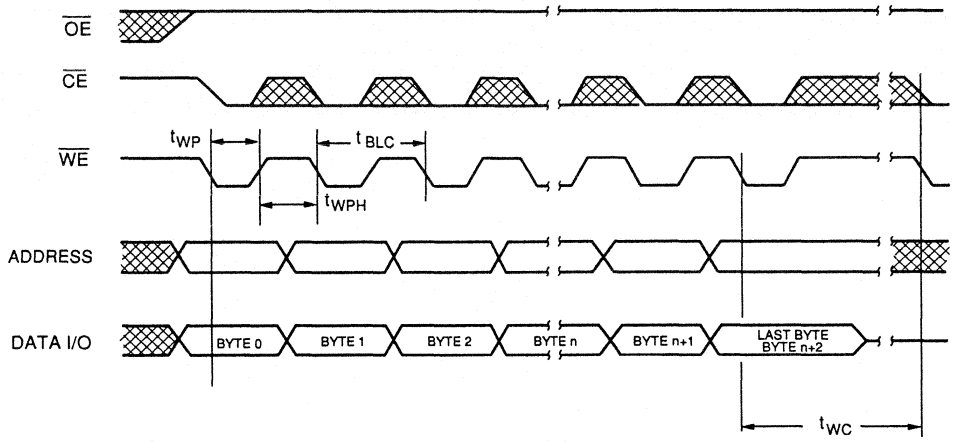


FIGURE 6. PAGE MODE WRITE CYCLE TIMING

XL2865A

8K X 8 Electrically Erasable PROM

FEATURES

- **Fast Read Access Times**
  — 250ns, 300ns, 350ns, 450ns
- **5 Volt-only Operation**
  — Including Write
- **Industrial Temperature Range Available (XLE2865A)**
- **Fast Nonvolatile Write Cycle**
  — Internally Latched Data and Address
  — 200ns Byte-load Cycle
  — 10ms Nonvolatile Write Cycle
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **$\overline{\text{DATA}}$ Polling To Minimize Write Cycle Times**
- **READY/$\overline{\text{BUSY}}$ Pin Status Indicator**
- **Automatic Page Write**
  — 1 to 32 bytes in 10ms (max.)
- **TTL Compatible Inputs and Outputs**

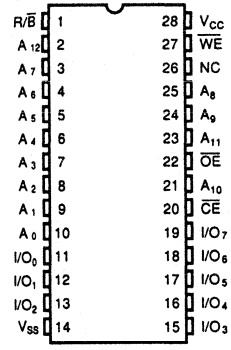
OVERVIEW

The XL2865A is a full-featured, 8K x 8 bit E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 16K bit E²PROM devices. Read access times are as low as 250ns; standby current, less than 50mA. The device is fully functional with a single 5V power supply, and the XL2865A is manufactured with EXEL's 2.0µ NMOS E²PROM process.

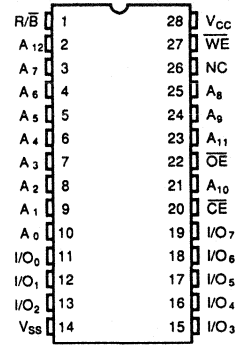
The device is exceptionally system friendly, incorporating a device status indicator and a fully automatic 32-byte page write feature. $\overline{\text{DATA}}$ polling and a READY/$\overline{\text{BUSY}}$ pin are provided to maximize device versatility and allow the host system to exploit the actual nonvolatile write cycle time. This is a software technique which is used to observe nonvolatile write cycle completion without requiring external hardware.

PIN CONFIGURATION

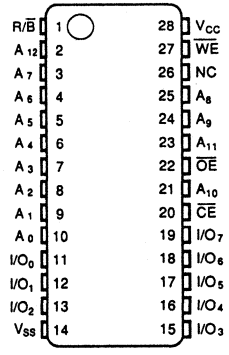
28 Pin PDIP
Type "P" Package



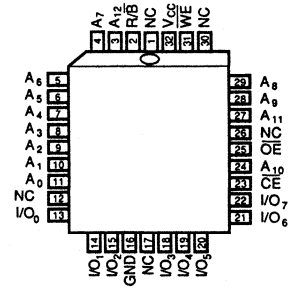
28 Pin CERDIP
Type "C" Package



Small Outline
Type "J" Package



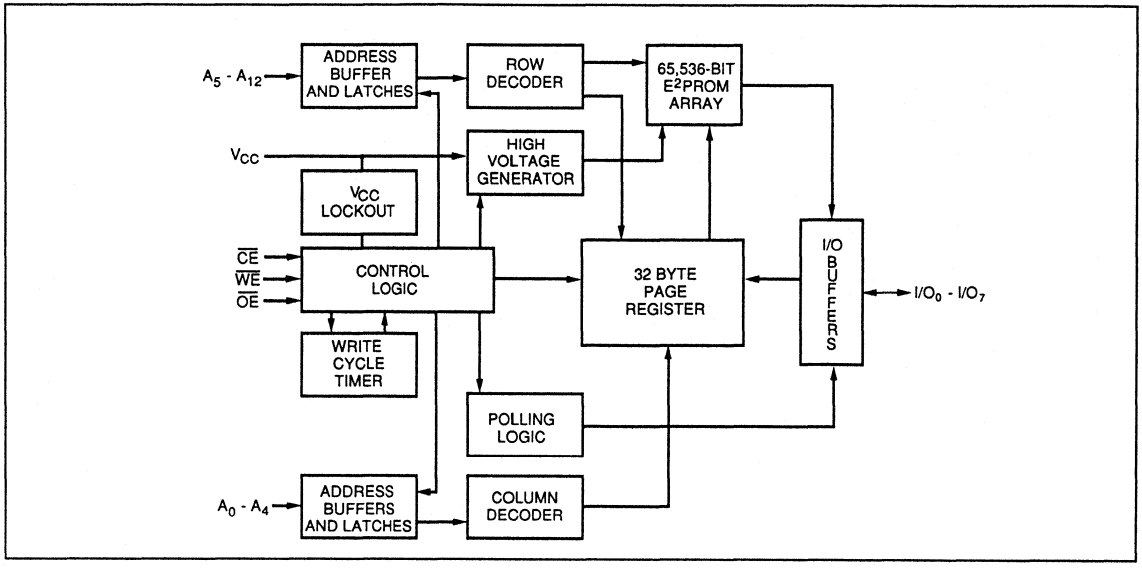
32 Pin PLCC
Type "D" Package



PIN NAMES

A_0-A_{10}	Address Inputs
I/O_0-I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
R/$\overline{B}$	READY/$\overline{\text{BUSY}}$ Indicator
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The automatic page write feature allows the system to program up to 32 bytes during a single nonvolatile write cycle, providing an effective write speed of at most 312ms/byte. The entire 8K byte memory may be programmed in a maximum of 2.6 seconds when the page write mode is employed.

The XL2865A features $\overline{OE}$ write inhibit logic and noise protected $\overline{WE}$ to inhibit inadvertent writes.

The XL2865A is compatible with industrial standard 8K x 8 E^2PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E^2PROMS as well.

APPLICATIONS

The XL2865A provides secure and reliable data storage thoughout your system's lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2865A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2865A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL2865A is designed for applications requiring up to 10,000 data writes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

The latches in the automatic page write buffer include corresponding flag bits which are set when a given page location is written. In the event that a nonvolatile write cycle occurs with less than 32-bytes of data, only those bytes in the E^2PROM array corresponding to the locations in the buffer which were actually written will be reprogrammed. This feature eliminates unnecessary cycling and ensures maximum endurance. This is in contrast to some competing E^2PROM devices which reprogram the full page of nonvolatile locations independent of the number of page latches actually written to. This wastes cell cycles and may substantially reduce device endurance and, consequently, system reliability.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL2865A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode

Data is read from the XL2865A by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the time when the final controlling line ($\overline{CE}$ or $\overline{OE}$) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state.)

Write Mode

In the XL2865A, the write cycle is initiated by applying a logical "0" to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is logical "1." The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$ (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both address and data are latched in a brief 150ns interval using a 5V supply and TTL write signals.

Once the data is latched, the XL2865A will automatically erase the selected byte and write the new data in less than 10ms. The host system is therefore freed to proceed with other operations while the XL2865A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress with the exception of I/O_7 if a read command is asserted. (See monitoring device status in the next column of this page.) (See Figures 3 and 4.)

Standby Mode

Whenever $\overline{CE}$ is brought HIGH, the device is set into its standby mode, placing the I/O pins in a high impedance state. Standby power dissipation is less than 50mA. While $\overline{CE}$ remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

Chip Erase — High Voltage Mode

The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command while holding data on the I/O inputs HIGH. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

MONITORING DEVICE STATUS

Because the internal nonvolatile write cycle is completely managed by the XL2865A, a status indicator has been incorporated to provide for the host system to monitor the READY/$\overline{BUSY}$ status of the device. This is accomplished through a system software routine which simply re-reads the XL2865A until it determines a simple logical condition.

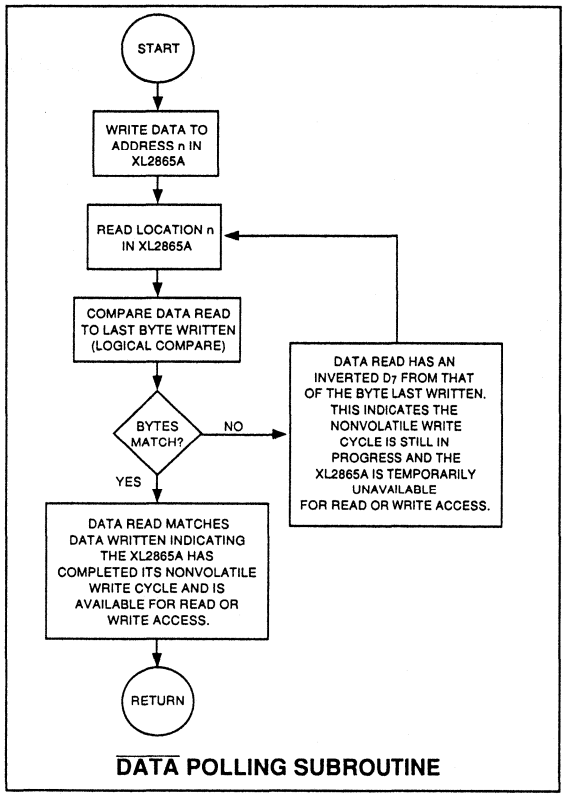
$\overline{DATA}$ Polling

The XL2865A provides a feature named $\overline{DATA}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL2865A is busy executing its nonvolatile write cycle will be interpreted as a $\overline{DATA}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{DATA}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or nonvolatile write cycle timing.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊓	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	⊓	Chip Erase*	$D_{IN} = V_{IH}$	Active
X	V_{IL}	X	Write Inhibit	—	—

*Contact EXEL Microelectronics for details on the Chip Erase Mode.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL2865A. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL2865A. During the 10ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O7. I/O7 is set to output the **complement** of the value of the MSB of the last byte written to the XL2865A when a read command is asserted. (See Figure 5.)

The READY/$\overline{\text{BUSY}}$ test procedure is quite simple. The system simply reads the location last written to in the XL2865A and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL2865A is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to wait the 10ms (max.) period specified and enabling accelerated device loading operations.

READY/$\overline{\text{BUSY}}$ Pin (R/$\overline{\text{B}}$)

The R/$\overline{\text{B}}$ pin (pin 1) is a dedicated status indicator which remains at a logic "1" during device operation unless the XL2865A is internally occupied with a nonvolatile write cycle or the supply voltage is below 4.0V. When a system write cycle is initiated, R/$\overline{\text{B}}$ is brought to a logic "0", returning to a logic "1" when the corresponding nonvolatile write cycle is completed. This pin may be conveniently polled for nonvolatile write cycle status or may be used to initiate an interrupt announcing to the controller that the cycle is complete and the device is, once again, available for normal access. This output is configured as an open-drain driver to be OR-tied and thus requires an appropriate pull-up resistor for proper operation. The pull-up resistor value for the R/B output may be calculated as follows:

$$R_P = \frac{5.1V}{I_{IL} + 2.1mA}$$

where I_{IL} = the sum of the input currents of all the devices tied to R/$\overline{\text{B}}$.

Automatic Page Write

The XL2865A contains a 32-byte temporary (volatile) buffer which allows the user to simultaneously program from one to 32 bytes in a page during a single 10ms (max.) nonvolatile write cycle without any special setup or software procedures. This can effectively reduce the byte write time by a factor of 32. The device will begin its nonvolatile write cycle from 300 to 600µs (t_{PL}) after the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). At this point, the device commences a nonvolatile write cycle and copies data from each of the latches which were updated into the designated E^2PROM locations (see Endurance and Data Retention section). Thus, all bytes to be programmed during an automatic page write cycle must be written into the page buffer within t_{PL} minimum to guarantee that they are transferred into the E^2PROM array. (See Figure 6).

The 32-byte page into which the data will be written is specified by the most significant bits of the address (A_5-A_{12}) presented during the first system write operation following the completion of a previous nonvolatile write cycle (or power-up). The byte within the specified page is identified by the five least significant bits of the address (A_0-A_4) presented during the first and subsequent system write cycles. Bytes may be written into the page in any order. If data is written more than once to the same byte in the temporary buffer during a single page load operation, then the most recently written data will be valid.

If a read operation is attempted during loading of the page buffer, the buffer load cycle is not affected. However, that read cycle will be interpreted as a $\overline{\text{DATA}}$ polling cycle.

WRITE PROTECT MECHANISMS

The XL2865A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

$\overline{OE}$ Write Inhibit

If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3.

Noise Protection

Write pulses of less than 20ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin (except $\overline{OE}$)* ..... -1.0V to +6.5V
Voltage on $\overline{OE}$ Pin* ..... -1.0V to +22.0V
ESD Rating 2000V
DC Output Current 5mA

*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

DC CHARACTERISTICS

T_A = 0°C to +70°C for the XLS2865A or -40°C to +85°C for the XLE2865A, V_{CC} = 5V±5%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	V_{CC} Current-Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		110	mA
I_{SB}	V_{CC} Current-Standby	$\overline{CE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open Other Inputs = 5.25V		50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5.25V	-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to 5.25V	-10	10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+ 0.5	V
V_{OL}	Output Low Voltage	I_{OL}= 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH}= -400 µA	2.4		V
V_H	High Voltage for Chip Erase		15	18	V

CAPACITANCE

T_A= +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figure 2)
T_A = 0°C to +70°C for the XLS2865A or -40°C to +85°C for the XLE2865A, V_{CC} = 5V±5%

Symbol	Parameter	XL2865A-250 Limits		XL2865A-300 Limits		XL2865A-350 Limits		XL2865A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		350		450		ns
t_{AA}	Address Access Time		250		300		350		450	ns
t_{CE}	Chip Enable Access Time		250		300		350		450	ns
t_{OE}	Output Enable Access Time		80		80		120		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	80	10	80	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	20		20		20		20		ns

WRITE CYCLE (See Figures 3 and 4)
T_A = 0°C to +70°C for the XLS2865A or -40°C to +85°C for the XLE2865A, V_{CC} = 5V±5%

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Nonvolatile Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	125		ns
t_{CS}	Chip Enable or Write Enable Setup Time	0		ns
t_{CH}	Chip Enable or Write Enable Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	150		ns
t_{OES}	Output Enable Setup Time	10		ns
t_{OEH}	Output Enable Hold Time	10		ns
t_{WP}*	Write Enable Pulse Width	50		ns
t_{WPH}	Write Recovery Time	50		ns
t_{DV}	Data Valid Time	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{PL}	Page Load Time	300	600	µs
t_{BP}	$\overline{CE}$ and $\overline{WE}$ Low to R/$\overline{B}$ Low		150	ns
t_{BWR}	Busy to Write Recovery Time		25	µs
t_{BLC}	Byte Load Cycle	0.2		µs

* NOTE: A write pulse of less than 20ns will not initiate a write cycle.

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

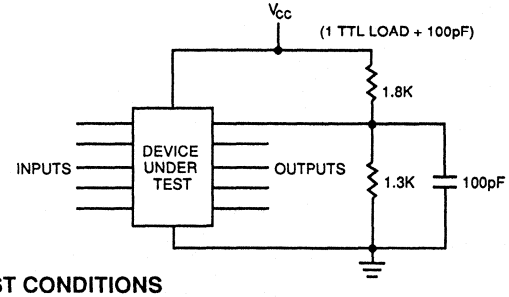


FIGURE 1. AC TEST CONDITIONS

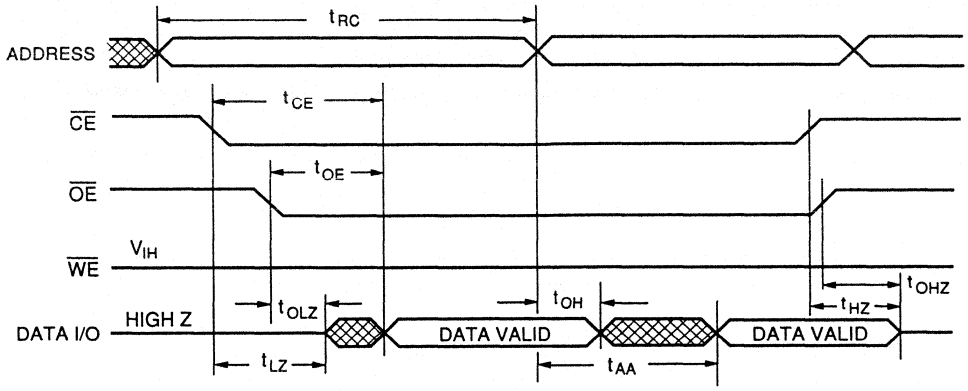


FIGURE 2. READ CYCLE TIMING

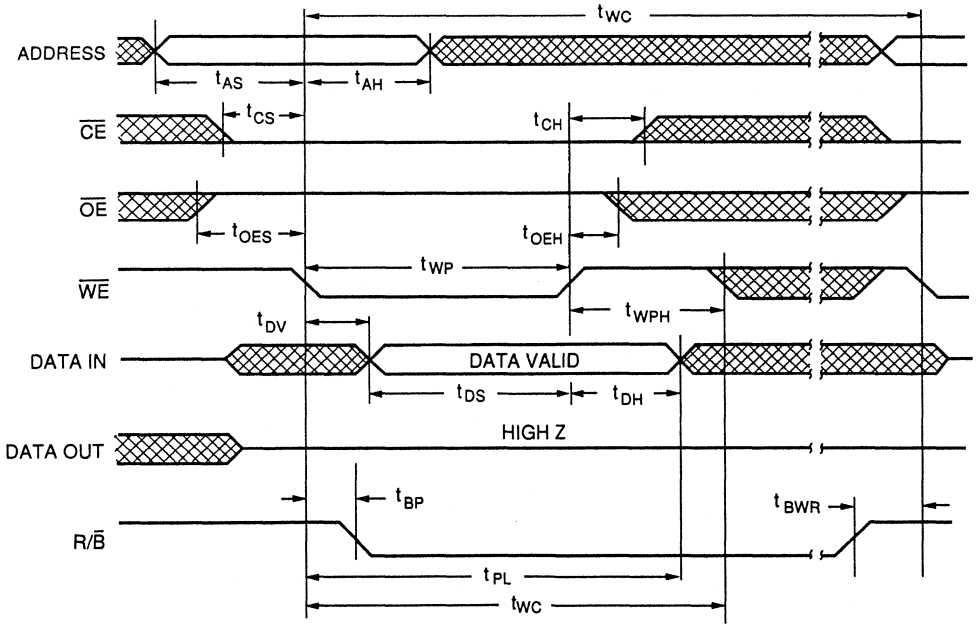


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

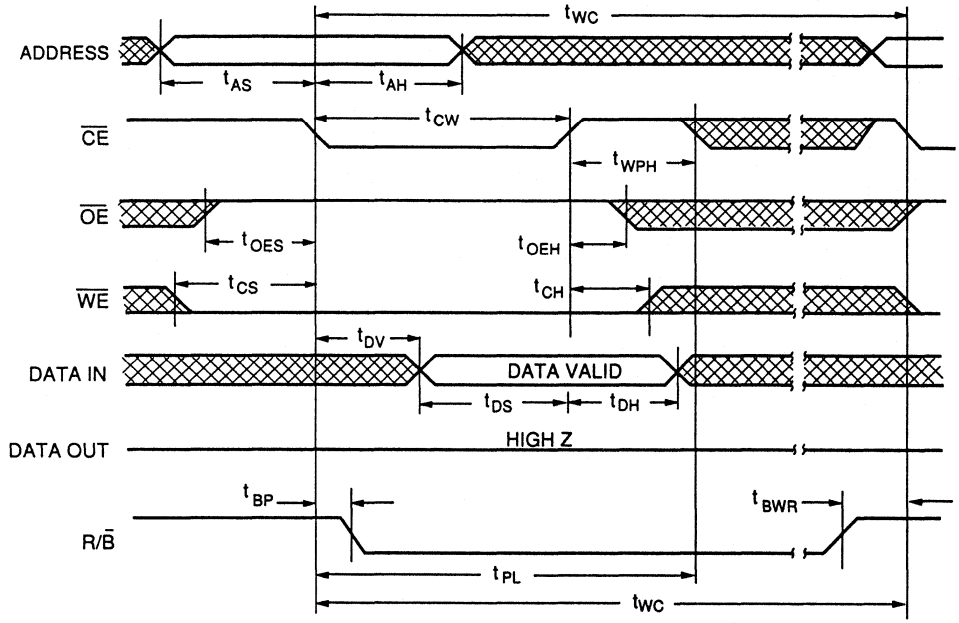
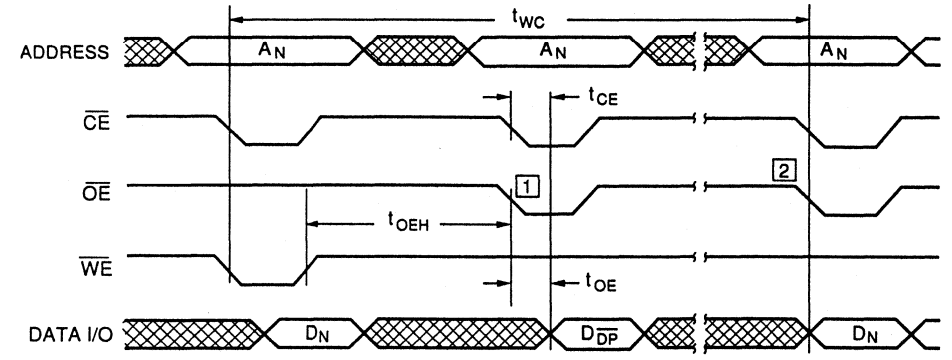


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING



1. This initiates a read cycle yielding $D_{\overline{DP}}$ (inverted MSB) at the output buffer indicating the device is still busy with the nonvolatile write cycle.

2. This initiates a read cycle yielding the data which was written to the XL2865A indicating that the nonvolatile write cycle is complete and that the device is available for subsequent commands.

FIGURE 5. $\overline{DATA}$ POLLING TIMING

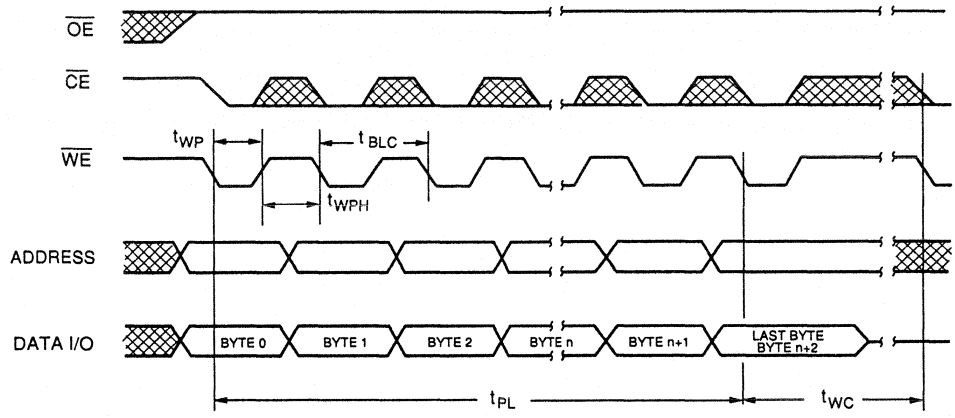


FIGURE 6. PAGE MODE WRITE CYCLE TIMING

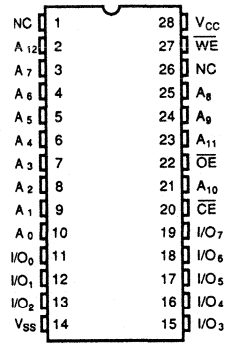
8K X 8 CMOS Electrically Erasable PROM
5ms Nonvolatile Write Cycle

FEATURES

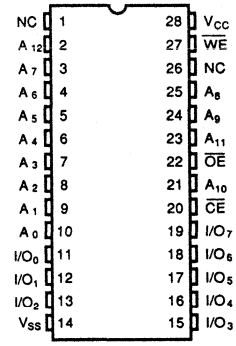
- **Fast Read Access Times**
  - **— 120ns, 150ns, 200ns and 250ns**
- **Low CMOS Power Consumption**
  - **— 60mA (Active)**
  - **— 150µA (Standby)**
- **5 Volt-only Operation**
  - **— Including write**
- **Fast Nonvolatile Write Cycle**
  - **— Internally latched data and address**
  - **— 120ns byte-load cycle**
  - **— 5ms (max.) nonvolatile write cycle**
- **Self-Timed Writes**
  - **— Effective 75µs/byte write**
  - **— 64 byte page input buffer**
  - **— Auto-erase before write**
  - **— $\overline{\text{DATA}}$ Polling**
- **Automatic Page Write Mode**
  - **— 64 byte page size**
  - **— 5ms page write time**
- **On-chip Inadvertent Write Protection**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **ESD Protected to 2000V**

PIN CONFIGURATIONS

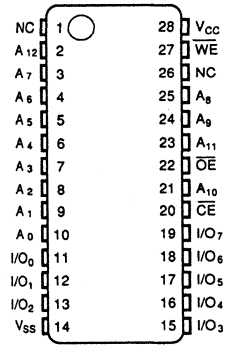
28 Pin CERDIP
Type "C" Package



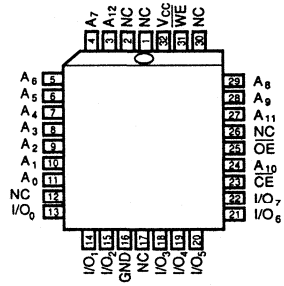
28 Pin Plastic DIP
Type "P" Package



28 Pin SOIC
Type "J" Package



32 Pin PLCC
Type "D" Package



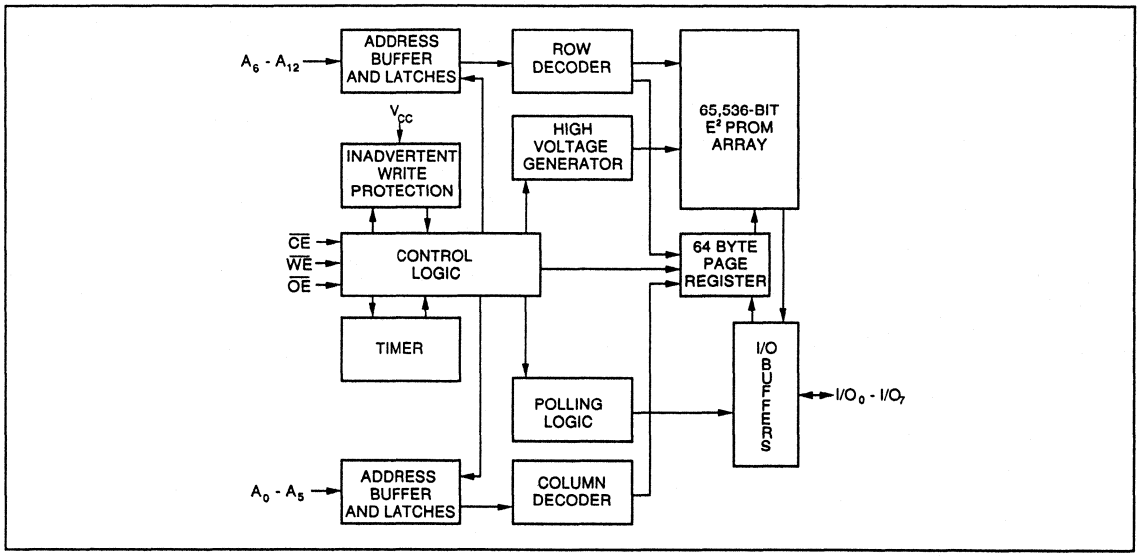
OVERVIEW

The XL28C64 is a full-featured, 8K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 64K devices, but offers improved speed and power efficiency. Read access times can be as low as 120ns; standby current, less than 100µA. It features a page-wide input buffer and improved protection against inadvertent writes. Operating modes function from a single 5V power supply, and the XL28C64 is manufactured with EXEL's proven double-metal, 1.4µ CMOS process.

PIN NAMES

A0-A12	Address Inputs
I/O0- I/O7	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
VCC	Supply Voltage
VSS	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and supplemental inadvertent write protection circuitry. It fits into standard SRAM sockets and responds to typical SRAM write commands.

The fully-automatic 64-byte page-write allows the entire memory to be programmed in less than 0.65 sec. Internal latches, for address and data, free the system bus during the 5ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read access time, adding to system performance.

Inadvertent writes are inhibited by a wide range of protections built into the XL28C64. A low V_{CC} lockout feature disables nonvolatile write cycles when V_{CC} drops below 3.5V (V_{WI}) (typical). Additionally, the XL28C64 features power-on reset and noise protected $\overline{WE}$.

The XL28C64 is compatible with existing 64K E^2PROMs—both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E^2PROMs as well.

APPLICATIONS

The nonvolatile storage in the XL28C64 replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in telephones and facsimile machines. The XL28C64 is ideal in applications that are self-adapting, such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C64 is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL28C64. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E^2PROM standards.

Read Mode
Data is read from the XL28C64 by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the latter of either the time when the controlling line goes LOW ($\overline{CE}$ or $\overline{OE}$), or the time when the address is established.

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The XL28C64 uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers this data in the page-buffer to the E^2PROM array without user intervention.

The XL28C64 contains (128) 64-byte pages. Address lines A_6-A_{12} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one nonvolatile write cycle must be on the same page. (A_6-A_{12} must remain unchanged.) Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written to any given byte when the nonvolatile write cycle begins is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to initiate the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. An internal byte-load timer is started on the falling edge of the controlling line. The timer provides a 100µs window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period.

When the byte-load timer times out, additional external byte-load cycles are ignored and data is automatically transferred from the page buffer to the E^2PROM array through an internally managed nonvolatile write cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

An internal write-flag is set on the first byte-load of each write cycle. Data pins remain in a high impedance state except during a byte-load (when they contain the forced input data) or during a $\overline{DATA}$ polling read (see below). When the high voltage cycle is completed, the write-flag is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 100µA with CMOS level inputs.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

MODE SELECTION

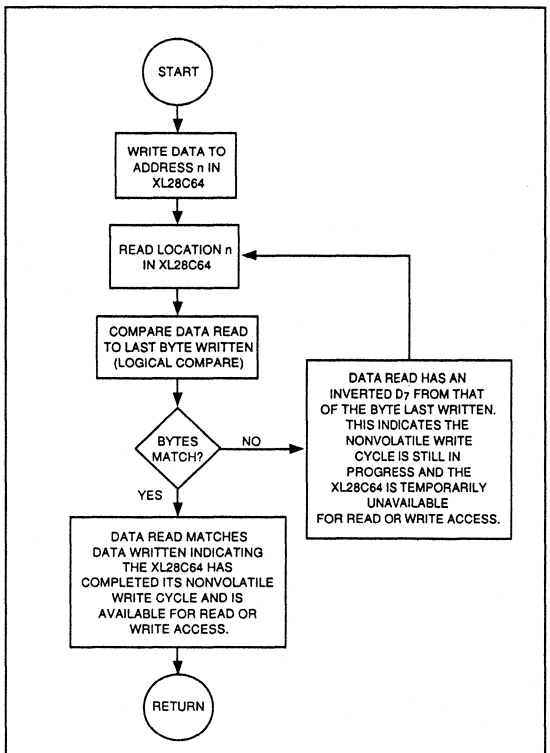
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓_⊓	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⊓_⊓	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In = X	Active
V_{IL}	V_{IL}	V_{IH}	$\overline{DATA}$ Polling	$\overline{D_7}$	Active
X	V_{IL}	X	Write Inhibit	X	Active

*Contact EXEL for details.

$\overline{\text{DATA}}$ Polling

The XL28C64 provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C64 is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or the nonvolatile cycle timing.

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C64. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C64. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers are set in a high impedance state with the exception of I/O_7. I/O_7 is set to output the complement of the value of the MSB of the last byte written to the XL28C64 ***when a read command is asserted.***



$\overline{\text{DATA}}$ POLLING SUBROUTINE

The READY/$\overline{\text{BUSY}}$ test procedure is quite simple. The system simply reads the location last written to in the XL28C64 and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C64 is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to await the 5ms (max.) period specified, and enabling accelerated device loading operations.

WRITE PROTECT MECHANISMS

The XL28C64 features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise.

$\overline{\text{OE}}$ Write Inhibit

If $\overline{\text{OE}}$ is brought LOW before the $\overline{\text{CE}}$ and $\overline{\text{WE}}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

V_{CC} Lockout

The XL28C64 has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL28C64 and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort nor affect nonvolatile write cycles already in progress, yet inhibits new cycles from being initiated.

Power-Up Write Enable Delay

At power-up, operation is inhibited until V_{CC} is stable and sufficiently high. Write operations are inhibited until 1ms after V_{CC} reaches 2.0V to allow the system to stabilize while blocking potential inadvertent write commands.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{\text{WE}}$ pin will not initiate nonvolatile write cycles.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Lead Soldering Temperature (less than 10 seconds).....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin* .....-1.0 to +7.0V
Voltage on $\overline{OE}$ Pin* .....-1.0 to +15V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C64 or -40°C to +85°C for the XLE28C64, V_{CC} = 5V ±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	Vcc Current — Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH} I/O's = open A_0-A_{12} toggling @ 5MHz		60	mA
I_{SB}	Vcc Current — Standby (TTL)	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = Vcc		2	mA
I_{SBC}	Vcc Current — Standby (CMOS)	$\overline{CE}$ = $\overline{WE}$ V cc-.2V $\overline{OE}$ = V ss+0.2V I/O's = open A_0-A_{12} = Vcc		150	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc		10	µA
I_{LO}	Output Leakage — Standby	V_{OUT} = GND to Vcc $\overline{CE}$ = V_{IH}		10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc + 0.5	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 Vcc-0.1		V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figures 1 and 2)

T_A=0°C to +70°C for the XLS28C64 or -40°C to +85°C for the XLE28C64, V_{CC}=5V±5%

Symbol	Test	XL28C64-120		XL28C64-150		XL28C64-200		XL28C64-250		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		60		75		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 3, 4 and 5)

T_A=0°C to +70°C for the XLS28C64 or -40°C to +85°C for the XLE28C64, V_{CC}=5V±5%

Symbol	Test	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{BLC}	Byte Load Cycle	.120	100	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

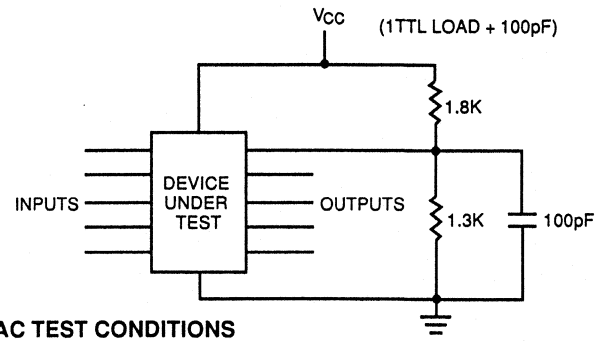


FIGURE 1. AC TEST CONDITIONS

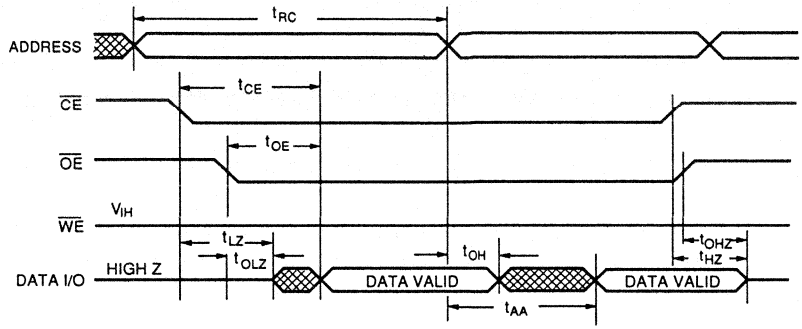


FIGURE 2. READ CYCLE TIMING

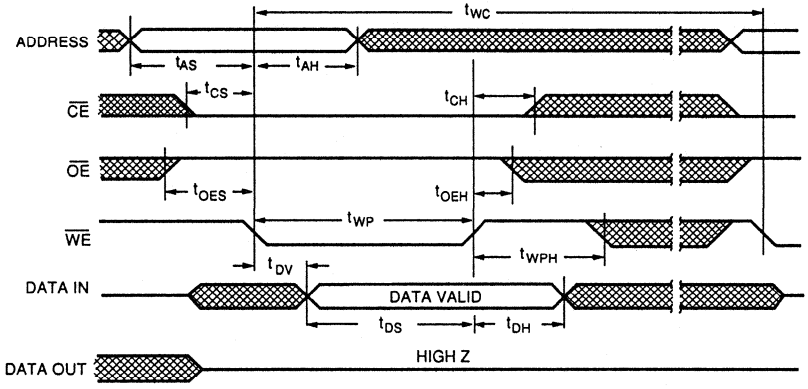


FIGURE 3. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

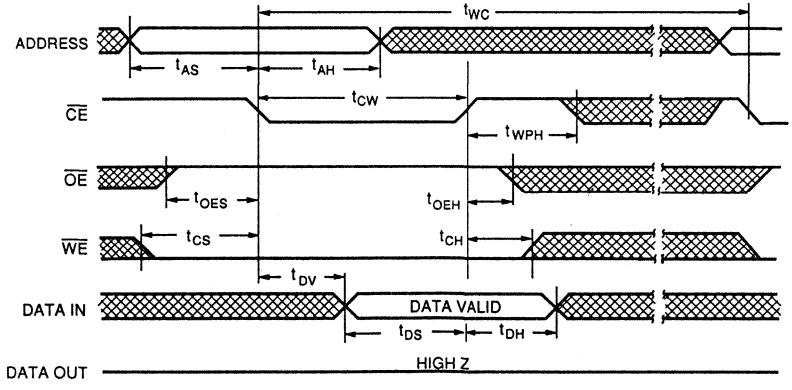


FIGURE 4. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

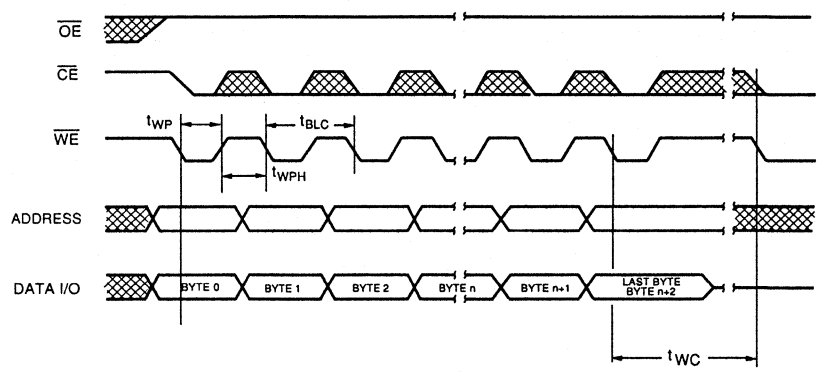


FIGURE 5. PAGE MODE WRITE CYCLE TIMING

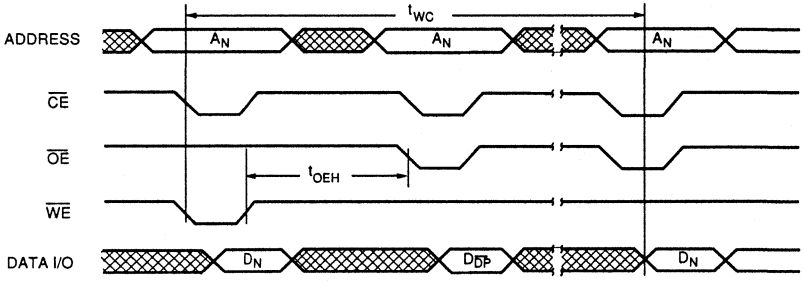


FIGURE 6. $\overline{\text{DATA}}$ POLLING TIMING

XL28C64B

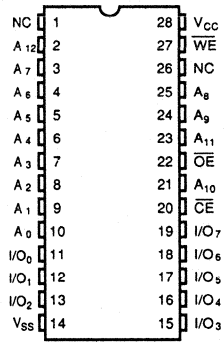
8K X 8 CMOS Electrically Erasable PROM
5ms Nonvolatile Write Cycle

FEATURES

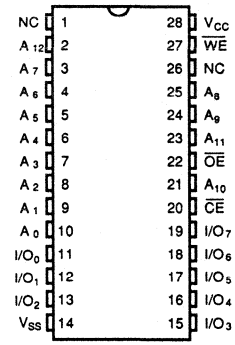
- **Fast Read Access Times**
  - **120ns, 150ns, 200ns and 250ns**
- **Low CMOS Power Consumption**
  - **60mA (Active)**
  - **150µA (Standby)**
- **5 Volt-only Operation**
  - **Including write**
- **Fast Nonvolatile Write Cycle**
  - **Internally latched data and address**
  - **120ns byte-load cycle**
  - **5ms (max.) nonvolatile write cycle**
- **Self-Timed Writes**
  - **Effective 75µs/byte write**
  - **64 byte page input buffer**
  - **Auto-erase before write**
  - **$\overline{\text{DATA}}$ Polling**
  - **Toggle bit**
- **Software Mode Control**
- **Automatic Page Write Mode**
  - **64 byte page size**
  - **5ms page write time**
- **On-chip Inadvertent Write Protection**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **ESD Protected to 2000V**

PIN CONFIGURATIONS

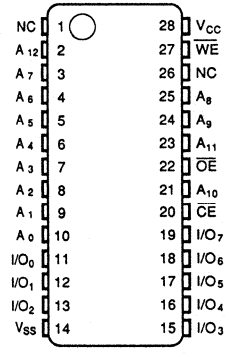
28 Pin CERDIP
Type "C" Package



28 Pin Plastic DIP
Type "P" Package



28 Pin SOIC
Type "J" Package



32 Pin PLCC
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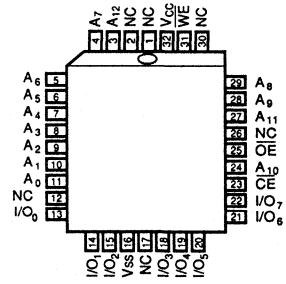

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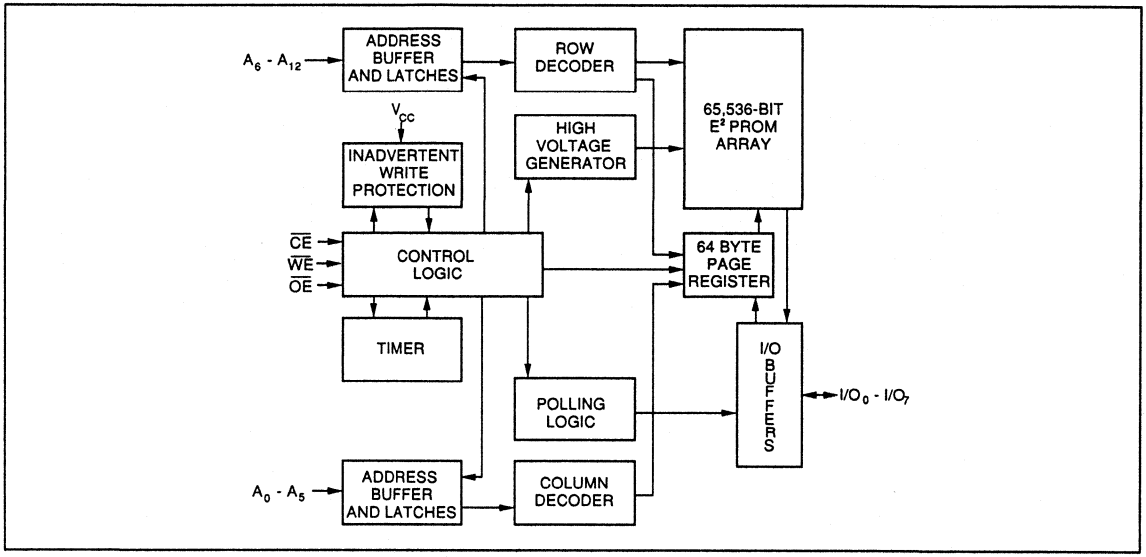

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The XL28C64B contains (128) 64-byte pages. Address lines A_6-A_{12} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one nonvolatile write cycle must be on the same page (A_6-A_{12} must remain unchanged). Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written to any given byte when the nonvolatile write cycle begins is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to initiate the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. An internal byte-load timer is started on the falling edge of the controlling line. The timer provides a 100µs window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period.

When the byte-load timer times out, additional external byte-load cycles are ignored and data is automatically transferred from the page buffer to the E^2PROM array through an internally managed nonvolatile write cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

An internal write-flag is set on the first byte-load of each write cycle. Data pins remain in a high impedance state except during a byte-load (when they contain the forced input data) or during a $\overline{DATA}$ polling read (see below). When the high voltage cycle is completed, the write-flag is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 200µA with CMOS level inputs.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to the Mode Selection chart.)

DEVICE OPERATION—SOFTWARE CONTROL

Under software control, the XL28C64B offers 5V-only data protection and chip erase. Software control is accomplished by byte-load sequences involving specific address and data patterns.

Short command sequences require three byte-loads; long sequences require six byte-loads. Whenever one of these sequences is recognized in a write operation, it is executed as a software command sequence, and any preceding byte-loads are lost.

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IL}	V_H	V_{IL}	Chip Erase*	Data In = X	Active
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_{IL}	V_{IH}	$\overline{DATA}$ Polling	$\overline{D_7}$	Active
X	V_{IL}	X	Write Inhibit	X	Active

*Contact EXEL for details.

These address and data patterns could conceivably occur in a normal application. However, the protocol utilizes differing page addresses within one write cycle — a practice that is illegal in standard write operations.

Chip Erase Cycle
This software command sequence activates the standard chip erase, but without the high voltage input on the $\overline{OE}$ pin. Contact EXEL technical support for details.

Set Data Protection Mode (See Figure 1)
This software command sequence disables the high voltage cycle for standard writes (those controlled by the enable lines). Each set-data-protect command can be followed by data for one page of the E²PROM array. Thereafter, standard writes are disabled, and can be enabled only by a disable-data-protect command. However, additional pages can be written by the set-data-protect command.

Set Data Protect Software Command Sequence:

Byte-load	A_{12}-A_0	I/O_7-I/O_0
1	1555 (hex)	AA (hex)
2	0AAA (hex)	55 (hex)
3	1555 (hex)	A0 (hex)

When this command is recognized, the part remains in write mode. Any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting a nonvolatile data protect bit. If the data protect bit was already set—by a previous set-data-protect command—it remains set. If a power failure interrupts the operation, neither the data nor the protect bit is written.

Setting the data protect bit inhibits only the high voltage cycles of standard writes (those controlled by the enable lines); byte-load cycles are still accepted. When the byte-load timer expires, the part skips the high voltage cycle and becomes accessible to the standard read mode.

Because the data-protect-status bit is a nonvolatile E² element, protect mode status is maintained during power off.

Disable Data Protection Mode
This software command sequence re-enables the high voltage cycle of the standard write (see Figure 2). Each disable-data-protect command can be accompanied by data for one page of the E²PROM. Standard writes are then enabled, until disabled by a subsequent set-data-protect command.

Disable Data Protect Software Command Sequence:

Byte-load	A_{12}-A_0	I/O_7-I/O_0
1	1555 (hex)	AA (hex)
2	0AAA (hex)	55 (hex)
3	1555 (hex)	80 (hex)
4	1555 (hex)	AA (hex)
5	0AAA (hex)	55 (hex)
6	1555 (hex)	20 (hex)

The six byte-loads specifying this command leave the part in write mode; any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting the nonvolatile data protection. If the data protection was already disabled (by a previous disable-data-protect command), it remains disabled. If a power failure interrupts the operation, neither the data nor the data protection is written. Because the data protect status bit is a nonvolatile E² element, data protection mode status is maintained during power off.

MONITORING DEVICE STATUS

Because the byte-load timer and its high voltage cycle are completely under the control of the XL28C64B, a status register allows the host system to monitor device status.

Status Register
Any read performed during the nonvolatile write cycle is interpreted as a status register read. (Reading the status register has no effect on the byte-load timer, byte-load flags, high voltage cycle or the contents of the page buffer.)

The status of a write operation is monitored in one of two ways; Toggle Polling or $\overline{DATA}$ Polling. While the nonvolatile write cycle is in progress, O_6 will toggle between 0 and 1 on successive reads; O_7 will hold the complement of bit 7 of the last byte loaded. When the write-latch is reset, the write operation is complete. O_6 and O_7 become bits 6 and 7 of the actual byte location. Bit 6 will no longer toggle; bit 7 will no longer be a complement.

While the write cycle is in progress, there is additional information available from the status register, as follows:

Bits 0 and 1: Reserved for use by factory
Bit 2: Always 0
Bit 3: 1 means data protect feature is enabled
0 means data protect feature is disabled
Bit 4: Always 1
Bit 5: Reserved for use by factory
Bit 6: Used in Toggle polling
Bit 7: Used in $\overline{DATA}$ Polling

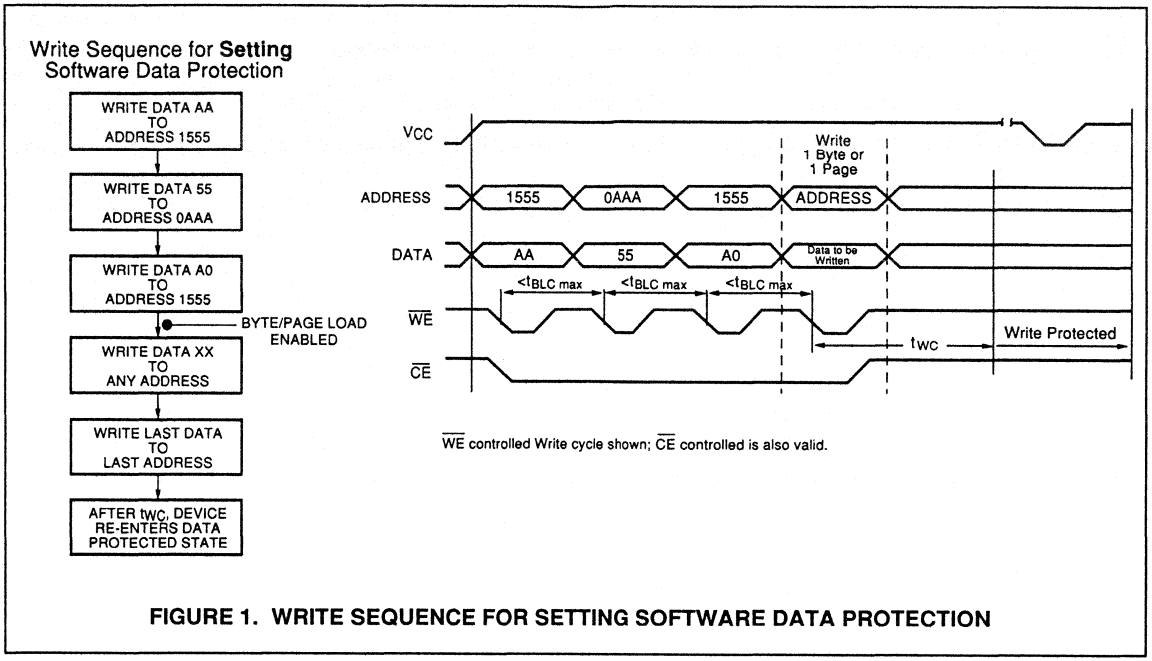


FIGURE 1. WRITE SEQUENCE FOR SETTING SOFTWARE DATA PROTECTION

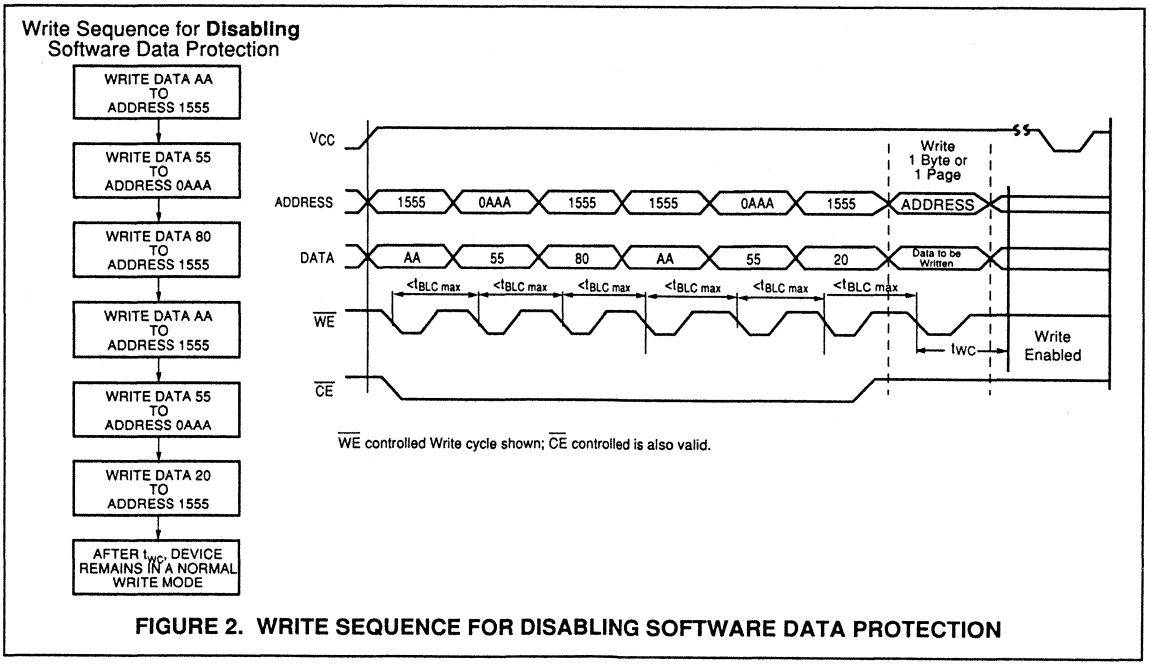
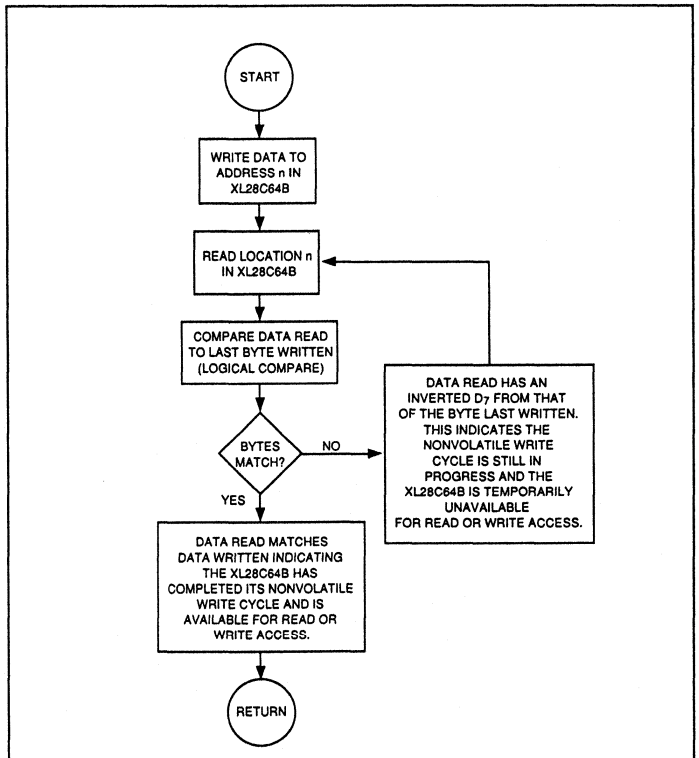


FIGURE 2. WRITE SEQUENCE FOR DISABLING SOFTWARE DATA PROTECTION

$\overline{\text{DATA}}$ Polling

The XL28C64B provides a feature named $\overline{\text{DATA}}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C64B is busy executing its nonvolatile write cycle will be interpreted as a $\overline{\text{DATA}}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{\text{DATA}}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or the nonvolatile cycle timing.

$\overline{\text{DATA}}$ polling is a simple software technique used to determine the status of the XL28C64B. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C64B. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers output the contents of the status register, during a read cycle. I/O_7 is set to output the complement of the value of the MSB of the last byte written to the XL28C64B when a read command is asserted.



$\overline{\text{DATA}}$ POLLING SUBROUTINE

The procedure is quite simple. The system simply reads the location last written to in the XL28C64B and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C64B is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to await the 5ms (max.) period specified, and enabling accelerated device loading operations.

WRITE PROTECT MECHANISMS

The XL28C64B features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise.

$\overline{OE}$ Write Inhibit

If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

V_{CC} Lockout

The XL28C64B has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL28C64B and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort nor affect nonvolatile write cycles already in progress, yet inhibits new cycles from being initiated.

Power-Up Write Enable Delay

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. Write operations are inhibited until 1ms after V_{CC} reaches 3.0V to allow the system to stabilize while blocking potential inadvertent write commands.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

Data Protection Mode (Software Controlled)

The XL28C64B can be placed in a write-disabled mode through software control.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) .....300°C
Supply Voltage .....0 to 6.5V
Voltage on Any Pin* .....-1.0 to +7.0V
Voltage on $\overline{OE}$ Pin* .....-1.0 to +15.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC} = 5V ±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	Vcc Current — Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH} I/O's = open A_0-A_{12} toggling at 5MHz		60	mA
I_{SB}	Vcc Current — Standby (TTL)	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{12} = Vcc		2	mA
I_{SBC}	Vcc Current — Standby (CMOS)	$\overline{CE}$ = $\overline{WE}$ V cc-.2V $\overline{OE}$ = V ss+0.2V I/O's = open A_0-A_{12} = Vcc		150	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc		10	µA
I_{LO}	Output Leakage — Standby	V_{OUT} = GND to Vcc $\overline{CE}$ = V_{IH}		10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA I_{OH} = -10µA	2.4 Vcc-0.1		V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figures 3 and 4)

T_A=0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%

Symbol	Test	XL28C64B-120		XL28C64B-150		XL28C64B-200		XL28C64B-250		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		200		250		ns
t_{AA}	Address Access Time		120		150		200		250	ns
t_{CE}	Chip Enable Access Time		120		150		200		250	ns
t_{OE}	Output Enable Access Time		50		60		75		100	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	15		15		15		15		ns

WRITE CYCLE (See Figures 5, 6 and 7)

T_A=0°C to +70°C for the XLS28C64B or -40°C to +85°C for the XLE28C64B, V_{CC}=5V±10%

Symbol	Test	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{BLC}	Byte Load Cycle	.120	100	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	0		ns
t_{DV}	Data Valid Time		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

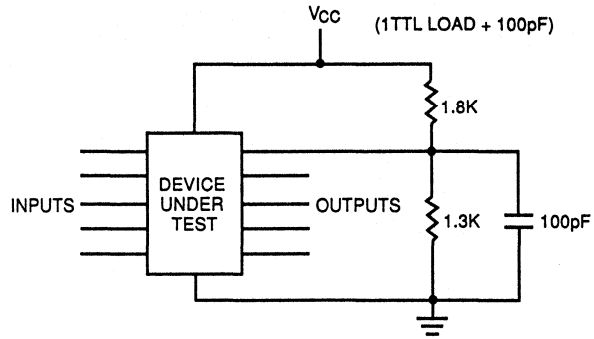


FIGURE 3. AC TEST CONDITIONS

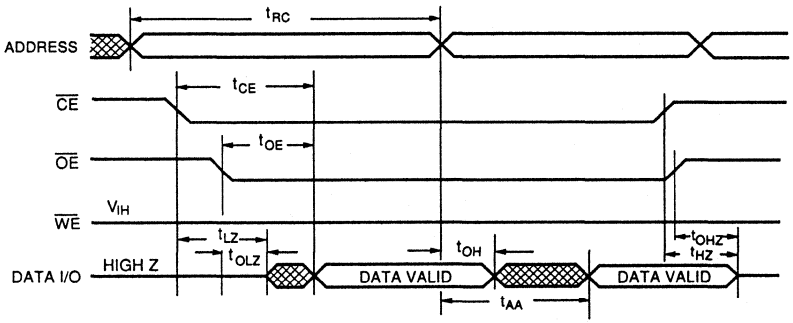


FIGURE 4. READ CYCLE TIMING

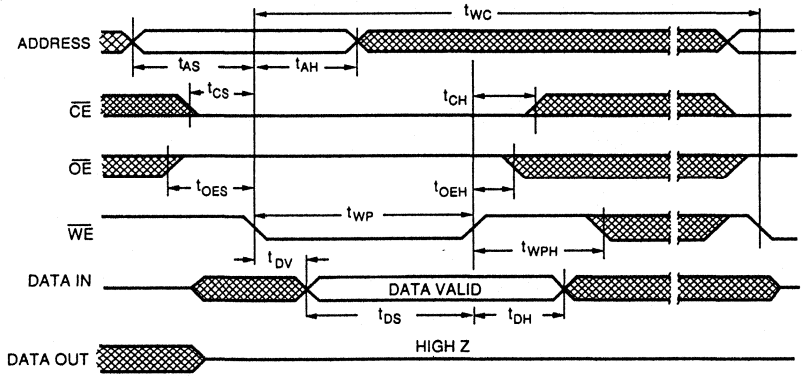


FIGURE 5. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

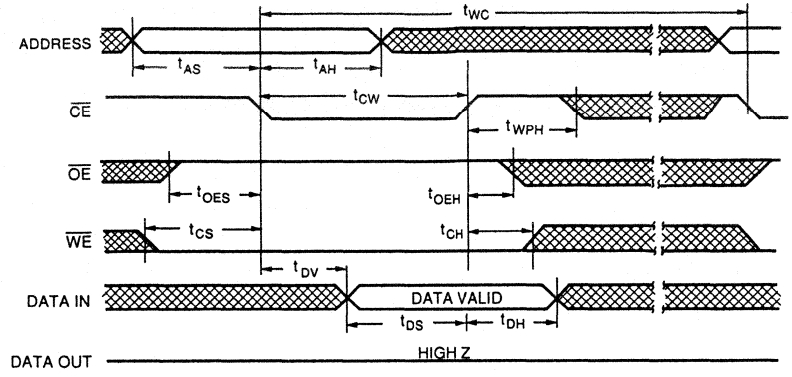


FIGURE 6. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

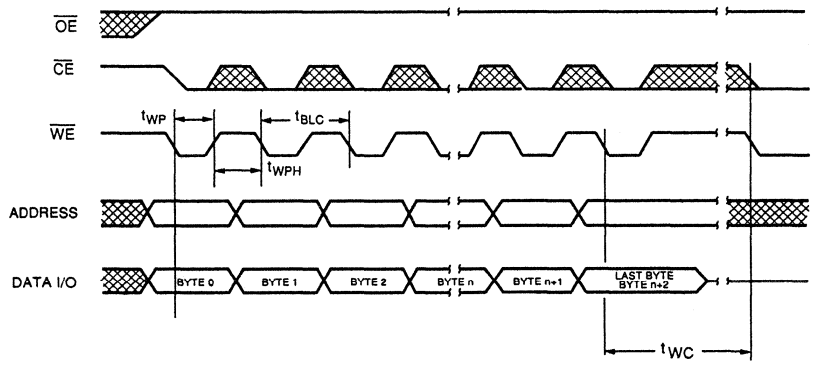


FIGURE 7. PAGE MODE WRITE CYCLE TIMING

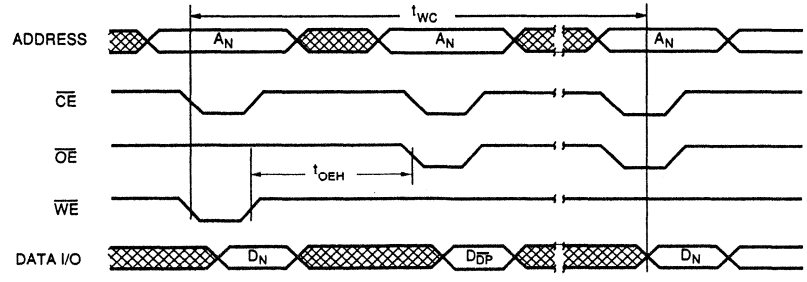


FIGURE 8. $\overline{DATA}$ POLLING TIMING

Preliminary

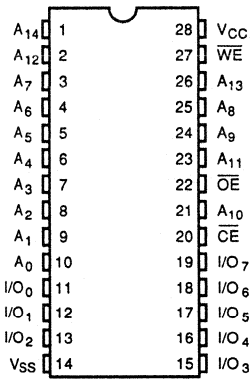
32K X 8 CMOS Electrically Erasable PROM
5ms Nonvolatile Write Cycle

FEATURES

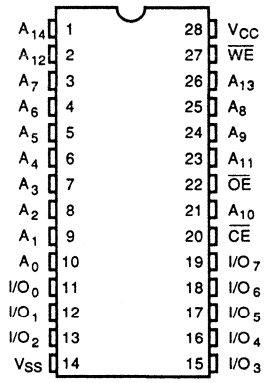
- **Fast Read Access Times**
  - **— 150ns, 200ns and 250ns**
- **Low CMOS Power Consumption**
  - **— 60mA (Active)**
  - **— 150µA (Stand By)**
- **5 Volt-only Operation**
  - **— Including write**
- **Fast Nonvolatile Write Cycle**
  - **— Internally latched data and address**
  - **— 120ns byte-load cycle**
  - **— 5ms (max.) nonvolatile write cycle**
- **Self-Timed Writes**
  - **— Effective 75µs/byte write**
  - **— 64 byte page input buffer**
  - **— Auto-erase before write**
  - **— $\overline{\text{DATA}}$ Polling**
  - **— Toggle bit**
- **Software Mode Control**
- **Automatic Page Write Mode**
  - **— 64 byte page size**
  - **— 10ms page write time**
- **On-chip Inadvertent Write Protection**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **ESD Protected to 2000V**

PIN CONFIGURATIONS

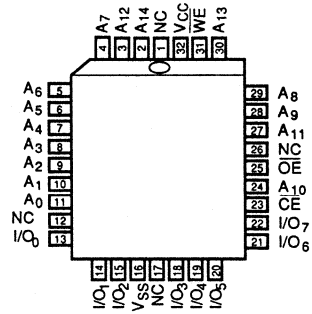
28 Pin CERDIP
Type "C" Package



28 Pin Plastic DIP
Type "P" Package



32 Pin PLCC
Type "D" Package



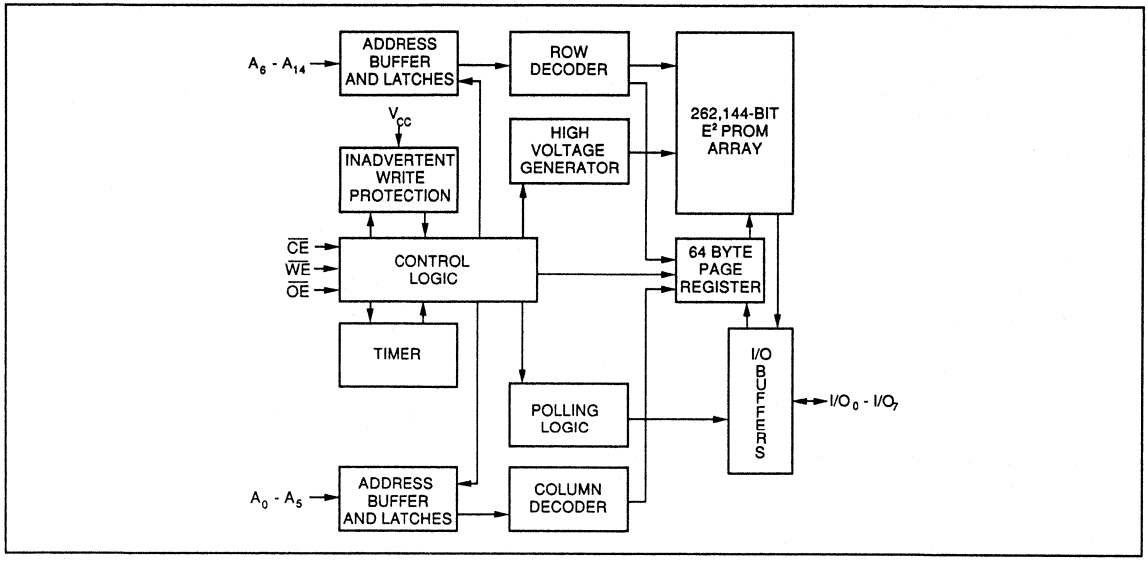
OVERVIEW

The XL28C256 is a full-featured, 32K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 256K devices, but offers improved speed and power efficiency. Read access times can be as low as 150ns; standby current, less than 100µA. It features a page-wide input buffer and improved protection against inadvertent writes. Operating modes function from a single 5V power supply, and the XL28C256 is manufactured with EXEL's proven double-metal, 1.4µ CMOS process. In order to speed up erase and write operations, a 64-byte page reprogramming function is provided.

PIN NAMES

A_0-A_{14}	Address Inputs
I/O_0- I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

BLOCK DIAGRAM



The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and supplemental inadvertent write protection circuitry. It fits into standard SRAM sockets and responds to typical SRAM write commands.

The fully-automatic 64-byte page-write allows the entire memory to be programmed in less than 0.65 sec. Internal latches, for address and data, free the system bus during the 5ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read access time, adding to system performance.

Inadvertent writes are inhibited by a wide range of protections built into the XL28C256. A low V_{CC} lockout feature disables nonvolatile write cycles when V_{CC} drops below 3.5V (V_{WI}) (typical). Additionally, the XL28C256 features power-on reset and noise protected $\overline{WE}$.

The XL28C256 is compatible with existing 256K E^2PROMs—both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E^2PROMs as well.

APPLICATIONS

The nonvolatile storage in the XL28C256 replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in telephones and facsimile machines. The XL28C256 is ideal in applications that are self-adapting, such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

ENDURANCE and DATA RETENTION

The XL28C256 is designed for applications requiring up to 10,000 data changes per E^2PROM byte ensuring a guaranteed endurance of over 325 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

DEVICE OPERATION

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard user-operating modes for the XL28C256. Chip erase (typically executed during test procedures) requires a higher supply voltage on the $\overline{OE}$ input pin. This conforms with existing E^2PROM standards.

Read Mode
Data is read from the XL28C256 by bringing both $\overline{CE}$ and $\overline{OE}$ LOW while keeping $\overline{WE}$ HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E^2PROM array. Read access time is measured from the latter of either the time when the controlling line goes LOW ($\overline{CE}$ or $\overline{OE}$), or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle.

Write Mode
The XL28C256 uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent nonvolatile write cycle transfers this data in the page-buffer to the E^2PROM array without user intervention.

The XL28C256 contains (512) 64-byte pages. Address lines A_6-A_{14} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one nonvolatile write cycle must be on the same page (A_6-A_{14} must remain unchanged). Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written to any given byte when the nonvolatile write cycle begins is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to initiate the byte-load cycle. The address is latched into internal address latches upon the last falling edge of $\overline{WE}$ or $\overline{CE}$. An internal byte-load timer is started on the falling edge of the controlling line. The timer provides a 100µs window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period.

When the byte-load timer times out, additional external byte-load cycles are ignored and data is automatically transferred from the page buffer to the E^2PROM array through an internally managed nonvolatile write cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

An internal write-flag is set on the first byte-load of each write cycle. Data pins remain in a high impedance state except during a byte-load (when they contain the forced input data) or during a $\overline{DATA}$ polling read (see below). When the high voltage cycle is completed, the write-flag is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Standby Mode
Whenever $\overline{CE}$ is brought HIGH, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 200µA with CMOS level inputs.

Chip Erase — High Voltage Mode
The chip erase mode allows the user to erase the entire E^2PROM array with a single command. The method requires the application of high voltage (V_H) on the $\overline{OE}$ pin, with $\overline{CE}$ at a logical "0." Chip erase is initiated by a standard byte write command, but in this case, the data on the I/O pins is ignored. A byte containing all "1's" is automatically written to all locations in the E^2PROM array. (Refer to Mode Selection chart.)

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⌐‾_‾⌐	Byte Write ($\overline{WE}$ Controlled)	D_{IN}	Active
⌐‾_‾⌐	V_{IH}	V_{IL}	Byte Write ($\overline{CE}$ Controlled)	D_{IN}	Active
V_{IH}	X	X	Standby	HIGH Z	Standby
V_{IL}	V_H	V_{IL}	Chip Erase	Data In = X	Active
V_{IL}	V_{IL}	V_{IH}	$\overline{DATA}$ Polling	$\overline{D_7}$	Active
X	V_{IL}	X	Write Inhibit	X	Active

DEVICE OPERATION—SOFTWARE CONTROL

Under software control, the XL28C256 offers 5V-only data protection and chip erase. Software control is accomplished by byte-load sequences involving specific address and data patterns.

Short command sequences require three byte-loads; long sequences require six byte-loads. Whenever one of these sequences is recognized in a write operation, it is executed as a software command sequence, and any preceding byte-loads are lost.

These address and data patterns could conceivably occur in a normal application. However, the protocol utilizes differing page addresses within one write cycle—a practice that is illegal in standard write operations.

Chip Erase Mode

This software command sequence activates the standard chip erase, but without the high voltage input on the $\overline{OE}$ pin. When the byte-loads for the command are complete, all byte flag latches are set. When the byte-load timer expires, a special mass-mode high voltage cycle is performed, erasing the entire E²PROM array. The device then returns to standard read mode.

Chip Erase Software Command Sequence:

Byte-load	A_{14}-A_0	I/O_7-I/O_0
1	5555 (hex)	AA (hex)
2	2AAA (hex)	55 (hex)
3	5555 (hex)	80 (hex)
4	5555 (hex)	AA (hex)
5	2AAA (hex)	55 (hex)
6	5555 (hex)	10 (hex)

Set Data Protection Mode (See Figure 1)

This software command sequence disables the high voltage cycle for standard writes (those controlled by the enable lines). Each "set data protect" command can be followed by data for one page of the E²PROM array. Thereafter, standard writes are disabled, and can be enabled only by a "disable data protect" command. However, additional pages can be written by the "set data protect" command.

Set Data Protect Software Command Sequence:

Byte-load	A_{14}-A_0	I/O_7-I/O_0
1	5555 (hex)	AA (hex)
2	2AAA (hex)	55 (hex)
3	5555 (hex)	A0 (hex)

When this command is recognized, the part remains in write mode. Any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting a nonvolatile data protect bit. If the data protect bit was already set—by a previous "set data protect" command—it remains set. If a power failure interrupts the operation, neither the data nor the protect bit is written.

Setting the data protect bit inhibits only the high voltage cycles of standard writes (those controlled by the enable lines); byte-load cycles are still accepted. When the byte-load timer expires, the part skips the high voltage cycle and becomes accessible to the standard read mode.

Because the data protect bit is a nonvolatile E² element, protect mode status is maintained during power off.

Disable Data Protection Mode (See Figure 2)

This software command sequence re-enables the high voltage cycle of the standard write. Each "disable data protect" command can be accompanied by data for one page of the E²PROM. Standard writes are then enabled, until disabled by a subsequent "set data protect" command.

Disable Data Protect Software Command Sequence:

Byte-load	A_{14}-A_0	I/O_7-I/O_0
1	5555 (hex)	AA (hex)
2	2AAA (hex)	55 (hex)
3	5555 (hex)	80 (hex)
4	5555 (hex)	AA (hex)
5	2AAA (hex)	55 (hex)
6	5555 (hex)	20 (hex)

The six byte-loads specifying this command leave the part in write mode; any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting the nonvolatile data protection. If the data protection was already set (by a previous set data protect command), it remains set. If a power failure interrupts the operation, neither the data nor the data protection is written.

For normal, hardware-controlled writes, the data protection inhibits only the high voltage cycles; byte-load cycles are still accepted. When the byte-load timer expires, the part skips the high voltage cycle and reverts to read mode.

Because the data protection is a nonvolatile E² element, protect mode status is maintained during power off.

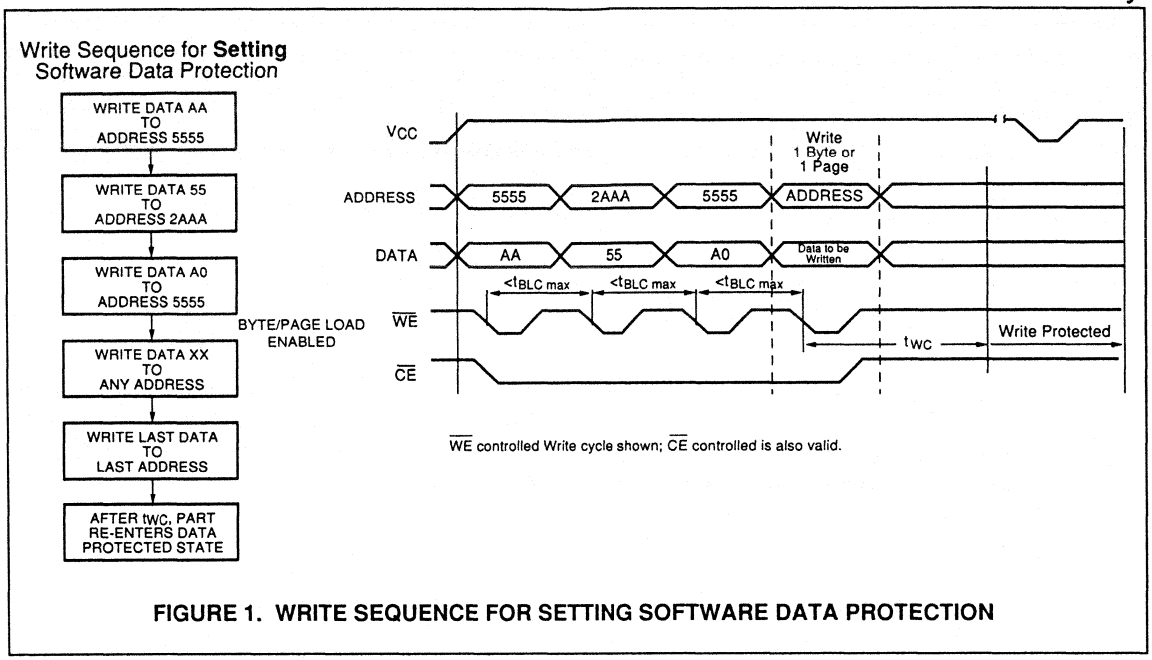


FIGURE 1. WRITE SEQUENCE FOR SETTING SOFTWARE DATA PROTECTION

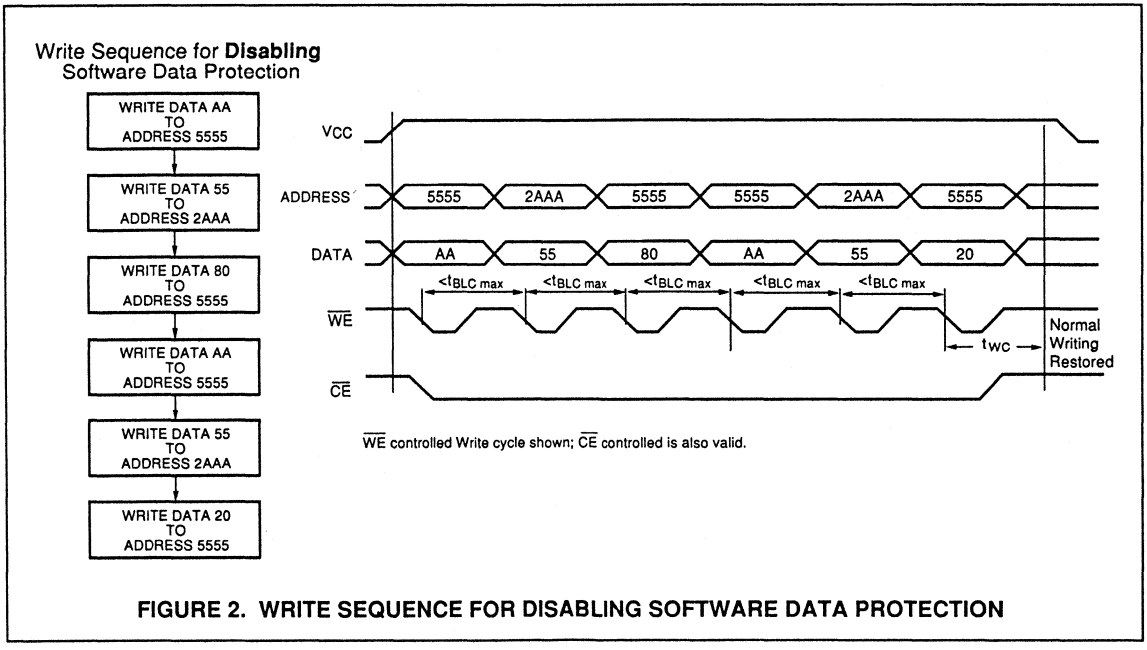


FIGURE 2. WRITE SEQUENCE FOR DISABLING SOFTWARE DATA PROTECTION

MONITORING DEVICE STATUS

Because the byte-load timer and its high voltage cycle are completely under the control of the XL28C256, a status register allows the host system to monitor device status.

Status Register

Any read performed during the nonvolatile write cycle is interpreted as a status register read. (Reading the status register has no effect on the byte-load timer, byte-load flags, high voltage cycle or the contents of the page buffer.)

The status of a write operation is monitored in one of two ways; Toggle Polling or $\overline{DATA}$ Polling. While the nonvolatile write cycle is in progress, O_6 will toggle between 0 and 1 on successive reads; O_7 will hold the complement of bit 7 of the last byte loaded. When the write-latch is reset, the write operation is complete. O_6 and O_7 become bits 6 and 7 of the actual byte location. Bit 6 will no longer toggle; bit 7 will no longer be a complement.

While the write cycle is in progress, there is additional information available from the status register, as follows:

Bits 0 and 1: Reserved for use by factory
- Bit 2: Always 0
- Bit 3: 1 means data protect feature is enabled
  0 means data protect feature is disabled
- Bit 4: Always 1
- Bit 5: Reserved for use by factory
- Bit 6: Used in Toggle polling
- Bit 7: Used in $\overline{DATA}$ Polling

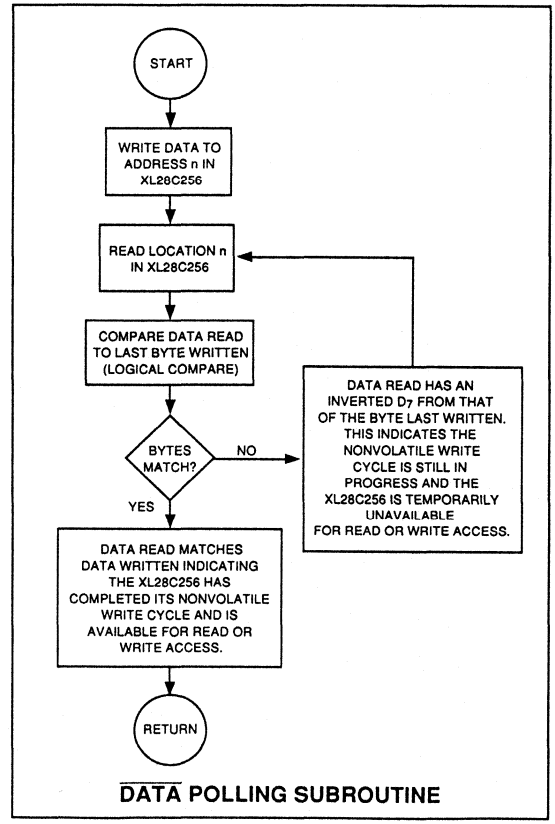
$\overline{DATA}$ Polling

The XL28C256 provides a feature named $\overline{DATA}$ polling which enables the host system to determine the status of the device through the use of the system busses. No additional hardware is required. Any attempt to read the part while the XL28C256 is busy executing its nonvolatile write cycle will be interpreted as a $\overline{DATA}$ polling read. This is performed by exercising the control pins in the same sequence as for a normal read. $\overline{DATA}$ polling cycles have no effect on the byte-load timer, contents of the data buffer or the nonvolatile cycle timing.

$\overline{DATA}$ polling is a simple software technique used to determine the status of the XL28C256. It is executed as a normal read cycle where the target byte location is the same as that of the byte last written to the XL28C256. During the 5ms (max.) period that the device requires to complete its nonvolatile write cycle, the I/O buffers output the contents of the status register, during a read cycle. I/O_7 is set to output the complement of the value of the MSB of the last byte written to the XL28C256 ***when a read command is asserted.***

This procedure is quite simple. The system simply reads the location last written to in the XL28C256 and executes a compare operation between the data thus retrieved and the original data byte written. If the compare fails, the XL28C256 is still busy with its nonvolatile write cycle. If the compare passes, the nonvolatile write cycle is complete and the device is available for read or write accesses.

This procedure is commonly used to determine the actual nonvolatile write cycle completion timing, eliminating the need to await the 5ms (max.) period specified, and enabling accelerated device loading operations.



$\overline{DATA}$ POLLING SUBROUTINE

WRITE PROTECT MECHANISMS

The XL28C256 features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise.

$\overline{OE}$ Write Inhibit

If $\overline{OE}$ is brought LOW before the $\overline{CE}$ and $\overline{WE}$ write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table on page 3. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

V_{CC} Lockout

The XL28C256 has a specialized power supply monitor circuit integrated to protect the device from inadvertent write commands asserted by the system during low V_{CC} conditions. This circuitry constantly evaluates the power supply voltage level applied to the XL28C256 and actively inhibits the initiation of nonvolatile write cycles if the applied supply voltage falls below V_{WI}. This circuitry does not abort nor affect nonvolatile write cycles already in progress, yet inhibits new cycles from being initiated.

Power-Up Write Enable Delay

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. Write operations are inhibited until 1ms after V_{CC} reaches V_{WI} to allow the system to stabilize while blocking potential inadvertent write commands.

Noise Protection

Write pulses of less than 10ns duration on the $\overline{WE}$ pin will not initiate nonvolatile write cycles.

Data Protection Mode (Software Controlled)

The XL28C256 can be placed in a write-disabled mode through software control.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin* ..... -1.0 to +7.0V
Voltage on $\overline{OE}$ pin* ..... -1.0 to +15.0V
ESD Rating 2000V
DC Output Current 5mA
*With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C for the XLS28C256 or -40°C to +85°C for the XLE28C256, V_{CC} = 5V ±10%

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I_{CC}	Vcc Current — Active (TTL)	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH} I/O's = open A_0-A_{14} toggling at 5MHz		60	mA
I_{SB}	Vcc Current — Standby (TTL)	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0-A_{14} = Vcc		2	mA
I_{SBC}	Vcc Current — Standby (CMOS)	$\overline{CE}$ = $\overline{WE}$ V cc-.2V $\overline{OE}$ = V ss+0.2V I/O's = open A_0-A_{14} = Vcc		150	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc		10	µA
I_{LO}	Output Leakage — Standby	V_{OUT} = GND to Vcc $\overline{CE}$ = V_{IH}		10	µA
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{IH}	Input High Voltage		2.0	Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400µA	2.4		V
V_H	High Voltage for Chip Erase		11.4	12.6	V

CAPACITANCE

T_A = 25°C, f = 1.0MHz

Symbol	Test	Test Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF

AC OPERATING CHARACTERISTICS

READ CYCLE (See Figures 3 and 4)

T_A=0°C to +70°C for the XLS28C256 or -40°C to +85°C for the XLE28C256, V_{CC}=5V±10%

Symbol	Test	XL28C256-150		XL28C256-200		XL28C256-250		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		200		250		ns
t_{AA}	Address Access Time		150		200		250	ns
t_{CE}	Chip Enable Access Time		150		200		250	ns
t_{OE}	Output Enable Access Time		70		80		90	ns
t_{LZ}	Chip Enable to Output in Low Z	0		0		0		ns
t_{HZ}	Chip Disable to Output in High Z	0	35	0	40	0	45	ns
t_{OLZ}	Output Enable to Output in Low Z	0		0		0		ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	45	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

WRITE CYCLE (See Figures 5, 6 and 7)

T_A=0°C to +70°C for the XLS28C256 or -40°C to +85°C for the XLE28C256, V_{CC}=5V±10%

Symbol	Test	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{BLC}	Byte Load Cycle	.120	100	µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	35		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	Chip Enable Pulse Width	50		ns
t_{OES}	Output Enable Setup Time	5		ns
t_{OEH}	Output Enable Hold Time	5		ns
t_{WP}	Write Enable Pulse Width	70		ns
t_{WPH}	Write Pulse Width High	50		ns
t_{DS}	Data Setup Time	30		ns
t_{DH}	Data Hold Time	5		ns
t_{DV}	Data Valid Time..		1	µs
t_{INIT}	Power-up Initialization Period		20	ms

Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns (1V to 2V)
Frequency	1MHz
Timing Reference Value	1.5V

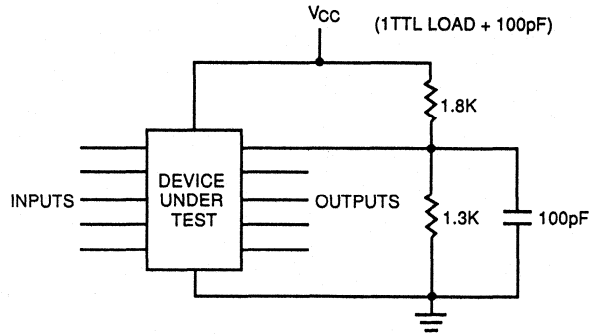


FIGURE 3. AC TEST CONDITIONS

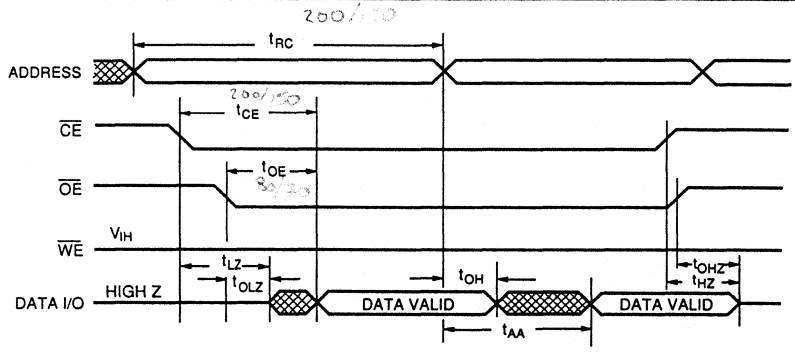


FIGURE 4. READ CYCLE TIMING

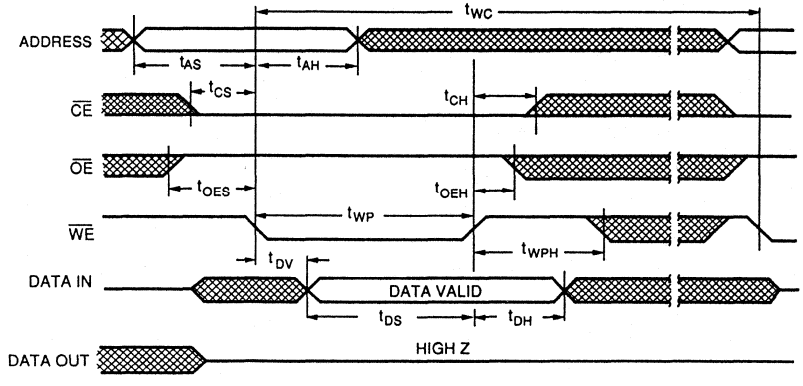


FIGURE 5. $\overline{WE}$ CONTROLLED WRITE CYCLE TIMING

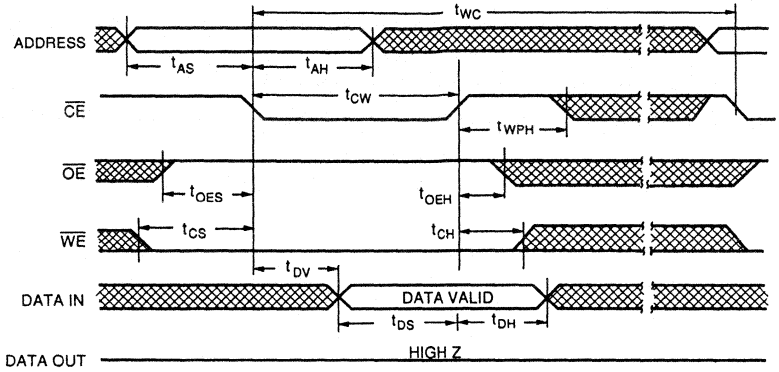


FIGURE 6. $\overline{CE}$ CONTROLLED WRITE CYCLE TIMING

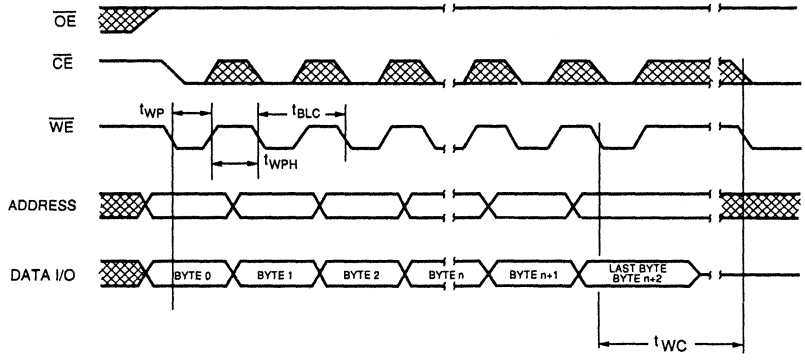


FIGURE 7. PAGE MODE WRITE CYCLE TIMING

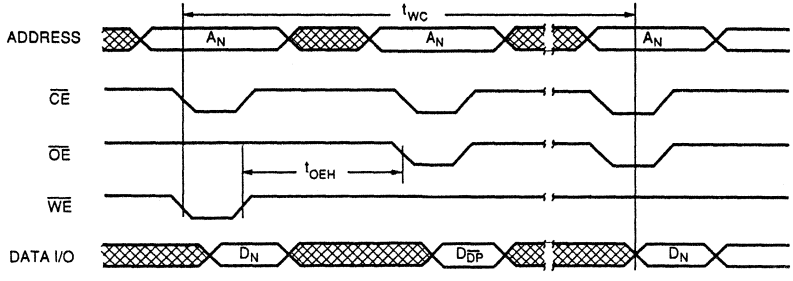


FIGURE 8. $\overline{DATA}$ POLLING TIMING

SECTION 4 Table of Contents

USING EXEL'S SERIAL E²PROMS

By: John Nagamine, Applications Engineer, August 1990

INTRODUCTION

Exel's XL93C46 - 1K bit, XL93C56 - 2K bit, and the XL93C66 - 4K bit serial E²PROMs provide a practical solution to many typical problems encountered in microprocessor applications. These problems include: data loss during a power shutdown, the absence of external address and data buses, the need for bulky and unreliable batteries for data retention during power outages, and design constraints imposed by external circuitry included to protect against inadvertent writes.

This application note discusses the usefulness of the serial E²PROMs in many applications. To illustrate this, a few examples of using the XL93C46 with common microprocessors and I/O ports are discussed.

THE XL93C46 FUNCTIONAL DESCRIPTION

The XL93C46 provides efficient nonvolatile read/write memory arranged as 64 registers of 16 bits each. The XL93C46 is fabricated in floating-gate CMOS E²PROM technology for very low active power consumption. Deselecting the device reduces power consumption further. The device is available in a 5V version which operates on a 5V ±10% power supply, as well as a 3V version, the XL93C46-3, which operates between 2.7 and 5.5 volts.

Seven 9-bit instructions control the operation of the device, which include read, write, and mode enable functions. The complete instruction set is shown in Table 1.

Since data is written into and read out of the memory serially, no address bus nor data bus is required, resulting in a minimal pin count package (8-pin), and provides a simple interface with any microprocessor-based system. The data out pin (DO) indicates the status of the device during the self-timed, nonvolatile programming cycle. If DO is a logical "0," the nonvolatile Write Cycle is still in progress. If DO is a logical "1," the Write Cycle is complete.

The automated nonvolatile Write Cycle includes a transparent erase-before-write feature eliminating the firmware overhead of erasing a memory location prior to writing to it as was required in earlier versions of serial E²PROMs. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. This state is attained by issuing a separate "Write Enable" (WRN) instruction. (Refer to Table 1.) Data is written in 16 bit words into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chips nonvolatile write cycle.

TABLE 1. THE 93C46 INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data
READ	1	10	(A_5-A_0)	
WEN (Write Enable)	1	00	11XXXX	
WRITE	1	01	(A_5-A_0)	D_{15}-D_0
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0
WDS (Write Disable)	1	00	00XXXX	
ERASE	1	11	(A_5-A_0)	
ERAL (Erase All Registers)	1	00	10XXXX	

READ

The READ instruction is the only instruction that outputs data through the DO pin. After the read instruction and address have been decoded, data is transferred from the addressed memory register into a serial shift register. (Note that one logical "0" bit precedes the actual 16-bit output data string.) The data bits output on the DO pin change during the low-to-high transitions of SK.

The XL93C46 has been designed to ensure that data read operations are reliable in low voltage environments. The device is guaranteed to provide valid data during read operations with V_{CC} as low as 2.0 volts. This is ideal for battery operated environments demanding low voltage operation.

The XL93C46 also has auto increment read capabilities. This feature provides a continuous stream of memory content in response to a single read operation. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 16 bits of the addressed word have been clocked out, the data in consecutively higher address locations is output. The addresses will wrap around while CS is HIGH until the Chip Select (CS) control pin is brought LOW. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

ERASE

After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH (after a minimum of t_{CS}), will cause DO to indicate the READY/$\overline{\text{BUSY}}$ status of the chip: "1" indicates the erase cycle is complete and the device is ready for another instruction; "0" indicates the erase cycle is still programming the addressed register. The XL93C46 also has an Erase All instruction. This full chip erase feature is provided for programming and testing ease. Erasing the entire chip results in the setting of all bits in the memory array to a logical "1."

WRITE

The Write instruction string includes 16 bits of data to be written into the specified register. After the last data bit has been clock into DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the internal self-timed nonvolatile programming cycle.

After a minimum wait of 250ns from the falling edge of CS (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip. (Note: The combination of CS HIGH, DI HIGH, and the rising edge of SK, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.) Prior to the execution of a WRITE instruction, the device must be write enabled. This is accomplished by issuing a separate Write Enable instruction (WEN). Refer to the instruction set in Table 1.

The XL93C46 also includes the Write All instruction. This instruction programs all registers with the data pattern specified in the data field of the Write All instruction. (See Table 1.) The WRALL instruction includes a sequence of DON'T CARE bits which constitute its address field. As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (t_{CS}), the DO pin provides the READY/$\overline{\text{BUSY}}$ status of the chip.

USING THE XL93C46 WITH MICROPROCESSORS

Typical byte wide E²PROMs require a separate address bus and data bus to interface with the MPU. Most single-chip microcomputers have no external data nor address bus, and often require nonvolatile storage of data to maintain the system integrity in the event of power loss. One solution is to employ a single-chip microcomputer with a power down standby mode for its on-chip RAM. However, this solution requires a battery which is inherently low in reliability and longevity, and has demanding power transition circuitry requirements.

The XL93C46 can interface with most microprocessor systems with only four connections in addition to the power and ground. The following illustrations in Figure 1 to Figure 5, display the connections to the 6500/1, 8051, and the 6805 microcontrollers, and the 6522 and 8255 peripheral I/O ports.

SUMMARY

Exel's serial E²PROM family offers a variety of solutions to many applications. It is easy to control with any microprocessor and offers a small pin out package, simple operation, low power consumption, nonvolatile memory storage, and a completely software interface to most applications.

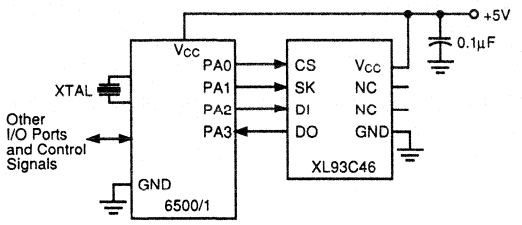


Figure 1. Interfacing the XL93C46 with the 6500/1

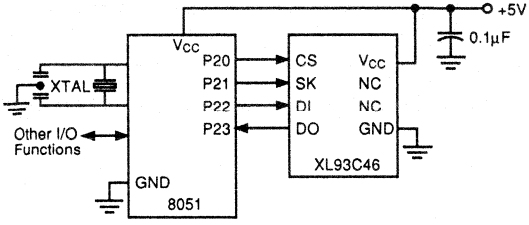


Figure 2. Interfacing the XL93C46 with the 8051 mController

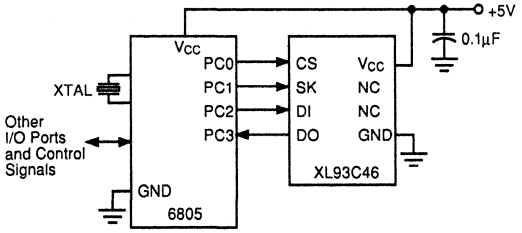


Figure 3. Interfacing the XL93C46 with the 6805 mController

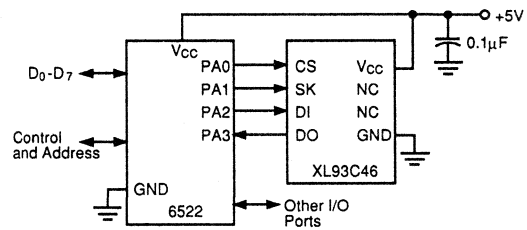


Figure 4. Interfacing the XL93C46 with the 6522 I/O

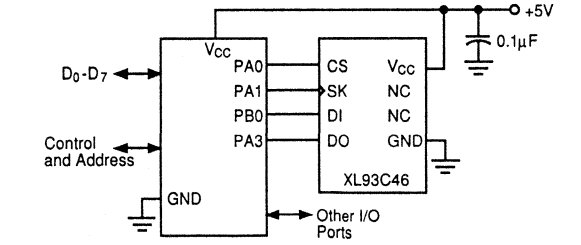


Figure 5. Interfacing the XL93C46 with the 8255 I/O

COMMON E²PROM QUESTIONS ANSWERED

By: John Nagamine, Applications Engineer, September 1990

INTRODUCTION

A wide variety of applications exist for the E²PROM. They include control stores, look up tables, calibration constants, configuration parameters, user programmable software storage, and artificial intelligence systems which update their algorithms as they learn. All of these applications require nonvolatile yet writable memory. Exel's E²PROMs offer additional features which make applications simple to implement. Among these features are:

- 5 Volt Only Operation
- 10,000 Rewrites per Byte
- 10 Year Data Retention
- TTL Compatible Interface
- Fast TTL Level Byte Write Operations
- Self-Timed Write Cycle with On-Chip Latches
- DATA Polling to Minimize Write Cycle Times
- Noise Filtered Control Pins
- Inadvertent Write Protection
- Page Write Features

Contained in this application note are commonly asked questions which arise when designing with E²PROMs. Clarification of these few questions may aid other designers in new application ideas and solutions.

Question 1: Is there any easy way to protect data on the E²PROM device from being overwritten by inadvertent Write commands generated on the system bus during power transitions?

Answer 1: Yes. Exel's E²PROMs provide a variety of features to prevent this occurrence. First, there is an on-chip voltage sensor which monitors the supply voltage level and disables the internal write circuitry whenever V_{CC} is out of range. Note the V_{CC} Protect voltage for the XL2864A and XL2865A is 4 volts, for the XL28C16A is 3 volts, and for the XL28C64 is 3.8 volts. Second, noise protection prevents write pulses of less than 20ns duration on the $\overline{WE}$ pin. This prevents spikes and glitches that might otherwise initiate an inadvertent Write Cycle. Third, Exel's E²PROMs have power up Write protection. At power up, write operations are inhibited until V_{CC} is stable and sufficiently HIGH. Write operations are inhibited until 1ms after V_{CC} reaches 3 volts to allow the system power supplies to stabilize.

Question 2: The Standby current requirements of Exel's NMOS E²PROMs are too great for a portable CMOS system. If their V_{CC} line is switched open, will their I/O lines load the bus?

Answer 2: No. The output driver for each I/O pin is composed of a matched series pair of enhancement mode NMOS FETs as shown below in Figure 1.

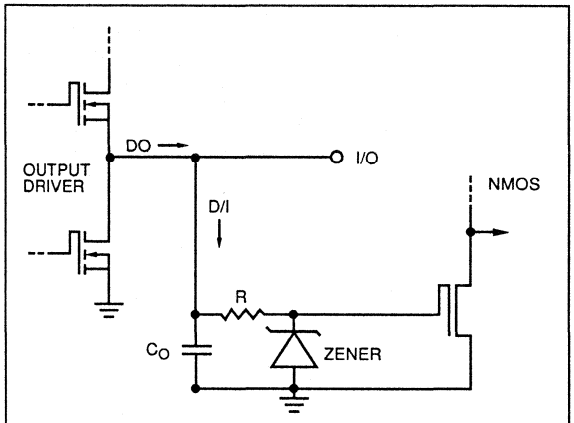


FIGURE 1. NMOS I/O CONFIGURATION

When the device is not selected, the drivers are in the HIGH-Z mode. When the device has no power applied, these FETs are not conducting so the output pin presents a HIGH-Z load to the bus. Thus, there is no loading beyond the input capacitance, and minimal leakage current. The lack of an upper clamp diode allows for signals to be safely applied to the device when the V_{CC} line is open.

Many remote and portable systems requiring maximum power efficiency use a low on-resistance Power FET to power up and power down the NMOS device under system control, as shown in Figure 2.

The Power FET must remain enabled for at least 10ms after the initiation of the most recent Write Cycle so that the NMOS E²PROM power supply remains within the specified operating voltage range for the duration of the nonvolatile Write Cycle. Making use of $\overline{DATA}$ Polling and the typical

Write Cycle time of 7ms, power consumption can be further reduced. Since the device does not load the bus during this period, the system is able to perform other tasks while the nonvolatile Write Cycle proceeds.

In applications which require further power efficiency, the NMOS devices can be replaced with operationally equivalent CMOS devices. Unlike the data lines of the NMOS parts which do not load the bus when the power supply is shut off, the CMOS parts may sink substantial current through the DATA pins if the DATA bus remains active when the power supply is removed. In order to prevent this, it is recommended that the power switching transistor be removed; thus continuously power in the CMOS device. Additionally, the extremely low power consumption of CMOS devices does not adversely affect system power consumption.

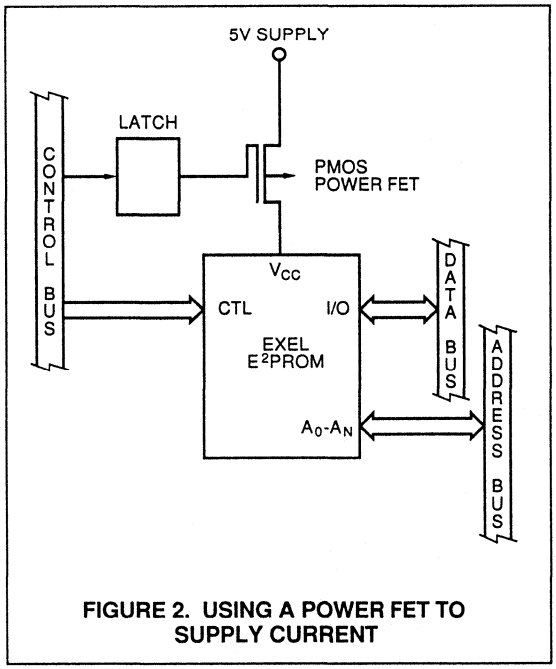


FIGURE 2. USING A POWER FET TO SUPPLY CURRENT

Question 3: The Maximum nonvolatile Write Cycle period is specified over the temperature range as 10ms on the XL2804A and the XL2816A. What is the typical time required and how might it be utilized?

Answer 3: Typically, these devices complete the nonvolatile Write Cycle in less than 7ms. The Write Cycle is initiated by applying a LOW to both $\overline{WE}$ and $\overline{CE}$ while $\overline{OE}$ is HIGH. The address inputs are latched into the device on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, to specify the byte location that is to be written. Data on the I/O pins is then latched into the device by bringing either $\overline{WE}$ or $\overline{CE}$ HIGH. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL2804A will automatically erase the selected byte and write the new data in less than 10ms. The system is freed for other functions during this period. The I/O pins will be in a high impedance state while the write operation is in progress.

The XL28C16A, XL2864A, XL2865A, XL28C64 , and the XL28C256 have software features designed into the device for the specific purpose of making use of the typical Write Cycle times. $\overline{DATA}$ Polling inverts D7 of the last byte written, and routes it to the output buffer while the device is internally occupied. This way the user simply reads the last address written to and compares the data to the last data written. When the values match, the nonvolatile write cycle is complete and device may be written to again.

Question 4: How do the Read Access and Write Cycle times vary with temperature?

Answer 4: Exel's maximum and minimum specifications are guaranteed over the full operating temperature range of the device. These values are established under worst case conditions and specified under a conservative margin. Thus, due to the worst case conditions and conservative margins, Exel's performance characteristics are actually much better than indicated by specifications. In terms of actual parameter variation, the Read Access times and the Write Cycle times for both NMOS and CMOS parts increase with rising temperature. Thus, worst case conditions for both read and write operations occur at high temperatures.

Question 5: Will signals applied to an NC (No Connect) pin damage the device?

Answer 5: No. The NC pins are not bonded and consequently have no electrical connections to the actual device.

Question 6: How much drive current is required to hold the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs LOW?

Answer 6: The input configuration of Exel's NMOS and CMOS E²PROMs are shown in Figures 3 and 4 respectively.

Only the leakage current, (10µA max.) and enough charge for the 6pF input capacitance, must be driven to either the NMOS or CMOS devices.

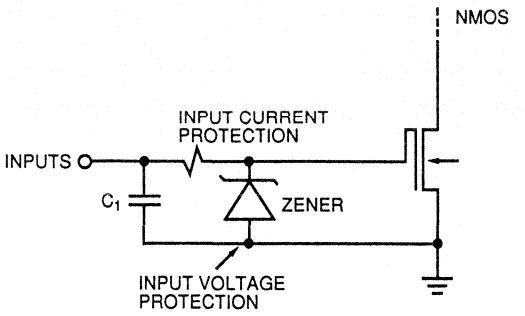


FIGURE 3. NMOS INPUT CONFIGURATION

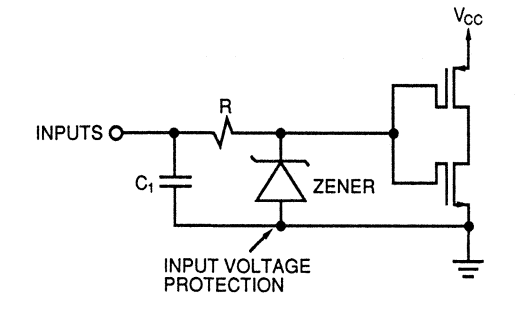


FIGURE 4. CMOS INPUT CONFIGURATION

Question 7: Can the E²PROM be read during the non-volatile Write Cycle?

Answer 7: No. During the internally timed Write Cycle, the device inputs are inhibited and its output pins are in a high impedance state. Once the Write Cycle is complete, (typically 7ms) normal data access may be resumed. DATA Polling, a feature available on the XL28C16A, XL2864A, XL28C64, XL2865A and the XL28C256, allows detection of the end of the Write Cycle. This is accomplished by allowing the system to monitor the device status via system busses using a simple read and compare operation.

Question 8: When interfacing the Exel E²PROMs with a CMOS system, are pullup resistors required?

Answer 8: Yes. The V_{OH} min. specification on the Exel NMOS devices is 2.4V and the V_{IH} min. for CMOS technology is 3.5V in a 5V environment. In this case, the 2.4V HIGH outputs from the NMOS technology may not be recognized as a HIGH by the CMOS inputs. To ensure that the NMOS E²PROM's HIGH outputs are recognized by the CMOS inputs, the pullup resistors are necessary. When driving NMOS technology with a CMOS system, no pullup resistors are needed. The CMOS outputs are completely compatible with the NMOS inputs.

Question 9: When using an entire bank of E²PROMs on a common bus, if some are enabled and some disabled, will all the chips be affected by a high voltage chip erase cycle?

Answer 9: No. Only those chips which are enabled will be cleared.

Question 10: During the Read cycle, Exel's E²PROM outputs go LOW before stabilizing with valid data. Although the data is valid long before the specified access time, is this phenomenon normal?

Answer 10: Yes. This operation is normal when clocking with $\overline{CE}$. While $\overline{CE}$ is HIGH, the device is in standby with the output buffers and sense amps turned off. When $\overline{CE}$ goes LOW, the output buffers are turned on and the sense amps are reading a LOW until the actual cell data reaches them. Therefore it is normal for the valid data to be preceded by a brief LOW output.

Question 11: When using the high voltage Chip Erase function on EXEL E²PROMs to erase data, could a highly skilled technologist detect what the original data was prior to erasure if given enough resources?

Answer 11: No. The floating gate storage mechanism is driven to complete saturation when programmed, and all free electrons are removed upon erasure. No trace of a previous state is left when a cell changes state. This makes Exel E²PROMs ideal for high security applications.

Question 12: When using several E²PROMs to form a contiguous address space, does the self-timed feature allow the user to write to each of them independently during a single nonvolatile Write Cycle?

Answer 12: Yes! The latches on the E²PROM free the system busses for the duration of the Write Cycle. 99.98% of the 10ms Write Cycle can be spent executing other system tasks, which could include initiating Write Cycles to the other E²PROMs not in the nonvolatile Write Cycle mode. This method of programming achieves very highly effective byte write speeds in multiple device systems.

Question 13: Does the 90C21, 93C56 and the 93C66 require an 'extra' clock to precede command sequences?

Answer 13: These devices require a falling edge of SK to initiate a command. Figure 5 illustrates this falling edge timing. If the clock is LOW when disabled, an 'extra' clock pulse is required to precede the command sequence on the DI pin. Figure 6 shows this extra clock pulse. This extra clock pulse will provide the falling edge required to begin commands.

Unlike the XL90C21, 93C56, and the XL93C66, the 93C46 does not require this falling edge. See Figure 7 for the XL93C46 instruction timing. An extra clock pulse will not affect the XL93C46 operation as long as the extra clock loads a "0" on the DI pin. (A "0" which precedes the start bit does not affect the operation of the serial devices.)

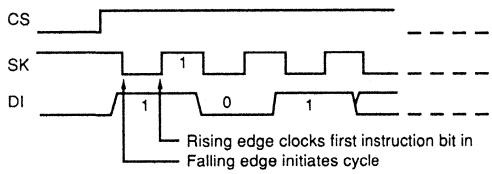


FIGURE 5. 93C56 WRITE CYCLE

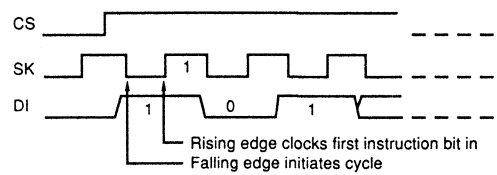


FIGURE 6. 93C56 WRITE CYCLE

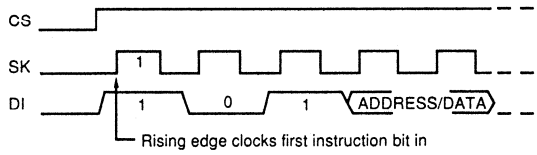


FIGURE 7. 93C46 WRITE CYCLE

DATA SECURITY — USING THE EXEL SECURE SERIAL E²PROM

By: John Nagamine, Applications Engineer, September 1990

INTRODUCTION

The XL93CS46 is Exel's secure serial 1K Electrically Erasable PROM. This device is well-suited for applications needing nonvolatile, yet writable memory requiring protection from unauthorized data alteration. The XL93CS46 offers selective write protection through the use of an on-chip protect register. This allows the device to be configured into both read-only memory (ROM) and E²PROM functional blocks. See Figure 1 below.

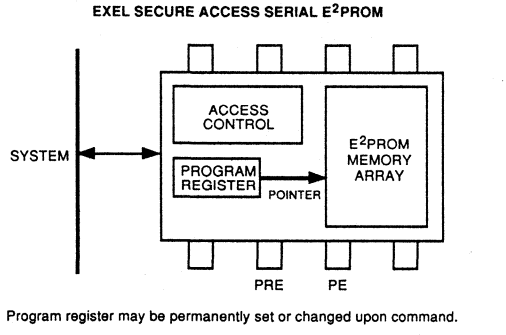
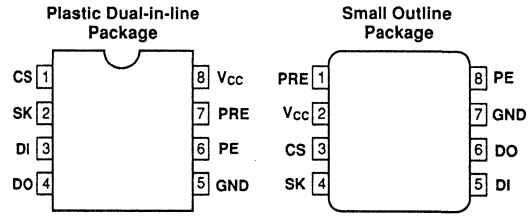


FIGURE 1. XL93CS46 SECURE ACCESS SERIAL E²PROM MEMORY ARRAY

This application note discusses the usefulness of having both ROM and E²PROM available to a system. After a brief overview of the XL93CS46, three applications which utilize the ROM/E²PROM capabilities of the part are discussed.

XL93CS46 FUNCTIONAL OVERVIEW

The XL93CS46 is a 64 by 16-bit secure serial E²PROM which exhibits extremely low power consumption. The device is available in both 5V only and 3V to 5V versions. Operation at low voltage is ideal for battery and power critical applications. The serial protocol provides a undemanding system interface structure allowing the device to be easily designed into microcontroller and microprocessor systems. Little or no support logic is required in most applications. The serial interface also allows the device to fit into a small 8-pin package, minimizing board space requirements. The pinout diagram is shown in Figure 2 below.



PIN NAMES

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
Vcc	Power Supply

FIGURE 2. XL93CS46 CHIP DIAGRAM

The XL93CS46 is controlled by twelve 9-bit instructions, each beginning with a logical "1" (the start bit). The start bit is followed by the opcode (2 bits), the address field (6 bits), and the data, in the case of a write instruction. The full set of instructions is shown in Table 1. Instructions are clocked in serially on the DI pin.

XL93CS46 INSTRUCTION SET

Instruction	Start Bit	OP Code	Address	Input Data	PRE Pin	PE Pin
READ	1	10	(A_5-A_0)		0	X
WEN (Write Enable)	1	00	11XXXX		0	1
WRITE	1	01	(A_5-A_0)	D_{15}-D_0	0	1
WRALL (Write All Registers)	1	00	01XXXX	D_{15}-D_0	0	1
WDS (Write Disable)	1	00	00XXXX		0	X
PRREAD (Protect Register Read)	1	10	XXXXXX		1	X
PREN (Protect Register Enable)	1	00	11XXXX		1	1
PRCLEAR (Protect Register Clear)	1	11	111111		1	1
PRWRITE (Protect Register Write)	1	01	(A_5-A_0)		1	1
PRDS (Protect Register Disable)	1	00	000000		1	1
ERASE REGISTER	1	11	(A_5-A_0)		0	1
ERAL (Erase All Registers)	1	00	10XXXX		0	1

AUTO INCREMENT READ INSTRUCTION

The READ instruction uses an address pointer that automatically increments when all 16 bits in one register have been clocked out. If clocking continues, successive registers are accessed and exported through DO, allowing the XL93CS46 memory to dump its entire data content in response to a single read instruction. Data can be read as a continuous data stream or as individual registers, providing from 16 to 1024 bits of data.

WRITE INSTRUCTION

The self-timed WRITE cycle (one register per write) includes an automatic erase-before-write feature. To protect against inadvertent writes, the WRITE instruction is accepted only when Write Enabled, when Program Enable pin (PE) is held HIGH, and only if the asserted register address is less than the address in the Protect Register. Data is written in 16 bit words into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip. (See Write Cycle Status.)

THE WRITE CYCLE STATUS

After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW to initiate the nonvolatile Write Cycle. After a minimum wait of 250ns (t_{CS}), if CS is brought HIGH, DO will indicate the READY/$\overline{\text{BUSY}}$ status of the chip: logical "0" indicates that programming is still in progress; a logical "1" indicates that the selected register has been written, and the part is ready for another instruction.

THE PROTECT REGISTER

The incorporation of the protect register in the XL93CS46 allows the device to function as ROM and E²PROM simultaneously. ROM is a requirement when the integrity of data stored in the device must be maintained. Any range of registers can be protected against data modification by programming the protect register. This register holds the address of the lowest memory register of the array region to be protected. The value in the Protect Register can be permanently set, ensuring that the selected range of ROM

registers can never be altered. The Protect Register can also be set impermanently with the flexibility to change it in some future moment. The distribution of ROM and E²PROM regions in the device is determined by the address in the Protect Register. The ideal ratio of ROM to E²PROM depends on the particular application.

Protect Register Enable (PREN)

The protect register enable (PREN) instruction enables the execution of the PRCLEAR, PRWRITE, and the PRDS instructions. It must be executed immediately before each of these instructions. Both the PRE and PE pins must be held HIGH with the PREN instruction is being loaded.

Protect Register Read (PRREAD):

The protect register read instruction causes the address stored in the Protect Register to be output on the DO pin. Similarly to the Read instruction, a dummy bit (logical "0") precedes the actual output string. While the PRREAD instruction is being loaded, the PRE pin must be held HIGH.

Protect Register Clear (PRCLEAR)

The protect register clear (PRCLEAR) instruction clears the address stored in the Protect Register, making the entire memory array accessible to the WRITE and WRALL instructions. If the Protect Register Disable (PRDS) instruction has been executed, the PRCLEAR will not operate. A PREN instruction must be executed immediately before the PRCLEAR instruction. Also, the PRE and PE pins must be held HIGH while the PRCLEAR instruction is being loaded.

Protect Register Write (PRWRITE)

The protect register write instruction loads the Protect Register with the address of the lowest register to be protected. Only registers with addresses **less** than the address in the Protect Register can be written by the WRITE instruction. While the PRWRITE instruction is being loaded, the PRE and PE pins must be held HIGH.

Protect Register Disable (PRDS)

The protect register disable (PRDS) instruction is effective only ONCE per XL93CS46 device. After this instruction has been executed, the Protect Register can not be modified. All registers with addresses greater than or equal to the address in the Protect Register are permanently protected from the Write and WRALL operations. A PREN instruction must be executed immediately before the PRDS instruction. Also, the PRE and PE pins must be held HIGH while the PRDS instruction is being loaded.

The protect register is valuable when an application requires a mix of E²PROM and ROM in the same device. The XL93CS46 can be made immune to inadvertent write hazards without even using the protect register. The entire device may be rendered write disabled by grounding the PE pin. Another way the XL93CS46 can be made less susceptible to inadvertent write cycle problems is by writing the system software to make use of the Write Enable (WEN) and Write Disable (WDS) instructions. However, E²PROMs are inherently susceptible to write commands during system failure. Use of the protect register under system control provides substantial supplemental protection.

USING THE XL93CS46

The XL93CS46 is easily integrated into a wide variety of applications. It can be used in applications that store configuration information, such as feature telephones, station presets on radios, and PC boards with configuration DIP switches and jumpers. It can be used to store control variables in adaptive, closed-loop systems, such as environment or motor controllers. The XL93CS46 can also be used for data logging.

In a microcontroller system, program code or data could be off-loaded from the internal ROM of the microcontroller into a ROM section in the XL93CS46. This is useful because if ROM code or data needed alteration, it would be much easier and cheaper to reprogram the XL93CS46 than to replace the entire microcontroller with the internal ROM. An E²PROM section could be allocated for any writable data, such as configuration and calibration values. ROM is desirable in this application because any spurious or unauthorized writes that could corrupt the program will be prevented. In the system manufacturing operation, the ROM data and the protect register value would be programmed into the device and the protect register enabled before PC board insertion. The PRE pin would be tied low on the board to prevent write access to the protect register. This configuration is shown in Figure 3.

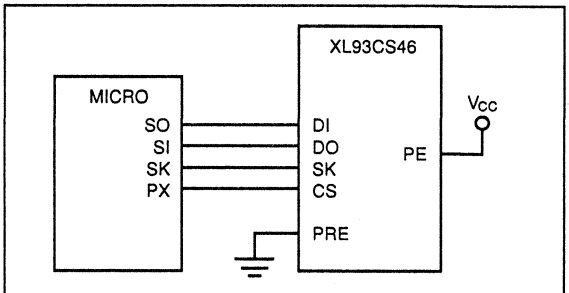
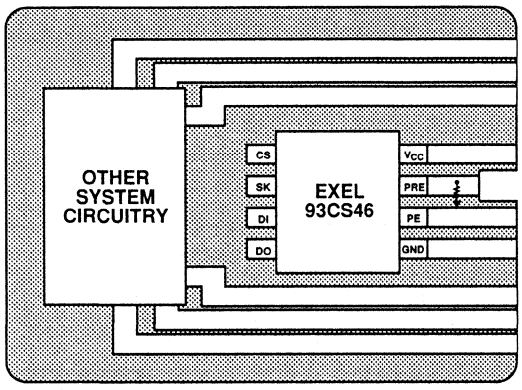


FIGURE 3. PROTECT REGISTER DISABLED

Another application for the XL93CS46 is in systems that support automated production. The XL93CS46 could be programmed on-board as it progressed through each step of the production process with production information such as date codes, status, board identification (serial number),

and fixed configuration information. The PRE pin could be pulled LOW with an on-board resistor to allow production test equipment to drive it HIGH to write data into the device and set the protect register, but prevent any writes to the protected locations during normal operation. This configuration is shown in Figure 4. When in production, the PRE pin could be driven HIGH. When in normal operation, the PRE pin would be pulled LOW through the pull down resistor.



Typical Configuration
PRE pin is accessable during board test but is held LOW while in end system ensuring protection against data alteration.

FIGURE 4. PROGRAM ENABLE PULLED LOW TO PREVENT WRITES DURING NORMAL OPERATION

A third application for the XL93CS46 is in data logging applications. The protect register can be programmed as the data is gathered to reduce the likelihood of modification. Data must be written from HIGH addresses to LOW addresses and the protect register decremented after each write instruction to protect the data just written. In order for the protect register to be accessed by system software, the PRE pin must be attached to an interface, usually a port pin. This configuration is shown below in Figure 5 . The protect register disable (PRDS) instruction must be used upon completion of logging to fully protect the data. PRDS will eliminate subsequent protect register modifications since this is a one time only, permanent setting.

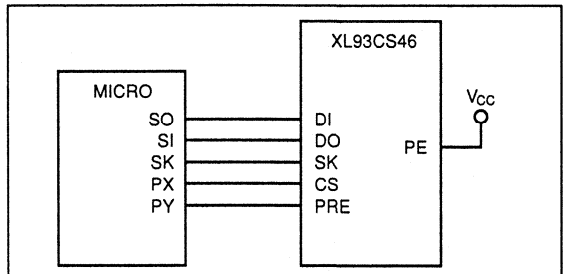


FIGURE 5. PROTECT REGISTER ENABLE

SUMMARY

The XL93CS46 provides a flexible option to many applications. It offers both the security of ROM and the alterability of E²PROM. It is available in both 5 volt and 3 to 5 volt operating devices. The XL93CS46 is an ideal solution for systems which require the flexibility of E²PROM and ROM, low cost, low power consumption, and a software-only interface.

THE CMOS ADVANTAGE

By: John Nagamine, Applications Engineer, August 1990

INTRODUCTION

Exel's CMOS E²PROMs offer many features desired for present day memory applications. They are nonvolatile yet easily alterable memory. Data is preserved for over 10 years whether or not the chip is supplied power. Exel's E²PROMs offer many features, such as 5V only operation, 3 to 5 volt operation, automatic erase before write, inadvertent write protection, and $\overline{\text{DATA}}$ Polling. This application note discusses the advantages of using Exel's CMOS technology rather than NMOS devices and upgrading an NMOS system to CMOS components.

CMOS ADVANTAGE OVER NMOS E²PROMs

CMOS is quickly becoming the dominant technology, displacing NMOS and TTL. CMOS offers a number of advantages over NMOS. First is power savings. NMOS E²PROMs consume a considerable amount of power when compared to CMOS devices. The low power consumption of CMOS helps to keep system temperatures lower, increasing long term reliability and reducing the need for extensive cooling systems. Also, the lower power dissipation which CMOS provides allows for higher packing density, saving valuable space on your system boards.

CMOS is also compatible with TTL inputs and outputs. The CMOS input stage consumes no active power when the input voltage is at ground or at the positive supply level (V_{CC}). The outputs of CMOS E²PROMs drive to the full limits of the power supply and offer a better noise margin than NMOS devices.

UPGRADING FROM NMOS TO CMOS

Generally it is quite easy to upgrade an NMOS memory system to CMOS technology. Many CMOS devices are direct replacements for their NMOS counterparts. Neither hardware nor software changes are needed.

In some cases, power switching transistors have been used to power down NMOS E²PROMs while the rest of the system remains active in order to reduce the system power consumption while the NMOS E²PROMs are not being accessed. In these cases, the data lines of the NMOS parts do not load the data bus substantially. However, a CMOS device may sink substantial current through the DATA pins if the DATA bus is higher than the E²PROM's power supply. In order to prevent this, it is recommended that the power switching transistor be removed, which results in a constant supply voltage to the CMOS V_{CC} pin and also a reduction to the component count and the system cost. The CMOS E²PROM must have power supplied to the V_{CC} pin as long as the data bus on the output lines are active. The low power consumption of the continuously powered CMOS device will not adversely affect the system power consumption.

SUMMARY

Replacing NMOS and TTL devices with CMOS devices, can drastically reduce the system power consumption. The large power savings is ideal to meet the strict power requirements of battery powered systems. Exel produces many CMOS devices which are direct replacements for their NMOS counterparts, making the CMOS upgrade very simple.

USING $\overline{\text{DATA}}$ POLLING TO OPTIMIZE WRITE CYCLE TIMES IN AN INTERRUPT DRIVEN SYSTEM

By: John Nagamine, Applications Engineer, August 1990

INTRODUCTION

The use of interrupt driven system designs have become increasingly popular in many applications because these systems usually have higher performance ratings and offer improved user friendliness. In interrupt driven environments, the system can perform a variety of tasks while waiting for a certain condition to occur. Writing to an E²PROM is an ideal example of the usefulness of an interrupt environment. Since E²PROMs take a relatively long period (2-10ms) to complete their internal nonvolatile Write Cycles, the system is free to perform other tasks while waiting for the memory. This application note discusses a method of using $\overline{\text{DATA}}$ Polling to optimize the Write Cycle times in interrupt driven systems.

FUNCTIONAL DESCRIPTION OF $\overline{\text{DATA}}$ POLLING

$\overline{\text{DATA}}$ Polling is a software method of detecting the end of a nonvolatile Write Cycle. This detection is essential because the typical write times for the E²PROMs are substantially shorter than their specified maximums; typically 3ms shorter. Note that the Write Cycles for E²PROMs are in milliseconds, not in the hundred nanosecond timeframes at which processors typically execute instructions. Thus, a microprocessor can execute many alternate operations in a 3ms interval. It is clear that if typical Write Cycle times were equal to the specified maximum Write Cycle times (Write Cycle always taking the maximum specified time to write), one would only have to time a fixed interval for each Write Cycle, either by a software loop or a hardware timer. The timer would generate an interrupt after the fixed time interval; then the next memory access could be initiated.

$\overline{\text{DATA}}$ Polling is accomplished by allowing the system to monitor the device status via system busses using a simple read and compare operation (see Figure 1). $\overline{\text{DATA}}$ Polling does not require any external hardware. During the nonvolatile Write Cycle, the most significant bit of the last byte written to the device is inverted and routed to the output buffer. The I/O pins remain in a high impedance state unless a read command is issued to the device. In this event, an inverted most significant bit will be available at I/O_7 ($I/O_6..I/O_0$ are indeterminate). Consequently, a comparison of bit 7 of the data read from the device with bit 7 of the last byte written will indicate unequal values. The data thus compared will not match until the chip has completed its nonvolatile Write Cycle, at which point the $\overline{\text{DATA}}$ Polling circuitry is disabled.

Non-Interrupt Environments

In applications where the processor is not directly controlling the Write Cycle, the software can perform compare loops on the MSB until the Write Cycle is complete. In applications which are more processing time efficient, a test program can be placed in the main program loop (outermost loop) to check the status of a previous Write Cycle on each pass through the main or outermost software loop. $\overline{\text{DATA}}$ Polling in these environments is simple, straightforward and requires no additional hardware.

Interrupt Driven Environments

In an interrupt environment, a main control loop may not exist to loop and poll data. Also, the software may require greater time efficiency than the looping solution offered. Ideally, the E²PROM could signal the system when the Write Cycle was completed. Although not obvious at first, $\overline{\text{DATA}}$ Polling can be used in interrupt environments to indicate the completion of a Write cycle.

In order to use $\overline{\text{DATA}}$ Polling in an interrupt driven environment, a time-based interrupt generator is needed. This could be a programmable timer or something as simple as an AC frequency interrupt. The timer output drives one of the processor's interrupt lines. Many systems already have such hardware on the bus and require no addition of counters nor timers to implement this solution. The timer is loaded and started when the Write instruction is issued. The processor does not check to see if the device has completed the Write Cycle until the timer issues an interrupt to the system. The interrupt service routine simply uses $\overline{\text{DATA}}$ Polling to determine if the Write Cycle is complete. In other words, the interrupt routine compares the data last written to the E²PROM to the data being read from the E²PROM. If the two match, the Write Cycle is complete and the device can be written to again. If not, the interrupt routine simply re-loads and starts the timer, and returns to the main program to continue processing until the next interrupt is generated. The interrupt routine may load the timer with a shorter time interval than that loaded when the write instruction was first issued. This allows the system to check for write completion at a more frequent interval. The ratio of the two times, the initial time loaded into the timer and the time the interrupt routine loads into the timer, depends on the application and the speed of the E²PROM. Typically, the initial time loaded into the timer is 4ms which

allows most of the Write Cycle time to pass before Polling the device. A typical time which the interrupt routine loads into the counter is 500µs, a much more frequent Polling time. Again, these times depend on the application and the hardware timer available. Flow Chart 1 illustrates this procedure of $\overline{DATA}$ Polling in an interrupt driven system.

SUMMARY

This implementation is simple and can be performed with little or no additional hardware. By using $\overline{DATA}$ Polling in an interrupt environment, the system has the advantage of using an interrupt driven write algorithm, which optimizes the Write Cycle times, while maintaining a software interface to the E²PROM.

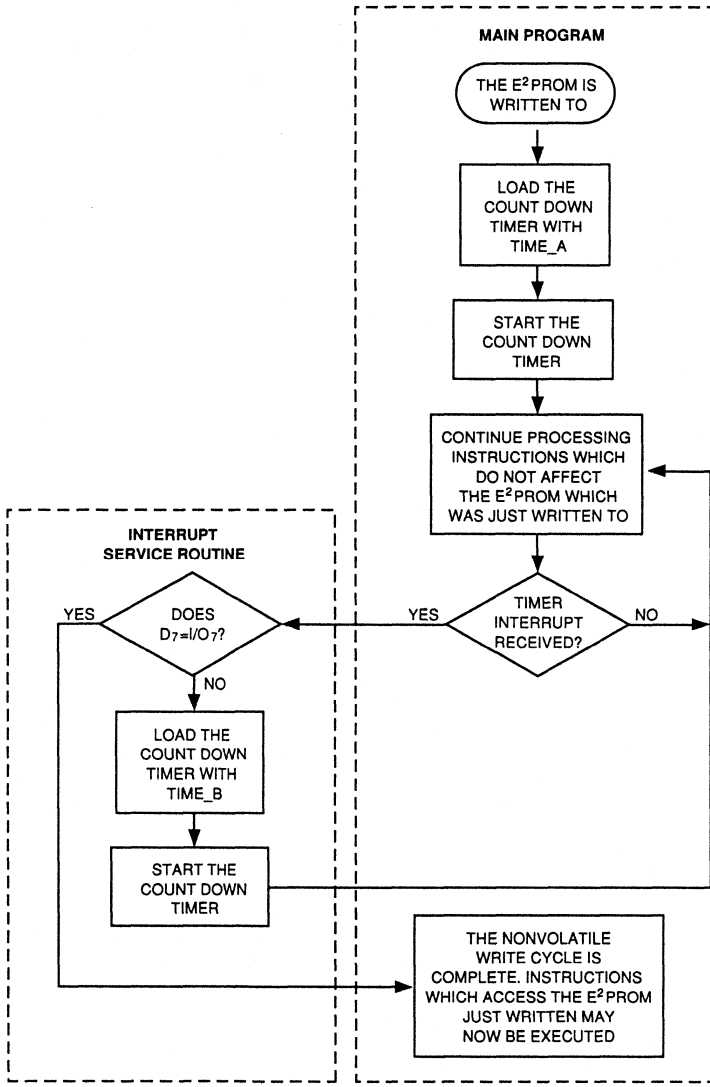


FIGURE 1. USING $\overline{DATA}$ POLLING IN AN INTERRUPT DRIVEN ENVIRONMENT

XL93C46/XL93C56 MICROCONTROLLER COMMUNICATION

By: John Nagamine, Applications Engineer, September 1990

INTRODUCTION

The XL93CXX is a family of serial access E²PROMs intended for use with today's standard microcontrollers and microcomputers. This application note discusses two special considerations which must be addressed when interfacing the XL93CXX family to microcontrollers with built in shift registers.

The first concern occurs if the microcontroller's shift registers are only 8 bits. The 8 bit shift register is not large enough to incorporate the 9 to 11 bit instructions required to control Exel's serial products.

The second concern occurs if the clock line on the microcontroller is initially a logic "1." This presents a timing hazard since the E²PROMs require the last clock during any operation to have a falling edge before the E²PROM is deselected.

FUNCTIONAL DESCRIPTION

The XL93CXX are nonvolatile, yet easily alterable, 16-bit serial E²PROMs. Software instructions control the operation of the devices. The data out pin (DO) indicates the status of the device during the self-timed nonvolatile programming cycle. The Write Cycle includes an automatic erase-before-write feature which eliminates the need for additional firmware overhead. To protect against inadvertent writes, the WRITE instruction is accepted only while the chip is in the write enabled state. To attain the Write Enabled state, a separate Write Enable instruction must be issued. Data is written in 16 bit units with each write instruction. If Chip Select (CS) is brought HIGH after initiation of the Write Cycle, the Data Output (DO) pin will indicate the READY/$\overline{\text{BUSY}}$ status of the chip. This initiates the nonvolatile Write Cycle of the E²PROM.

INTERNAL 8-BIT SHIFT REGISTERS

First, the instruction sequence controlling Exel's serial products range from 9 to 11 bits. In many microcontrollers, the built-in shift registers will send and receive data 8 bits at a time. These 8-bits are not sufficient to produce a complete instruction to the E²PROM. However, the internal shift registers can be used to communicate with the E²PROM by loading and shifting the internal registers more than once. All of the most significant extra bits (required to make a multiple of 8) are shifted into memory as zeros, before the start bit is sent. (All leading zeros shifted into the E²PROM will be ignored.) This process allows 8 bit shift registers to communicate with the serial E²PROMs.

MICROPROCESSORS WITH A NORMALLY HIGH CLOCK

Second, the clock line on some microcontrollers is initially a logic "1." In these cases, the clock consists of a falling edge and then a rising edge. The concern is that the E²PROM requires the last clock during any operation to have a falling edge before the E²PROM is deselected. One solution here would be simply to add one additional clock pulse to the SK pin before deselecting the device. Another solution (for those processors which must send 8 clock increments) is to send one byte of zeros before deselecting the device. Additional zeros clocked into the E²PROM after the instruction, address and data are ignored.

SUMMARY

Exel's family of serial E²PROMs are very easy to use with today's microcontrollers. Serial E²PROMs offer space saving 8-pin packages, low power consumption, and nonvolatile, yet easily alterable memories. Using the internal shift registers of the microcontrollers further simplifies the use of Exel's E²PROMs. Communication between the microcontroller and the E²PROM becomes a simple load and shift operation.

FIELD ALTERABLE SOFTWARE THROUGH E²PROM

By: John Nagamine, Applications Engineer, September 1990

INTRODUCTION

This application note discusses the advantages of utilizing E²PROMs in system design. In-field re-programmability offers the software designer a flexible environment. By programming high level routines in E²PROMs while lower level, machine code procedures in ROM, a flexible, low cost system may be implemented.

THE HYBRID SYSTEM

E²PROMs have opened many options to the software designer. These devices allow for in-field re-programmability, which greatly reduces cost and time of software changes or upgrades. The E²PROM allows the designer the capability to completely upgrade or change his software from a remote location without replacing system ROMs or EPROMs which is costly and inconvenient. Complete in-field re-programmability requires that the entire program store be implemented with E²PROM. This is a costly approach. An alternative is a "hybrid" system.

A "hybrid" system is a design which utilizes both EPROMs or ROMs and E²PROMs to yield a design which features the best of both approaches: a flexible, partially re-programmable system, while maintaining the low cost of a full ROM implementation.

THE ADVANTAGES OF A PARTIALLY RE-PROGRAMMABLE SYSTEM

Most software applications are written in a "Top-Down" programming. This structure is composed of high level software routines calling lower level subroutines which perform individual, simple tasks. The high level software routines become very simple. They may be composed of nothing more than a few subroutine calls. As more and more of the processing tasks are pushed "down" into low level routines, the main procedure in the high level segment becomes short and simple.

It is in these structured programs that the utilization of E²PROMs provides huge advantages. Since the outermost program, the highest level program, is quite compact, it can be implemented in E²PROM while the majority of the machine code in the lower levels can be implemented in ROM or EPROM. Changes to software then become as simple as changing the jump location in the E²PROM or the order of subroutine calls.

A reprogrammable system also leaves the designer the option to use a section of the E²PROM for low level "patch" alterations to the software. If the low level software needs updating, the new version of the machine code can be loaded into the patch area of the E²PROM. The jump or subroutine call is simply changed to call the new version now residing in the E²PROM. Figure 1 shows a typical memory map of the system described above. Figure 2 shows how the "patch" area in the E²PROM is used to replace low level programs which required modification.

The high level program is also modified to point to the new procedure in the "patch" area.

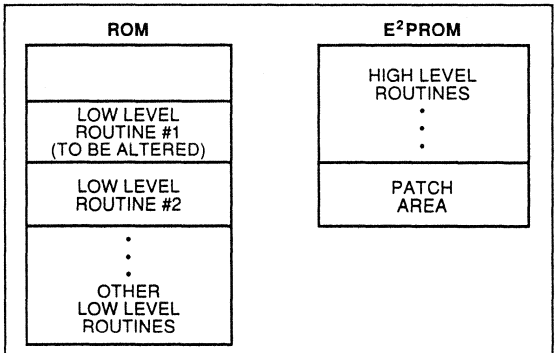


FIGURE 1. MEMORY MAP: ORIGINAL CONFIGURATION

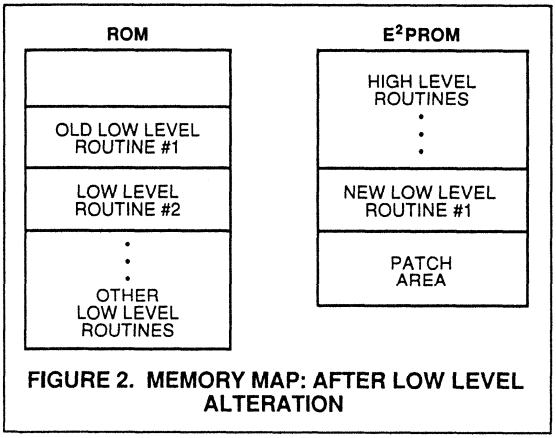


FIGURE 2. MEMORY MAP: AFTER LOW LEVEL ALTERATION

SUMMARY

Ultimate system upgrade flexibility can be attained through a complete E²PROM design; however, this implementation is sometimes less cost effective. However, a minimal amount of E²PROM can add great flexibility to systems. The ability to update system software and the ability to store user alterable parameters, such as configuration data are just a few of these advantages. The ideal ratio of ROM and EPROM to E²PROM depends on the application and the need for re-programmability. The advantage of the "hybrid" approach is that it requires that only the high level portion of the code be stored in E²PROM. Utilizing a combination of both ROMs or EPROMs and E²PROMs can result in a system which exhibits the advantages of in-field alterability.

EXEL SERIAL E²PROMS WITH A SHARED I/O CONFIGURATION

By: John Nagamine, Applications Engineer, September 1990

INTRODUCTION

Exel's large family of serial E²PROMs provides a wide range of low cost, nonvolatile memory feature options. It offers solutions to many applications, offering cost, space and power savings when compared with other solutions. These devices use only four signal lines to communicate with the application environment: Chip Select (CS), Serial Clock (SK), Data Input (DI), and Data Output (DO). To further reduce the required number of signal lines to three, the DI and DO pins can be connected to form a single I/O interface signal path.

This application note discusses solutions to two concerns which may arise when using Exel's serial E²PROMs with the DI and DO pins tied together. These concerns arise when considering two brief intervals which occur during normal operation and present apparent contention hazards as the data in and data out signals are simultaneously asserted. The first situation occurs when the DO pin outputs the dummy "0" bit to indicate the beginning of the output data stream. If A_0 is a logical "1," and the DI driver has not been disabled by the time the "0" dummy bit is output on DO, DI/DO contention is a potential hazard. The second situation occurs when the programming status signal, output on the DO pin, is inadvertently clocked into the device as a start bit, resetting the status signal before it can be read.

DI/DO CONTENTION

When the read instruction is issued to the serial E²PROM sharing a common DI/DO line, both the DI signal and the DO drivers are active, raising a concern regarding reliable system operation.

HAZARD DESCRIPTION

Since the DO pin remains in high impedance while most of the READ instruction is being clocked into the E²PROM, no contention occurs. However, typically 50ns after the rising edge of the serial clock which shifts in the least significant address bit (A_0), DO becomes active asserting the dummy "0" bit to indicate the beginning of the output data stream. If A_0 is a logical "1," and the DI driver has not been disabled by the time the time the "0" dummy bit is output on DO, a low impedance path to ground is created through the DI driver pullup and DO pulldown device. Figures 1A and 1B illustrate the timing and circuitry involved.

This condition poses a threat to T_I, the FET which pulls DO LOW.

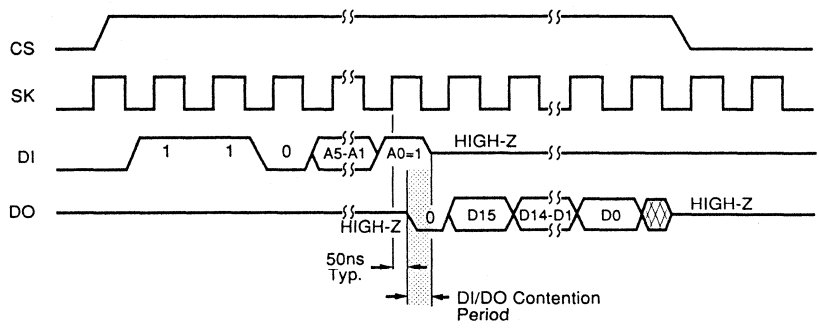


FIGURE 1A. DI/DO CONTENTION TIMING DURING A READ OPERATION

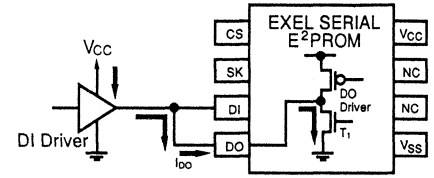


FIGURE 1B. DI = "1"; DO = "0" LOW IMPEDANCE CURRENT PATH

SOLUTION

To minimize potential hazards during this low impedance condition, a current limiting resistor may be placed between the two driving sources, the DI driver and T_1. Two configurations are shown below in Figure 2A and 2B. An alternate solution, shown in Figure 2C, uses an open drain driver with a pullup resistor (R_P).

The clocking rate in any case should be considered to ensure that the resistor selected can charge or discharge the shared DI/DO bus capacitance before the subsequent clock edge.

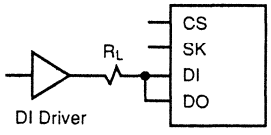


FIGURE 2A.

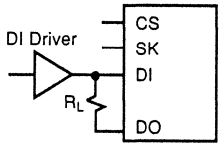


FIGURE 2B.

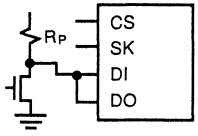


FIGURE 2C.

To Define or Eliminate the Additional Limiting Resistor (R_L)
The purpose of the Limiting Resistor (R_L) is to ensure that the current passing through T_1 does not exceed the transistors' capacity. In most designs the Limiting Resistor can be omitted altogether since T_1 has been designed to accommodate a steady state 5mA without diminished reliability.

To define R_L the driver circuitry of the controller must be considered in conjunction with the T_1 on-channel resistance as shown in Figures 2D & 2E.

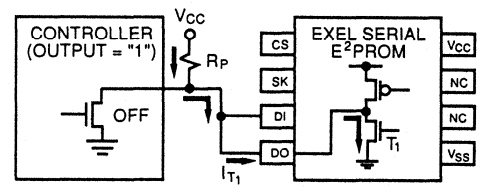


FIGURE 2D. OPEN COLLECTOR DRIVER

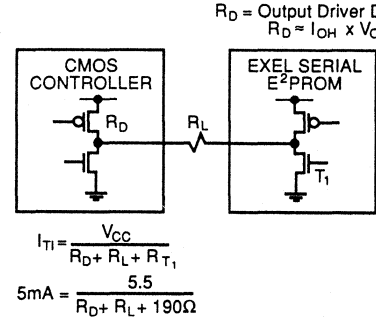


FIGURE 2E. ACTIVE DRIVER

In the case of an open Collector Driver, R_P can serve as both the pullup resistor and that which limits I_{T_1}. For this purpose T_1 may be modeled as a resistor approximated by $I_{OL} \times V_{OL}$ (from the DC parameters).

$$R_{T_1} = \left(\frac{.4}{.0021}\right)$$

$$R_{T_1} = 190\Omega$$

Now $I_{T_1} = V_{CC}/(R_P + R_{T_1})$

R_P min. can be calculated based on a maximum I_{T_1} of 5mA.

$$5mA = \frac{V_{CC}}{R_P + R_{T_1}}$$

Using V_{CC} (Max) of 5.5V

$$R_{P(Min.)} = \frac{5.5V}{5mA} - 190$$

$$R_P \text{ (Min.)} = 910\Omega$$

Obviously, any larger value of R_P will further limit I_{T_1} providing a greater margin of safety.

In the case of a driver without an open collector, the internal on-channel resistance can be approximated using I_{OH} x V_{OH} from the DC Parameter Tables in the datasheet of Describing the Controller. Once this approximation has been made, I_{T1} can be calculated as above. Include a Limiting Resistor (R_L) if the calculated I_{T1} exceeds 5mA.

Note: One final consideration when you have resolved the concern of excess current through T_1 is that of ensuring that the voltage divider provides your intended signal level to DI when the controller is sending data into the E²PROM and DO is active. Please consider the effects of your resultant voltage divider on DI signal levels in the following cases:

- µP outputting "1" to DI and DO = "0"
- µP outputting "0" to DI and DO = "1"

Addressing each of these simple cases in turn will provide you with certainty regarding the reliable performance of your final design.

INADVERTENT STATUS CLEAR

When programming serial E²PROM with the DI and DO pins shared by one line, care should be taken to avoid bus contention.

HAZARD DESCRIPTION

Each member in Exel's serial E²PROM family has a self-timed and internally managed nonvolatile write cycle. The programming status signal indicates whether the nonvolatile write cycle is still in progress (a logical "0" on the DO pin), or has been completed (a logical "1" on the DO pin). This feature allows the user to minimize the programming time by using the status of the DO pin during the course of a programming cycle to determine the actual nonvolatile write cycle completion time.

The programming status signal can be read on the DO pin by bringing CS HIGH after initiating a nonvolatile write cycle. In a four signal system interface, after a programming cycle is complete, the status signal is reset to high impedance by the start bit of the next instruction. Figure 3 illustrates the status signal reset timing of a four signal interface.

In a shared DI/DO configuration, a DO status signal of "1" can be clocked into the device as a start bit and inadvertently reset the status signal before it can be read. This can interfere with the next incoming instruction cycle. The combination of CS HIGH, DI HIGH, and the rising edge of SK, resets the READY/$\overline{\text{BUSY}}$ flag. Therefore, it is important if you want to access the READY/$\overline{\text{BUSY}}$ flag, not to reset it through this combination of control signals.

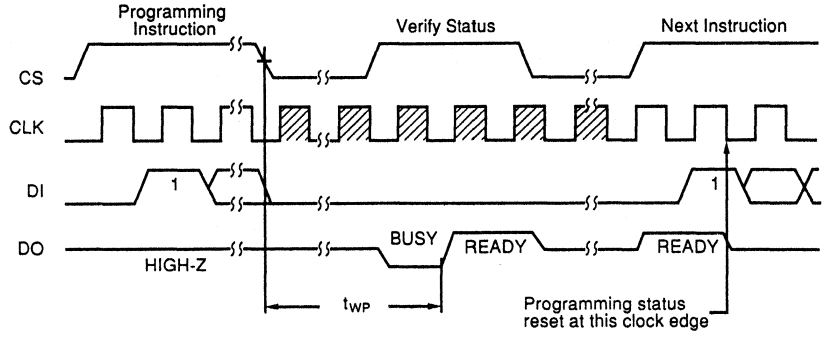


FIGURE 3. PROGRAMMING INSTRUCTION AND STATUS RESET WITH 4-SIGNAL INTERFACE

SOLUTION

In order to avoid the hazard of clearing the status signal, the steps listed bellow are recommended.

1) In order prevent the "1" ready status from resetting the status signal before it can be read, the clock (SK) should be stopped after shifting in the programming instruction.

2) After reading the "1" ready status, a minimum of one SK pulse should be input while the DO signal is HIGH in order to reset the status signal.

3) Finally, to reset the instruction logic, CS should then be brought LOW.

The next instruction can now be executed correctly, without any contention from the DO signal. Figure 4, shown below illustrates the timing diagram for the solution discussed above.

SUMMARY

If precautions are taken to avoid DI/DO excess current and unintentional status clearing, using the DI/DO pins as a single I/O signal effectively minimizes the size of the system interface.

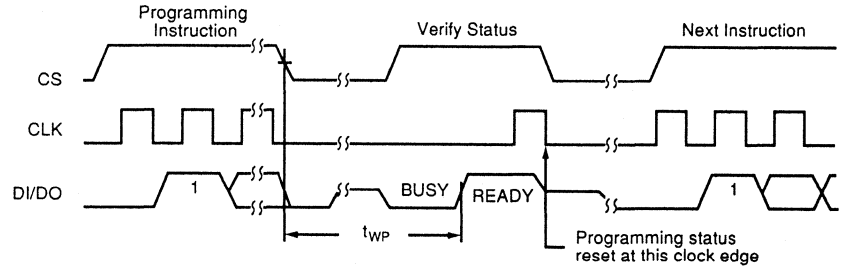


FIGURE 4. PROGRAMMING INSTRUCTION AND STATUS RESET WITH 3-SIGNAL INTERFACE

HOW THE FLOATING GATE E²PROM WORKS

E²PROMs combine many of the most desirable attributes of simpler memory types. E²PROMs are fast, reliable, easy-to-use writable yet **nonvolatile** memory devices. Their effect on existing system design methodology is tremendous. The functions of DIP switches and potentiometers, as well as ROMs, (E)PROMs, NOVRAMs and RAMs are rapidly being consolidated into these extraordinary parts.

E²PROMs achieve their nonvolatility through the use of a floating gate structure similar to that of EPROMs. To change the state of the charge stored on the floating gate, electrons are passed through a silicon dioxide insulator to or from the floating gate by means of a quantum mechanical phenomenon named Fowler-Nordheim tunneling. Basically, when the electric field applied across an insulator exceeds approximately 10^7 volts per centimeter, some number of electrons from the negative electrode will acquire enough energy to pass a short distance through the 'forbidden' band gap of the insulator and enter the conduction band, where they will flow freely toward the positive electrode. The electrons 'tunnel' through the barrier to get to the other side. In E²PROM devices, the negative electrode is the floating gate, the insulator is silicon dioxide, and the positive electrode is the silicon substrate.

Fowler-Nordheim tunneling has been extensively modeled. The models accurately predict how many electrons pass from the negative electrode and move freely toward the positive electrode given an applied voltage and specified time period. Since the threshold field strength required for tunneling is approximately 10 megavolts per centimeter, very thin tunnel oxide regions (approximately 125 angstroms thick) are required to enable operation with reasonable on-chip voltages (on the order of 20 volts). See figure 1.

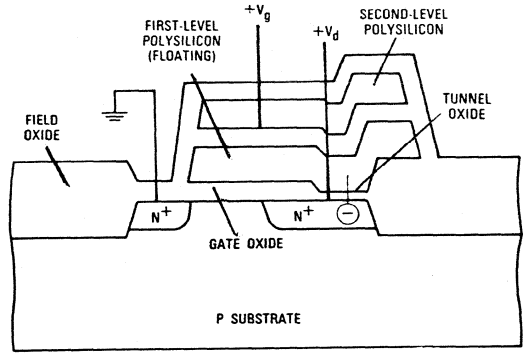


Figure 1. Cross Section of the Basic E²PROM Cell

To tunnel electrons onto the floating gate, the drain voltage (V_D) is brought to zero while raising the gate to V_G. This capacitively couples the floating gate to a positive potential causing electrons to 'tunnel' onto it. The process may be reversed to discharge the gate by applying a positive potential to the drain while grounding the gate.

In either case the specified conditions must be maintained for a time sufficient to cause the required amount of charge to transfer. This time will be influenced by factors such as the thin oxide dimension, the device's threshold voltage, and the shape and amplitude of the high voltage pulse.

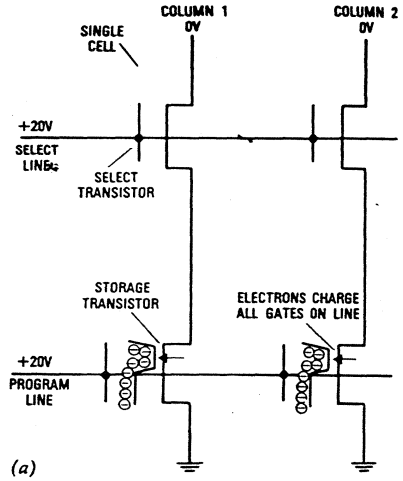


Figure 2a. Cell Operation During Erase

One of the basic E²PROM cells uses a two transistor approach (see figure 2a). The floating gate cell on the bottom acts as the actual storage mechanism. The upper transistor is used to select the cell and to block other rows from discharging when a given column is raised high.

Before a selected byte can be written, it must first be erased. Erasure is no more than a write operation in which all cells are returned to a charged state (or logical one). This is accomplished by raising both the SELECT and PROGRAM lines to approximately 20 volts while the column lines are grounded, as in figure 2a. This condition creates the required electric field to force the electrons through the tunnel oxide to the floating gate where they become trapped.

Once all the floating gates of a byte are charged, the write operation may follow by merely discharging the gates of those bits intended to be logical zero. To accomplish this, the PROGRAM line is grounded and the designated SELECT line is raised to approximately 20 volts. Also, the column lines are raised or lowered to match the incoming data pattern. For example, the bit on the left in figure 2b shows its column line raised, causing the cell to discharge. The bit on the right shows its column line at ground potential. Consequently, that cell's charge undergoes no change.

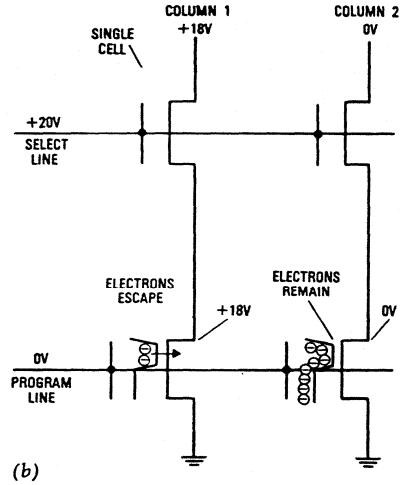


Figure 2b. Cell Operation During Write

The floating gate lies over the conducting region of an N-channel FET. The device is read by applying a positive bias (lower than that required to cause the tunneling phenomenon) to both the SELECT and PROGRAM lines and observing whether the selected FET is conductive. When the floating gate is charged, the FET remains off and is recognized as a logical one. When the gate is discharged, the FET is turned on and represents a logical zero (the charged state may actually represent a logic one or a logic zero at the device output pins, depending on the design of the peripheral circuitry). Since no charge is transferred from the floating gate during this process, the nonvolatile data remains secure through an unlimited number of read operations.

E²PROM ENDURANCE AND DATA RETENTION

Like other memory devices, E²PROMs have characteristics which may affect a customer's application. The most important of these are endurance and data retention.

Endurance refers to the maximum number of erase and write operations through which each cell in the memory array can be cycled reliably. A typical specification limits the number of cycles to 10,000.

Most of today's E²PROMs rely on the Fowler-Nordheim tunneling phenomenon across a thin (tunneling) oxide for their operation. Endurance limitations are characteristically caused by dielectric breakdown in this oxide. This can occur in two ways.

In an ideal E²PROM cell, the electric field across the tunneling oxide should be constant. However, because of imperfections inherent in the manufacturing process, the thickness of the oxide may not be constant, with some cells having greater variations than the average. Thinner areas, then, are subject to a higher electric-field strength and therefore greater tunneling current during erase/write cycles. As more cycles are performed, the probability increases that a pinhole or other imperfection in the tunneling oxide will break down. Eventually a cell will fail to program correctly because of a shorted tunnel oxide layer. Endurance failures of this type usually occur early in the life of the device and are normally weeded out by the erase/write cycling performed by the manufacturer during device testing.

The major cause of endurance limitations, however, is dielectric breakdown related to the trapping of a minute number of electrons in the tunnel dielectric during each erase/write operation. An ideal feature of a tunneling dielectric is that it should never remember the number of electrons that passed through it or the voltage that was previously applied across the film. Unfortunately, for the thermally grown silicon dioxide used as the insulator in E²PROMs, there always exist a number of electron and hole traps. When the cell is erased or written, electrons are injected through the thin oxide and some of them will be captured by these traps, causing a build-up of negative charges in the oxide. This effect, which is cumulative, reduces the electric field at the injection interface, thus decreasing the tunneling current and causing the gradual reduction of the threshold margins required to differentiate logic ones and zeros (see figure 1). More importantly, the trapped electrons cause an increase in the electric field across the oxide which eventually results in a partial breakdown of the oxide and leakage of the charge stored on the floating gate. This failure, which manifests itself as a data retention failure, usually occurs before the threshold margin has been reduced to a point below the minimum acceptable margin.

It should be noted that endurance, like speed, varies from device to device and from lot to lot. The problem, then, is to non-destructively test the devices to select those with the desired endurance characterisitics. Unfortunately, this can only be done by actually programming the device many times, measuring the degra-

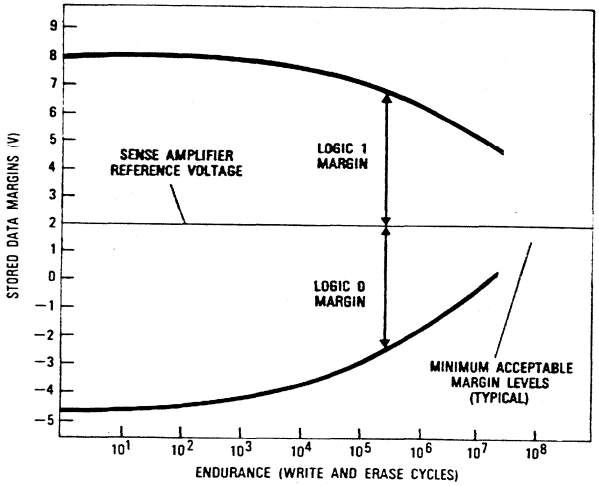


Figure 1. Cell Margin Characterisitics

dation in the cell's threshold margin, and then predicting the likely endurance. Some devices, of course, will not pass the screen for, say, 10,000 cycles but can be predicted to be usable for less than that number. Also, the screening test is much simpler if it is only necessary to predict that the device will program a limited number of times, say 100. Thus, EXEL is able to offer, at a lower cost, 'low endurance' versions of some products for those applications which do not require extended endurance characteristics.

Since an endurance failure is a failure of a bit and not a catastrophic device failure, some manufacturers utilize a dual-cell per bit architecture to produce devices specified for high endurance applications (the probability of both cells failing simultaneously being small). This, however, is not a cost-effective technique since the chip size is greatly increased. EXEL's approach is to extend endurance via process technology improvements. We expect to make higher endurance specifications standard in the future. Even today, of course, EXEL's products exhibit outstanding endurance characterisitics.

Data retention is the ability of the E²PROM cell to retain its charge over extended periods of time in the absence of applied gate bias. Failures are caused primarily by impurities in the structure of the storage device, which cause undesired leakage paths.

It may be thought that data retention can be increased by programming with higher voltages or for longer periods of time. Actually, plots of cell margin versus time approach each other asymptotically, regardless of the initial margin (see figure 2). Thus, the cell should not be overprogrammed, since this may actually be detrimental to the endurance characteristics.

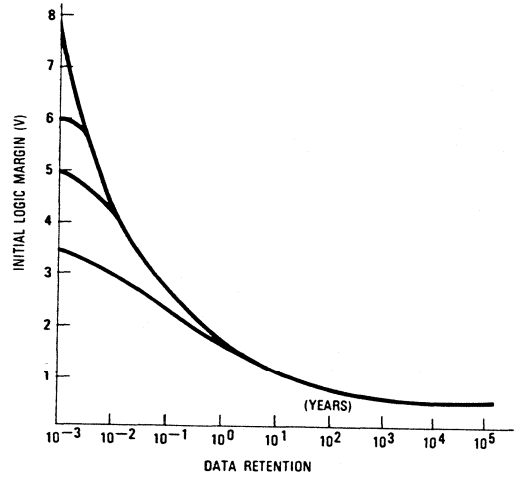


Figure 2. Data Retention Characteristics

Data retention characteristics can be predicted by measuring cell margin after baking at a high temperature. All EXEL devices are specified for a data retention of 10 years minimum from the last write. Some competing non-volatile alternatives, such as CMOS static RAMs with integrated battery backup, specify data retention from time of manufacture, not from time of the last write.

MINIMIZING WRITE TIMES ON THE XL2816A

By Reggie Huff, EXEL Marketing

The 2816A has become a remarkably popular memory type as the industry's first full-featured 5-Volt-only electrically erasable PROM. It incorporates a winning feature set which includes latches for data and address as well as an automatic and fully self-timed nonvolatile erase/write cycle. These features result in an easy-to-use, alterable, yet nonvolatile memory device.

PURPOSE

The purpose of this Application Note is to describe a method of utilizing the typical nonvolatile write times of the XL2816A. By enabling the system to sense when the nonvolatile write cycle is actually complete, instead of waiting for the maximum specified nonvolatile write period (10 ms) to expire, the system can achieve an average write time reduction of 40%.

SIMPLE TECHNIQUE

The XL2816A is a fully self timed device which internally monitors and governs the sequence required to perform the nonvolatile erase/write cycle (see state diagram in figure 1). Once the XL2816A has recognized a valid write command and initiated its internal write cycle, it places its data bus output buffers in a high impedance state. If the system is fitted with pullup resistors on the data bus, then any attempted data access (read) during the nonvolatile write cycle will result in FF_{16} data acquisition due to the effect of the pullup resistors (see figure 2).

Upon completion of the nonvolatile write cycle, the XL2816A releases control of its output buffers back to the control pins (OE, CE, WE). Thus, any read once the nonvolatile write cycle is complete will result in a valid data acquisition.

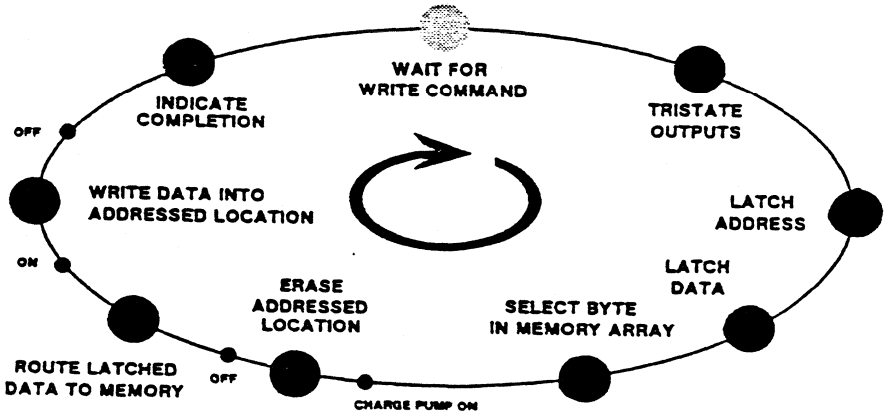


Figure 1. Nonvolatile Write Cycle State Diagram

Consequently, a software loop wherein a specific non-FF_{16} location is accessed and tested for data verification may be used to determine the actual nonvolatile write cycle completion.

A sample 'quick-write' subroutine flow chart is illustrated in figure 3. This utilizes the XL2816A's high impedance output buffer to determine ready or busy status. After initiating the byte write cycle, at least 5ms will expire before the nonvolatile write cycle will be complete. Since the control, data and address busses are freed by the XL2816A during the nonvolatile write period, the system might use this time to perform other tasks. This is indicated by the 'optional user code' box in the flow chart. The test loop merely reads a test location in the memory and compares the acquired data with FF_{16}. If the data matches FF_{16}, the XL2816A's output buffers are still disabled, indicating that the nonvolatile write cycle is still in progress, and the flow loops back for another test. When the data acquired is the known contents of the test location, the flow exits from the subroutine. The XL2816A may now be accessed for read data or started upon a new write cycle.

Note that the test location may be any byte in the E²PROM whose contents are a value other than FF_{16}. If the contents of the test location are 00_{16}, a simple 'jump-if-non-zero' instruction may be used for the loop. Also, in this case, only a single pull-up resistor on any line of the data bus would be required to assure a non-zero value when the XL2816A's output buffers are open.

CONCLUSION

Systems requiring maximum E²PROM write speeds can utilize the cost effective and readily available XL2816A without waiting 10ms for each byte write. The natural features of this popular device may be easily exploited to provide the information which more expensive devices offer via their READY/BUSY and DATA polling features. The XL2816A, when fully utilized, is one of the most advanced, versatile and cost effective memory solutions available today.

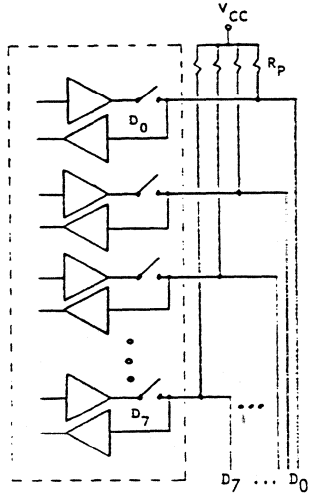


Figure 2. Model of XL2816A Output Buffer During Non-volatile Write

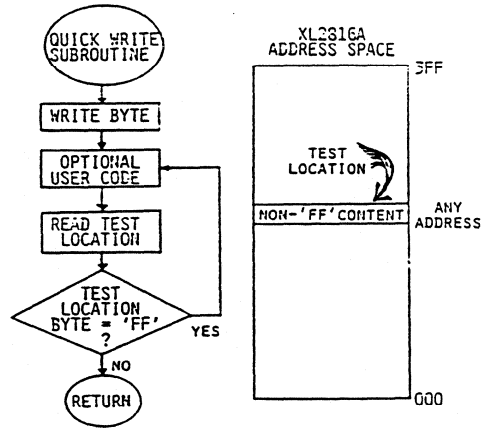


Figure 3. Flow Chart for Quick Write Subroutine

USING THE XL2816A IN THE UNIVERSAL 28-PIN SITE

by Reggie Huff, Exel Marketing

The XL2816A is the most widely available and inexpensive full featured E²PROM in production today. Its pinout configuration, however, does not allow for future expansion to the higher density E²PROMs such as the XL2864A, the XL2865A or future 256K devices. This incompatibility is easily resolved by designing the board with a universal JEDEC-standard 28-pin socket and two jumpers to allow the option of the XL2816A or any of the aforementioned higher density memories.

Purpose

The purpose of this Application Note is to describe the method of designing a 28-pin socket which will accommodate the 24-pin XL2816A as well as higher density memories such as the XL2864A and XL2865A.

Method

Figure 1 shows the compatibility of the pin assignments of the XL2816A with the JEDEC-standard 28-pin socket. Note that when the XL2816A is lower justified in the 28-pin socket, only two pins require reassignment. This can be accomplished via the jumpers shown in the figure. When the jumpers are in the 'a' position, the V_{CC} and WE inputs are routed to the proper pins for operation of the XL2816A. When the jumpers are set, instead, in the 'b' position, the higher order address signals A_{11} and A_{13} are appropriately routed to their corresponding input pins for the 28-pin memory devices.

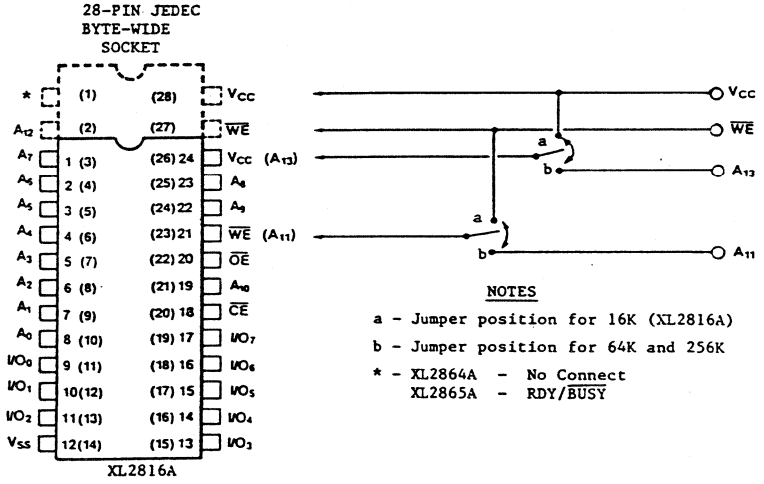


Figure 1. Universal 28-Pin Site and Required Jumpers

If only 16K and 64K compatibility is required, then A_{13} will never be needed. Since pin (26) has a NC assignment on the EXEL 64K E^2PROMs, V_{CC} may be permanently routed to both pins (26) and (28), thus eliminating the requirement for the upper jumper.

Pin (1) on the 28-pin socket, though irrelevant when the XL2816A is used, serves different functions on the higher density memories. It may be left disconnected if the alternate memory for the socket will be the **XL2864A** since its pin (1) has a NC assignment. If the **XL2865A** is to be used in alternate applications, pin (1) becomes an open collector output offering Ready/Busy information.

Addressing the different density E^2PROMs is a separate matter and figure 2 illustrates the use of an inexpensive 32x8 PROM to generate the appropriate decoding. Table 1 shows a simple example of coding of this PROM to accomodate a total of 16K bytes of non-volatile memory implemented as either eight XL2816As or two XL2864As (or XL2865As). With the PROM's A_3 input jumper connected in position 'a', the sockets are ready to accept XL2816As and one of the eight 16K devices is selected as a function of the PROM inputs A_2 through A_0 (address inputs A_{13} through A_{11}). When desired, the jumper can be moved to position 'b' and the eight 16K devices can be replaced by two 64K devices. This PROM decoding technique offers maximum versatility since the PROM code can be defined to allow any combination of 16K and 64K E^2PROMs as well as any other memories (ROMs, EPROMs or RAMs) on the board. Also, this address decoding scheme may, of course, be extended to accommodate more sockets and higher density devices through variations in the PROM code.

It is clear that through simple board layout planning, the EXEL E^2PROM memory solution can be implemented to take advantage of both today's most cost effective memories and tomorrow's advanced technology. Contact EXEL's Technical Marketing Department if you require technical support in planning your E^2PROM memory designs.

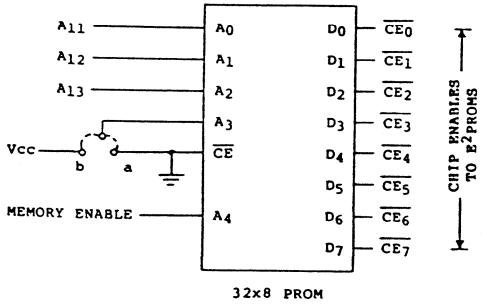


Figure 2. PROM CE Decoder

PROM INPUTS					PROM OUTPUTS								
A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	0	1	1	1	1	1	1	1	0	--
0	0	0	0	1	1	1	1	1	1	1	0	1	
0	0	0	1	0	1	1	1	1	1	0	1	1	JUMPER IN POSITION A
0	0	0	1	1	1	1	1	1	0	1	1	1	
0	0	1	0	0	1	1	1	0	1	1	1	1	
0	0	1	0	1	1	1	0	1	1	1	1	1	
0	0	1	1	0	1	0	1	1	1	1	1	1	
0	0	1	1	1	0	1	1	1	1	1	1	1	
0	1	0	0	0	1	1	1	1	1	1	1	0	--
0	1	0	0	1	1	1	1	1	1	1	1	0	
0	1	0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	1	0	
0	1	1	0	0	1	1	1	1	1	1	0	1	
0	1	1	0	1	1	1	1	1	1	1	0	1	
0	1	1	1	0	1	1	1	1	1	1	0	1	
0	1	1	1	1	1	1	1	1	1	1	0	1	JUMPER IN POSITION B
1	d	d	d	d	d	d	d	d	d	d	d	d	

NOTE: "d" indicates "don't care"

Table 1. PROM Coding Example

THE E²PROM AS A DIP SWITCH REPLACEMENT

DIP switches have been used to provide small amounts of nonvolatile memory for storage of information such as configuration parameters, calibration constants, identification codes, and other data subject to infrequent data changes. The primary feature which has made these switches attractive to designers is their low initial cost.

E²PROMs, of course, also provide nonvolatile storage. In the past designers have shied away from using E²PROMs to provide the functions of DIP switches due to the high cost of these devices. However, the cost of E²PROMS has dropped dramatically as the result of technology improvements, manufacturing learning curve and competition. **It now becomes economically viable to use E²PROMs as replacements for DIP switches.**

The True Cost of DIP Switches

Although the DIP switch itself has a low initial cost, additional costs are associated with the use of these devices in a microprocessor system. First there is the cost of the decoders, resistors and gates required to interface the switches to the microprocessor. Then there are the 'hidden' costs, including:

* Use of switches limits PC board layout flexibility, since the switches must be accessible for changing.
* Switches are difficult to test at incoming inspection. Thus, bad components may be found only at final test, or even worse, only at the user site.
* Wave soldering can cause contamination of the switch. Special provisions must be made for soldering the switches onto the board.
* Full testing of the assembled board requires that the switches be changed manually. This is a time-consuming operation and as a result the board is often not tested completely.
* The equipment must contain special doors or hatches to allow access to the switches for service.
* A simple change to a DIP switch may require that a serviceperson visit the customer's site.

When all the above are considered, it is evident that the true cost of the DIP switch is much higher than apparent.

Benefits of the E²PROM Solution

Regardless of cost considerations, there are many benefits that accrue when an E²PROM alternative is used. The solid state solution, of course, offers greatly improved reliability. The units are 100% tested by EXEL, and can be further tested quickly and thoroughly to any desired level by the customer. Special board layout considerations and special soldering steps are eliminated. Board testing is simplified and more complete, since the 'switch' settings can be changed easily by automatic test equipment. Special access provisions are not needed since the contents of the E²PROM can be changed from a keyboard or even remotely via a modem. Post-delivery service costs are reduced in the same way.

Foremost, though, is the added value that the E²PROM solution brings to both the OEM and his customer. Since this component represents the equivalent of thousands of switches, more options can be added to enhance the total value of the system. Portions of the memory can be used to store data such as the equipment configuration and the assembly and service histories. Through these, problems in assembly can be traced, the revision status of the equipment can be easily determined, and extra equipment features can be easily enabled, all via a small cost in software, with no extra components.

Implementation of the E²PROM Solution

Interfacing the E²PROM to the microprocessor requires only a single output from an address decoder, such as a 74LS138, regardless of the number of bytes used as 'switches'.

Several methods may be used to interface the DIP switches to the microprocessor system. One of the simplest uses an octal buffer such as a 74LS244 for each switch. A more economical method, figure 1, uses a quad two-input multiplexer such as the 74LS257. 74LS253s or 74LS251s may be used if more than one switch is required. Only a single decoder output is required to support up to eight switches and the mux'es are less expensive than the octal buffers. A resistor must be attached from the buffer side of each switch to Vcc to pull the input up when the switch is open.

The number of resistors required could be reduced to a total of eight for any number of switches if diodes were used for the multiplexing function. However, the drop across the diode raises the logic '0' level seen by the buffer, which may cause problems in noisy environments. Thus, this alternative is not considered.

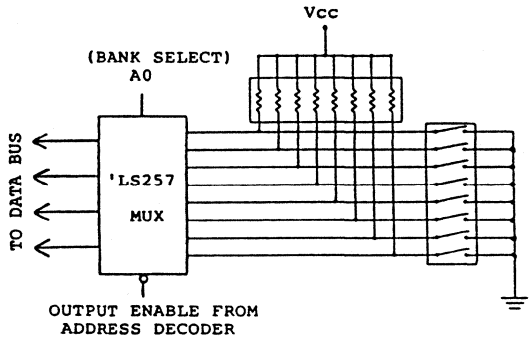


Figure 1. DIP Switch Interface

E²PROMs: Ensuring Data Integrity

by Reggie Huff, Exel Marketing

INTRODUCTION

The 5-Volt only E²PROM brought to the digital design industry a remarkably versatile memory device which, for the first time, merged the in-system alterability characteristics and design ease of static RAMs with the nonvolatile storage characteristics of ROMs and PROMs. This innovation provided a simple and reliable solution to many system designs and subsequently became one of the most desirable memory elements in the industry.

Along with this amazing invention came a subtle system hazard known as "inadvertent" or "false" writes. Inadvertent writes were, at first, often falsely interpreted as a random data change within the memory itself. This intimidated many interested system designers into disregarding E²PROM technology and settling for inferior and often more costly memory solutions. Upon closer inspection, the actual cause was revealed to be valid write commands which were inadvertently issued to the E²PROM during system power transitions, brownouts, and power line "hiccups". Initially, E²PROM manufacturers suggested support circuitry to protect their memories from these system indiscretions. More recent IC designs have moved this protection onto the chip itself, eliminating the problem of inadvertent write hazards and, finally, providing safe and reliable electrically alterable nonvolatile memory devices.

System designs utilizing E²PROMs vary dramatically in both implementation and nature. Consequently, these systems are optimally supported by an equivalent variety of false write protection mechanisms. Some cost-critical designs are best served by inexpensive E²PROM devices (e.g., XL2816A) coupled with simple external protection circuitry. Other design engineers utilize a sound understanding of the false write hazard combined with the thorough on-chip protection mechanisms. Leading edge designs incorporate EXEL's state-of-the-art E²PROMs, with their fully integrated inadvertent write protection, to achieve exceptionally efficient solutions. Whatever your design specifications may be, EXEL offers an E²PROM solution which ***eliminates*** the problem of inadvertent hazards and provides ROM-like data confidence.

This applications note will describe the nature and source of inadvertent data alteration as it applies to E²PROM technology as well as describing the variety of protection mechanisms designed into the memory chips themselves. Also, an assortment of external solutions will be discussed along with the specific applications which they best support.

Inadvertent write hazards can easily be eliminated as a system concern through an understanding of the true nature of the problem combined with some design foresight. *In many existing systems, sporadic false writes may be curtailed by simply replacing competitor's E²PROM devices with the write-protection-enhanced EXEL equivalents.*

THE SOURCE OF INADVERTENT WRITES

The evolutionary tree in Figure 1 shows the progressive development of nonvolatile memory toward easy alterability. Eventually, this lineage merged with the static RAM to provide the best attributes of each memory type in a single device. Today's fully featured E²PROMs offer secure zero-power data retention characteristics combined with an easily interfaced RAM-like writability. This highly flexible memory type, due to its dual nature, is susceptible to the hazard of inadvertent write commands which may be issued to it by the system control bus during the system power transitions.

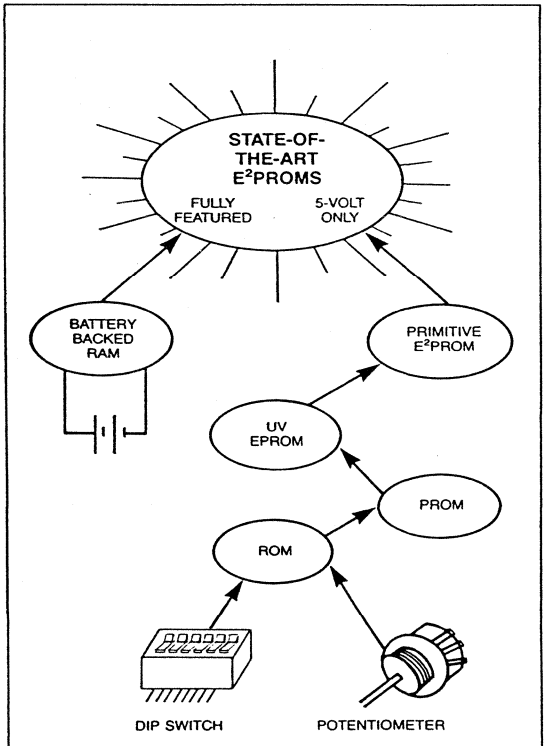


Figure 1. Nonvolatile Memory Evolution Chain

Digital Garbage

Chip designers who have developed logic devices, microprocessors and controllers have never concerned themselves with what their devices spit onto the bus during system power transitions. Formerly, this did not present a problem since nonvolatile memory types were not alterable in system and the volatile memories (RAMs) lost all data after power down and were initialized after the system stabilized following the power-on sequence. Clearly, even if write commands were inadvertently generated during these system power transitions, no critical data alteration would occur.

Indiscrete System Commands

Fully automated (internally latched and timed) E²PROMs can recognize write commands which, although logically valid, are actually the result of noise spikes, glitches and bus contention occurring in the system while the power supply is transitioning. These signals may erroneously initiate nonvolatile write cycles in the E²PROM causing garbage on both the address and data buses to be internally latched. Subsequently this data may be written into the nonvolatile memory array. Once it's clear that the source of inadvertent data changes exists external to the E²PROM, a wide variety of possible protection mechanisms are brought forth as feasible, practical solutions.

ON-CHIP PROTECTION MECHANISMS

As the evolutionary trend to integrate the E²PROM support circuitry onto the memory chip itself has continued, protection features have become a part of the accepted E²PROM norm. EXEL design engineers have developed and integrated a variety of mechanisms which protect the E²PROM data integrity throughout power transitions, brownouts and system noise bursts.

These features include:

- $\overline{WE}$ Noise Filter
- V_{CC} Lockout Circuitry
- Power-up Write Delay
- Software Write Enable Control

Through the informed utilization of these advanced features, the system engineer can quickly eliminate concern about his E²PROM data integrity and return his attention to an exploration of the power and versatility that EXEL E²PROMs offer to the system design.

$\overline{WE}$ Noise Filter

The $\overline{WE}$ noise filter is a very basic protection scheme incorporated in all EXEL NMOS memories, which blocks common "glitches" and short duration noise spikes from initiating a nonvolatile write cycle. This feature is active during both power transitions and during normal operation. Figure 2a shows the range of $\overline{WE}$ pulse widths and their influence on the XL2816A. This filter mechanism is achieved through the use of an internal capacitor (C_{FILTER}) from the $\overline{WE}$ input to (V_{SS}) which must be charged and discharged through the input protection resistance (R_P) and the system $\overline{WE}$ connections. Figure 2b shows a model of the $\overline{WE}$ input filter.

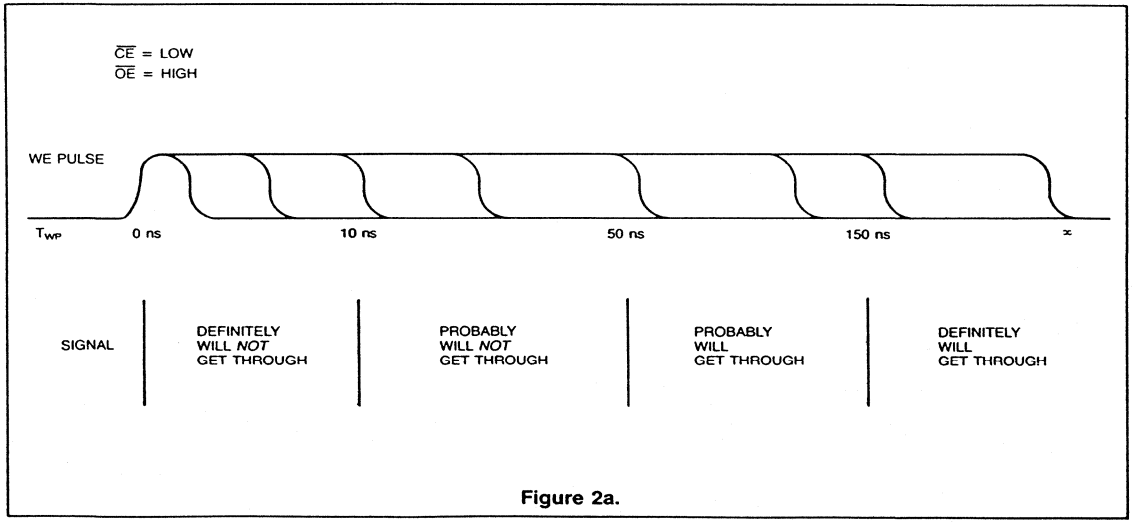


Figure 2a.

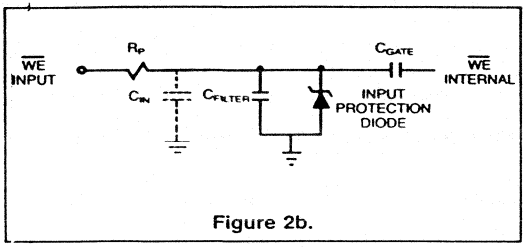


Figure 2b.

Although the data sheet specification requires a minimum $\overline{WE}$ pulse width (t_{WP}), the internal write cycle *can* be initiated with a pulse of shorter duration than that. For example, assuming $\overline{CE}$ and $\overline{OE}$ are at appropriate levels, supplying the XL2816A with a $\overline{WE}$ pulse of ≥150 nanoseconds is guaranteed to initiate a nonvolatile write cycle. A shorter $\overline{WE}$ pulse *may*, however, also initiate a write cycle. This is just not guaranteed. The purpose of the $\overline{WE}$ noise filter is, therefore, to eliminate glitches and noise as a potential source of inadvertent write cycles.

V_{CC} Lockout Mechanism

The V_{CC} Lockout mechanism is the most technologically sophisticated protection mechanism offered on E²PROMs today. It is a fully integrated automatic function. It operates transparently to, and without intervention from, the system and can effectively eliminate power transition related inadvertent write cycles.

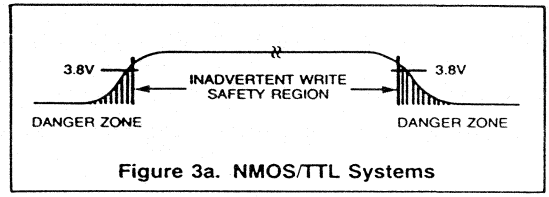


Figure 3a. NMOS/TTL Systems

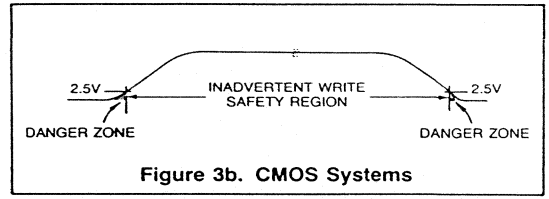


Figure 3b. CMOS Systems

Figure 3. Danger Region Graphs

APP. 4 NOTES

How It Works

The danger region graphs (Figures 3a and 3b) show the system V_{CC} ranges in which the probability of unintended, system generated, E²PROM write commands increases dramatically. The function of the V_{CC} lockout mechanism is to monitor the applied V_{CC} level and inhibit any E²PROM write commands coincident with $V_{CC} \leq V_{WI}$. In other words, this circuit watches the supply voltage and disables the internal write circuitry any time that V_{CC} drops below a specified threshold voltage (V_{WI}). A model of this function is shown in Figure 4.

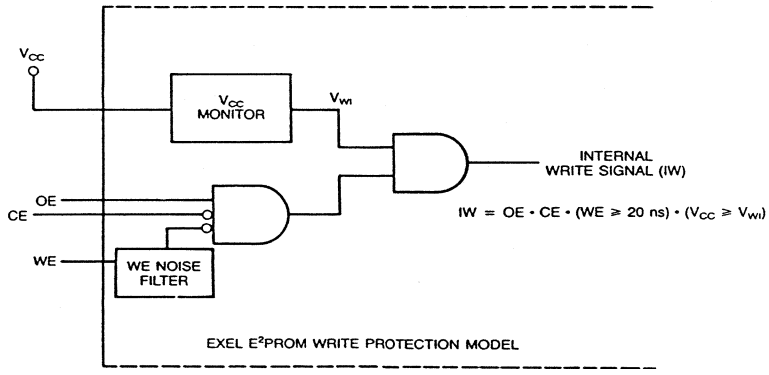


Figure 4. V_{CC} Lockout Circuit Model

The V_{CC} level below which write cycles are inhibited is specified in the *DC Operating Characteristics* section of the device data sheet. This trip point is defined as a voltage range instead of a constant level to account for manufacturing variations and changes in thresholds as the device temperature varies throughout its allowable range. The XL2816A, for example, specifies a range between 3.0 V and 3.5 V within which the V_{WI} trip point will vary. This range normally provides sufficient protection when the system is implemented using CMOS components since these usually offer responsible logic down to V_{CC} = 2.5 V. However, if NMOS or bipolar logic is utilized, then additional precaution is advised since their outputs often become sporadic when V_{CC} is below 3.8 V.

The V_{CC} lockout voltage (V_{WI}) on the XL2864A and XL2865A is specified as a window from 4.0 V to 4.5 V. This range is high enough to block even the indiscriminate signals of NMOS and bipolar systems. Referring again to the danger region graphs (Figures 3a and 3b), it is clear that by blocking write commands when V_{CC} is below 4.0 V, the primary hazards of system generated inadvertent write cycles are eliminated.

Hysteresis

A small hysteresis region is designed about the V_{WI} threshold to eliminate possible oscillations and to simplify the management of brief V_{CC} dips (brownouts). The XL2864A and XL2865A, for example, display the following characteristics:

When V_{CC} is rising from a level below V_{WI}, these devices will wait a maximum of 50 µs before recognizing write commands.

When V_{CC} is falling from a level greater than V_{WI}, these devices will initially assume that a brownout is occurring and so remain fully operational for 50 ns after the V_{WI} threshold is crossed. If the V_{CC} level returns to or above V_{WI} within 50 ns, then the device does not evoke the internal write inhibition features. After 50 ns has passed, if V_{CC} is still less than V_{WI}, then the write lockout feature is activated, write commands are ignored and any nonvolatile write cycle in progress will be aborted.

Limitations of the V_{CC} Lockout

The V_{CC} lockout mechanism eliminates the hazards of inadvertent data alterations in *most* system designs. It is, however, possible to circumvent this protection through unusual system designs. A system requirement when relying on the on-chip V_{CC} sensor is that the same supply voltage powers all of the components which can drive the control bus.

In a system with multiple power supplies (see Figure 5), the possibility exists that the power supply of a device

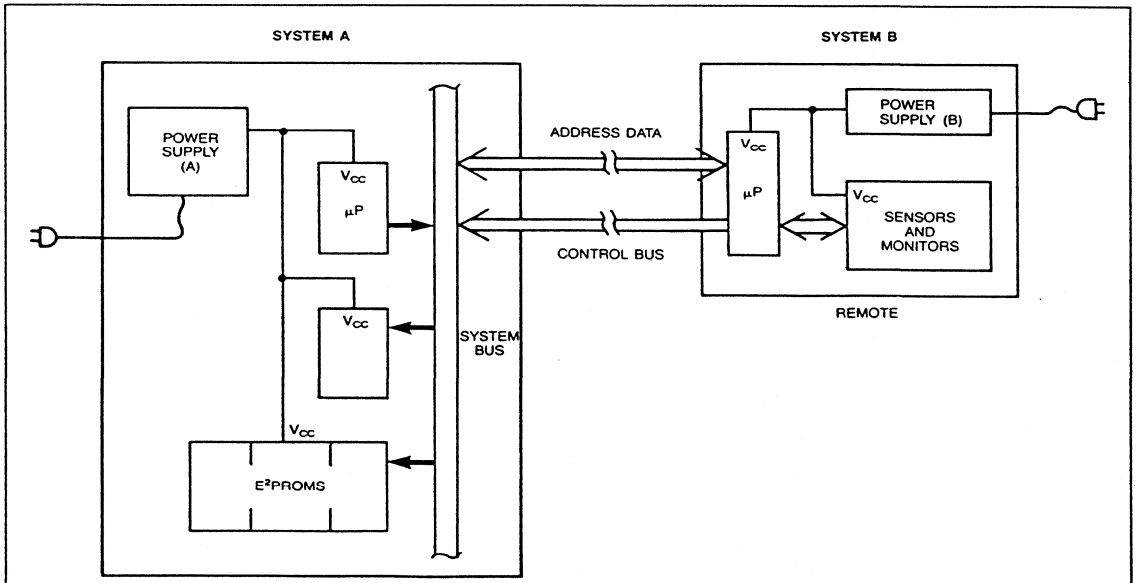


Figure 5. Multiple Power Supplies (Example)

driving the control bus (Power Supply B) could falter without affecting the power supply which operates the E²PROM (Power Supply A). In this case, inadvertent write signals issued on the control bus would not be blocked by the V_{CC} lockout mechanism since the V_{CC} lockout circuit would be monitoring an operational level supply voltage.

A second way to thwart the V_{CC} lockout mechanism is through the use of components whose outputs become unstable or erratic at supply voltages above 4.0 V. If a system is designed, for instance, with components limited to a 5% variation in V_{CC} and if those components are capable of asserting indiscriminate signals on the control bus when V_{CC} is above 4.0 V, then an alternate method of protection is recommended.

XL2816A Power-Up Delay

The XL2816A has one inadvertent write protection mechanism which is unique amongst the E²PROM products. This feature is called the POWER UP DELAY mechanism and effectively blocks any write commands issued to the E²PROM during and immediately after power-up. Its purpose is to allow the system to stabilize the control bus before allowing the memory to respond to write commands. Note that this delay mechanism does not affect E²PROM read commands.

Most inadvertent data alterations occur during the power-up phase of system power transitions. This is primarily due to the fact that any write cycles which are initiated during the power-up phase have plenty of time to complete whereas those initiated as power falls away are often disabled by lack of power before any nonvolatile data alteration actually occurs. While V_{CC} is on the way up between V_{WI} and the voltage at which the system operates reliably, transient signals might combine to assert a valid write command. The power-up delay function on the XL2816A eliminates this hazard by ensuring that 5-20 ms elapse after V_{CC} reaches V_{WI} before nonvolatile write cycles are enabled (see Figure 6). This feature is offered only on the XL2816A since the ensuing E²PROMs incorporate a V_{WI} within the range of 4.0-4.5 V. This higher write inhibit threshold window essentially eliminates the inadvertent write hazard without the need for the additional power-up delay protection.

The power-up delay feature can often eliminate bothersome write hazards by merely replacing another manufacturer's 2816A device in an existing design. When inadvertent data alterations are occurring during the power-up transition, the enhanced XL2816A will often curtail the problem without further board revisions.

Although the power-up delay enhancement, when combined with the other standard XL2816A protection features, will eliminate most system write hazards, it may not constitute a complete and reliable solution in all applications. Take, for example, a system which has such great capacitance on the supply rail that the power down period, as V_{CC} falls from 4.0 V to 3.0 V, is 100 ms. Such a system could perform multiple nonvolatile write cycles in a single power down cycle. To handle this peril the power-down period could be sharply reduced by shorting the V_{CC} rail capacitance to ground upon power loss. Combining the XL2816A's power-up delay feature with a short (<200μs) power down period is a simple way to shut out power transition related inadvertent writes.

Note: In the unlikely event of a power crash during a nonvolatile write cycle, the content of the byte currently being operated upon will be indeterminate.

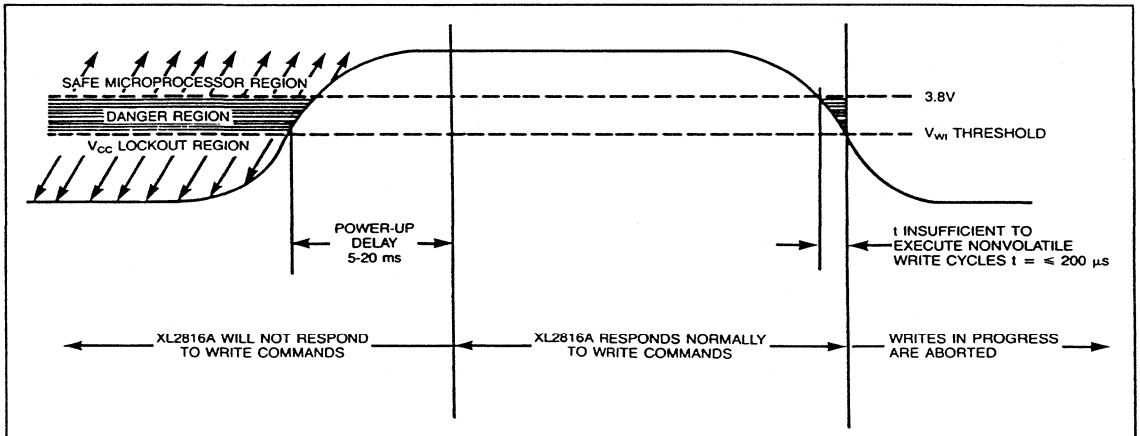


Figure 6. XL2816A Protection Scheme

XL28C64A/65A Software Write Protect Feature

A powerful form of inadvertent write protection is provided by the nonvolatile data protect bit on the XL28C64A and XL28C65A. This software controlled bit determines the memory device's ability to respond to system generated write commands.

With the data protect bit set, the XL28C64A or XL28C65A power up with the on-board, high voltage write cycle disabled. This essentially renders the device a ROM. When E²PROM data alteration is desired, a software procedure is performed by the system, which resets the data protect bit, placing the device into a write enabled mode. When the write sequence is completed, the device can be returned to its ROM mode by setting the data protect bit. While the device is protected, brownouts and system crashes cannot generate unintentional data changes. This feature is described in detail in the respective data sheets.

Logic Certain Control Conditions

Each of EXEL's RAM-like E²PROMs requires a unique control pin combination which includes $\overline{WE}$, $\overline{CE}$, and $\overline{OE}$ in order to initiate a nonvolatile write cycle.

NV WRITE CYCLE INITIATION = $\overline{CE} \cdot \overline{WE} \cdot \overline{\overline{OE}} \cdot$ (protection conditions met)

(Equation 1)

Therefore, inadvertent write hazards will be circumvented by violating any one of these write conditions during system power transitions. This may be accomplished by holding either $\overline{CE}$ or $\overline{WE}$ up near V_{CC} or by "bootstrapping" $\overline{OE}$ to the ground rail. Since V_{CC} is changing during system power-up and power-down, the best solution is to hold $\overline{OE}$ at V_{SS} during perilous periods. Several simple circuits which perform this function will be discussed in the following sections.

On-Chip Protection Summary

Many useful features have been designed into EXEL's E²PROM products to eliminate the hazards of inadvertent data alteration. Each of these features addresses a particular aspect of the inadvertent write problem. By choosing the proper E²PROM device for a given application, the on-chip protection mechanisms will combine to shut out unintentional data changes (see Table 1). When redundant protection is desired, or when cost considerations override on-chip protection values, then external protection circuitry may be utilized to protect the nonvolatile data. This is the subject of the next section.

OFF-CHIP WRITE PROTECTION CIRCUITS

In some applications it is desirable to implement external power-up/down protection to enhance data security and prevent unusual conditions from risking the data integrity. EXEL E²PROMs are designed to accommodate external protection schemes, and some of the simple protection circuit solutions are discussed in this section. The fundamental principle is that inadvertent write signals which occur on the control bus may be blocked from the E²PROM by managing one of its control lines and violating the write condition when hazardous conditions exist. The primary concern is during power-up and power-down periods.

EXEL E²PROMs	$\overline{WE}$ Noise Filter	Logic Certain Control	Power-Up Write Delay	V_{CC} Lockout	Software Write Protect	Relative Effectiveness
XL2804A	Yes	Yes	Yes	3.0 V	No	Good
XL2816A	Yes	Yes	Yes	3.0 V	No	Good
XL28C16A	Yes	Yes	Yes	4.0 V	Yes	Excellent
XL2864A	Yes	Yes	No	4.0 V	No	Excellent
XL28C64A	Yes	Yes	Yes	4.0 V	Yes	Excellent
XL2865A	Yes	Yes	No	4.0 V	No	Excellent
XL28C65A	Yes	Yes	Yes	4.0 V	Yes	Excellent
XL46C15 XL46HC64/64L	No special protection required. High voltage programming only.					Excellent

Table 1. On-Chip Protection Features

Since both $\overline{CE}$ and $\overline{WE}$ must be low in order to initiate a nonvolatile write cycle (refer to Equation 1), holding either one of these signals to the V_{CC} rail will render the E²PROM ROM-like. Likewise, since the $\overline{OE}$ pin must be held high to initiate a write cycle, then holding it to the ground rail will also inhibit write commands from initiating a nonvolatile write cycle (see Table 2).

This, consequently, results in two basic approaches to external inadvertent write protection designs:

Service Accessed Firmware Applications

An example of Hold High Protection is shown in Figure 7a. This is a simple and inexpensive approach to eliminating unauthorized data changes. The switch may be a DIP switch mounted inside the machine available only to service personnel, a security lock-type switch (Figure 7b) or a contact made upon insertion of a programming cable (Figure 7c).

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
X	X	H	($\overline{WE}$) Write Inhibit
X	L	X	($\overline{OE}$) Write Inhibit
H	X	X	($\overline{CE}$) Write Inhibit
L	H	L	Write Operation Executed

Table 2.

With the switch open during normal system operation, the $\overline{WE}$ pin is held high via R_P, eliminating the chance of data alterations. When service personnel want to update the firmware, they simply close the switch, giving the system full access to the E²PROM's RAM-like interface.

APP. 4 NOTES

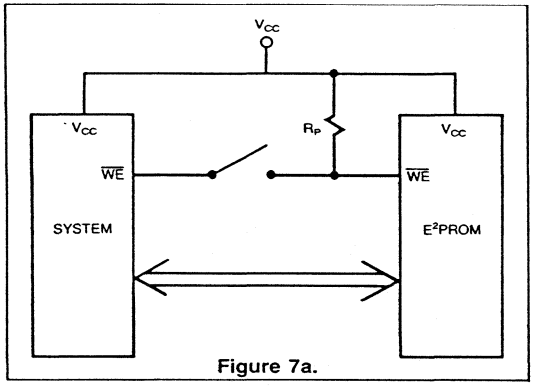


Figure 7a.

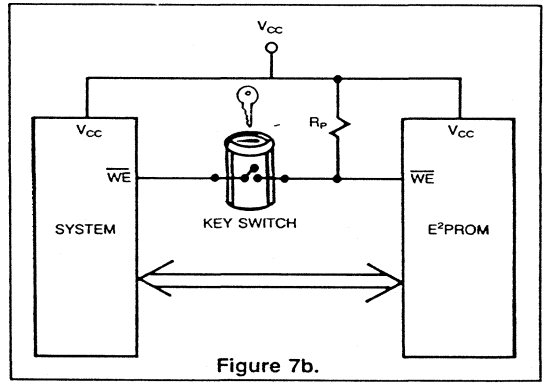


Figure 7b.

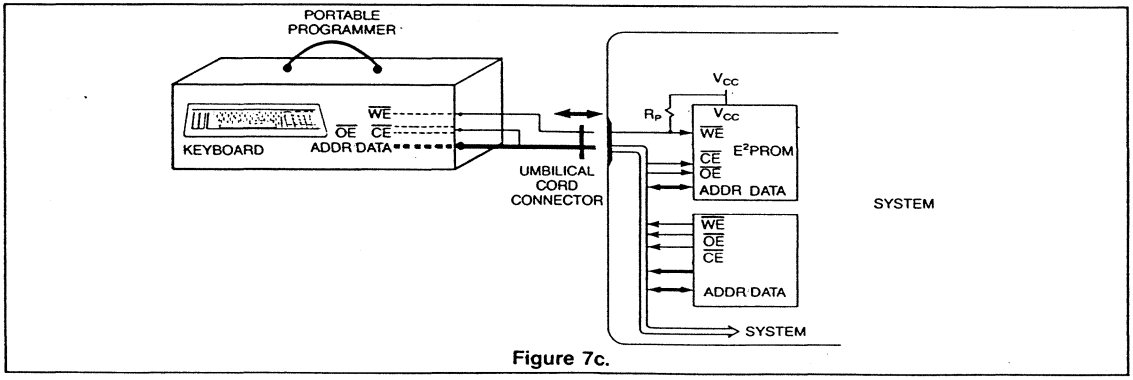


Figure 7c.

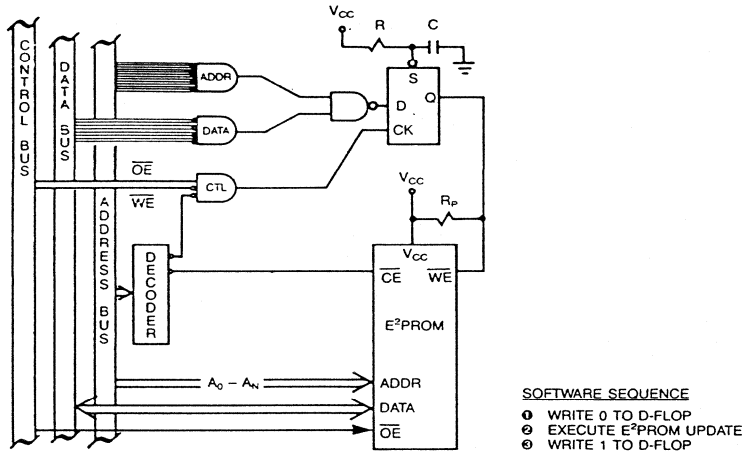


Figure 8. External Software $\overline{WE}$ Control

A second example is shown in Figure 8. This software controlled switch performs the same function as the hardware switch, yet it allows for software access and control. In this application, it is important to restrict the latch to a CMOS type, which will provide responsible outputs to V_{CC} levels below 3.0 V. During power-up, the RC circuit holds the $\overline{SET}$ input low to ensure that $\overline{WE}$ stays high. The address and data AND gates ensure that only a specific and unique address/data combination will provide a logic "0" to the D-latch input. The control AND gate clocks the data into the latch only when a system write cycle is directed to the latch. Upon this combination of events, the E²PROM $\overline{WE}$ pin is set low and data may be altered through write cycles in which bytes are clocked in using the $\overline{CE}$ control pin. Once the E²PROM data has been updated, the latch is reset to a logic "1" and the E²PROM becomes ROM-like once again.

Fully Automatic Power Transition Protection

The V_{CC} lockout mechanism described previously in the *On-Chip Protection Mechanisms* section is easily implemented externally, allowing the designer to set the V_{WI} trip point at any level desired. For example, a high precision machine might utilize many V_{CC} ±5% components and consequently a V_{WI} threshold set at 4.75 V would provide more security than the on-chip 4.0 V threshold. This may be accomplished by using one of the Intersil Programmable Voltage Reference options.

Intersil ICL8211/ICL7665 Solutions

Figure 9a shows the implementation of the Intersil ICL8211 to provide external V_{CC} monitoring and inadvertent write control. R_1 and R_2 are selected according to a formula supplied in the ICL8211 data sheet to provide the desired V_{WI} threshold voltage. The ICL8211 monitors the applied supply voltage level and when it drops below the V_{WI} defined by R_1 and R_2, its open collector output pin turns on, pulling the $\overline{OE}$ line low, thereby violating the necessary write condition. Consequently, any time that the supply voltage is below the specified level, write commands present on the control bus will be suppressed. Figure 9b shows the relationship between V_{CC} and V_{OUT} as the system turns on and then off again. Since the output driver of the ICL8211 is an open collector device, any other open collector driver may be used to control $\overline{OE}$ during normal system operation.

Note: V_{OUT} rises when V_{CC} is below 1.56 V. This is not an issue with respect to protecting the V_{CC} since the on-chip protection blocks writes when V_{CC} is below 3.0 V (XL2816A).

The ICL8211 provides a simple and inexpensive solution to the problem of automating V_{CC} level controlled inadvertent write inhibition. Intersil also offers a low power device which may be used in the same fashion. The Intersil ICL7665 is a Micropower Under/Over Voltage detector which performs just as the ICL8211 yet utilizes less than 3 μa of supply current (the ICL8211 specifies a typical value of 22 μa). Each of these Intersil components are available in an 8-pin mini-DIP, the T0-99 can and as die. Please refer to the Intersil Data Book.

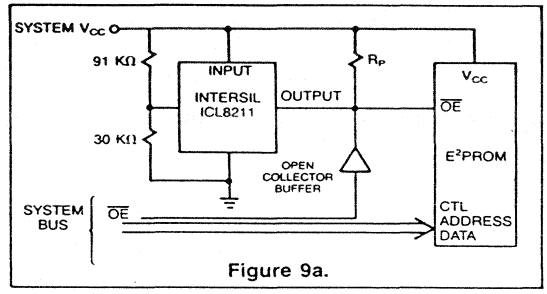


Figure 9a.

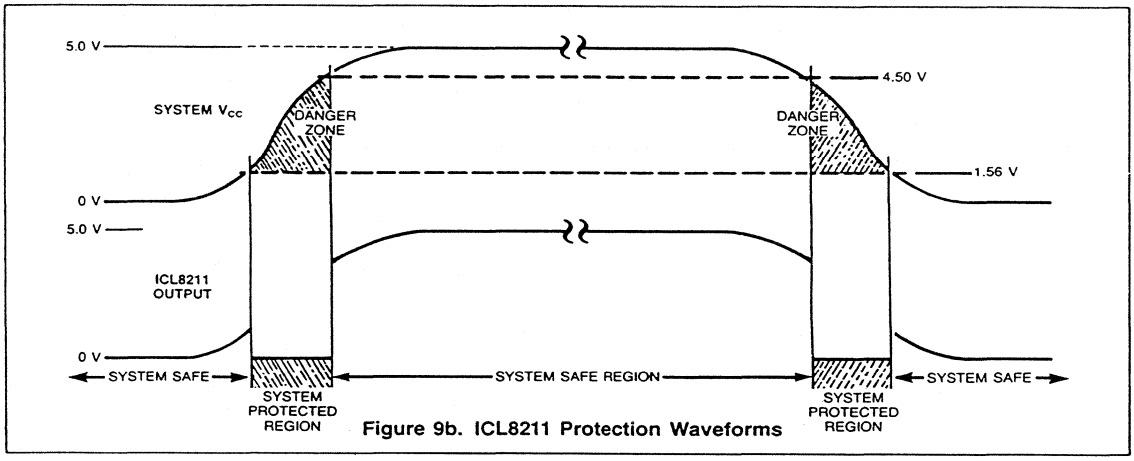


Figure 9b. ICL8211 Protection Waveforms

APP 4 NOTES

SGS L487 – Precision Voltage Regulator Solution

Designs which utilize a local 5-V regulator are very simply write protected by replacing the standard regulator with the L487 from SGS, a precision 500 ma 5-V regulator which provides two extra pins. Figure 10a shows the implementation of the L487. The reset-output-pin is an open-collector driver which provides a low output whenever the output voltage of the regulator drops below 4.859. When the output voltage is above the threshold voltage, the pullup resistor (R_P) holds $\overline{OE}$ high just as in the ICL8211 example. The delay-capacitor-pin can be tied to a capacitor (C_d) to define a power-up delay, providing additional protection during power-up like that incorporated in the XL2816A on-chip protection mechanism. Figure 10b shows the corresponding waveforms.

This solution is particularly attractive where board changes are to be avoided such as in the direct replacement of static RAMs or when an NMOS or TTL designer initially overlooked write protection for the XL2816A. The L487 may directly replace the existing regulator with the two additional pins wrapped up and appropriately connected via jumper wires!

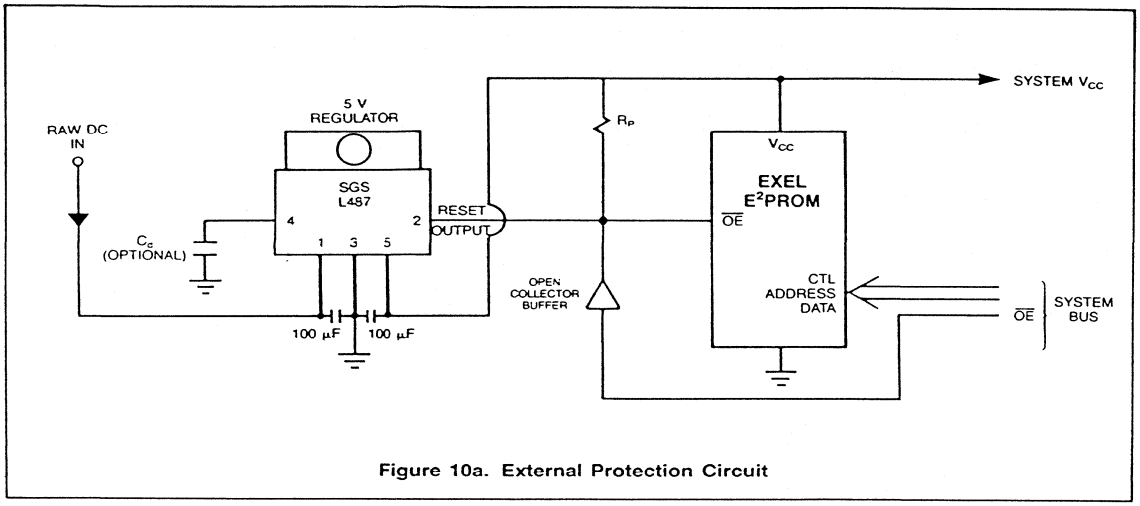


Figure 10a. External Protection Circuit

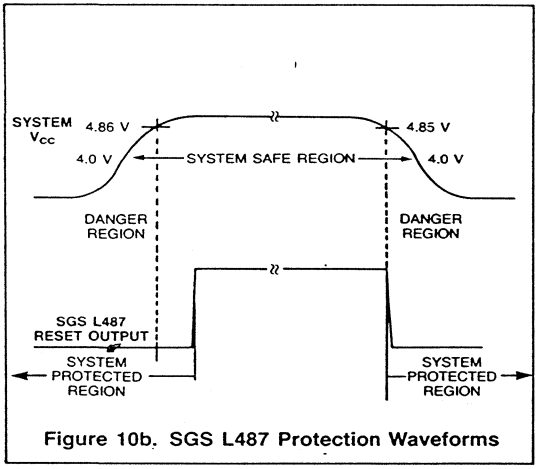


Figure 10b. SGS L487 Protection Waveforms

TL7705A – Supply Voltage Supervisor

A monolithic external inadvertent write solution from Texas instruments is shown in Figure 11. This device performs the same function as the ICL8211; however, the trip voltage is internally preset, eliminating the requirement for external resistors in the design. The open-collector RESET output controls OE just as in the previous examples. This output is specified to be low whenever V_{CC} is between 3.6 and 4.5 V. This can leave the device vulnerable in the range from 3.0 V, where the XL2816A internal protection takes over, and 3.6 V, where the TL7705A cuts in. Texas Instruments is developing an applications note to assist designers with this problem. Please contact Texas Instruments for current information.

Filtering Control Signals

If inadvertent write signals are occurring as a combination of spikes or glitches, the simple $\overline{RC}$ network shown in

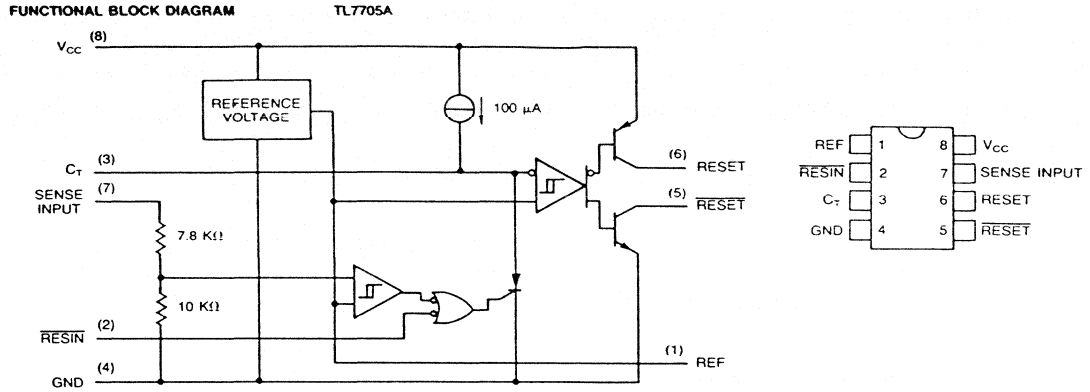


Figure 11. Texas Instruments Integrated Solution

Figure 12 will eliminate them by requiring extended pulse widths on the system bus to charge (or discharge) C_d before the signal is passed through to the E²PROM control pin. The diode serves to prevent the $\overline{WE}$ pin from being subject to negative voltage if V_{CC} drops to zero quickly. Note that this simple and inexpensive approach will increase the minimum $\overline{WE}$ pulse width which the system must supply during a write cycle. Slower systems will easily accommodate this constraint. However, high performance systems with normally short write pulse widths will require special consideration to successfully implement this solution.

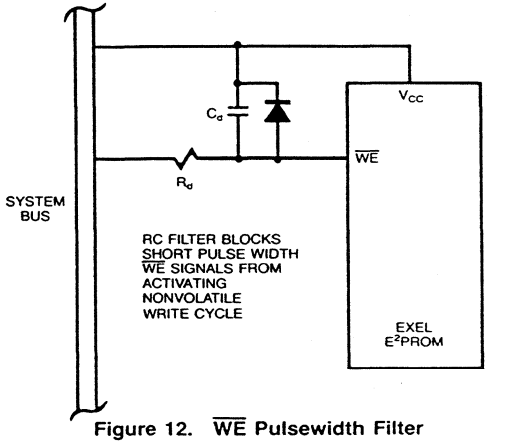


Figure 12. $\overline{WE}$ Pulsewidth Filter

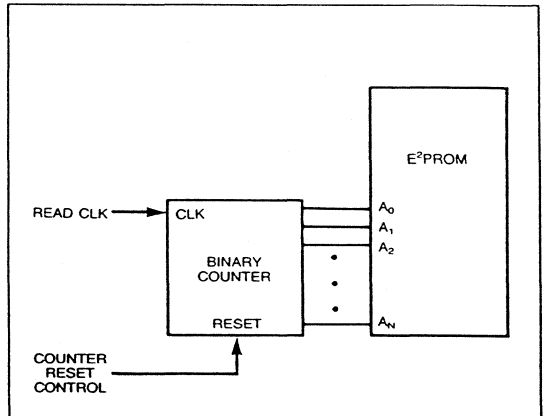


Figure 13. Byte 000 Sacrifice Method

Byte Sacrifice

One clever solution to the inadvertent write concern is shown in Figure 13. The system for which this was implemented was a message display unit which used a counter to sequence up through the memory array reading out the message to be displayed. During power transitions, the address lines are held at zero through the counter reset mechanism. Although inadvertent write cycles are not inhibited, any unintended data changes are directed to address zero, which is disregarded during normal system operation.

Plug-In Memory Cartridge Applications

The zero-power storage capability of E²PROMs makes them ideal for memory cartridge applications. Sporadic signals are inevitable during the physical cartridge insertion into a "hot" socket. To protect the E²PROM data integrity in such an environment the control pin contacts may be recessed so that they connect last during insertion and disconnect first during removal. Figure 14 shows the connection layout which ensures that the memory is powered up with the control pins held to V_{CC} or V_{SS} via R_P to violate the write condition until the active system takes control.

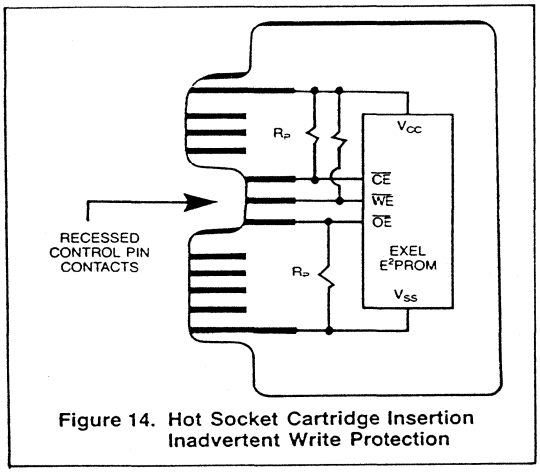


Figure 14. Hot Socket Cartridge Insertion Inadvertent Write Protection

One other concern with cartridge applications is the threat of Electro-Static Discharge (ESD) damage while the cartridge is unsocketed. To limit the potential voltage and current surges applied to the E²PROM inputs, current limiting resistors and input protection diodes are recommended as shown in Figure 15a. Figure 15b shows these diodes being replaced by a single Zener diode as an alternate solution. In either case, design consideration must be given to the magnitude of anticipated ESD voltages in selecting the value of the limiting resistors as well as in choosing diodes with the surge current capacities and switching speeds necessary. The input itself may be simply modeled as a 10 pF capacitor as in Figure 15c.

Figure 15. E²PROM Cartridge Applications ESD Protection

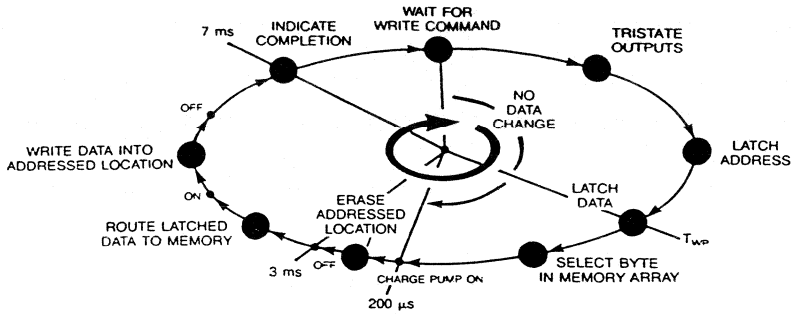


Figure 16. Self-Timed E²PROM Write Cycle State Diagram

APP. 4 NOTES

POWER CRASH!

Once unintentional write commands have been eliminated either through EXEL's advanced on-chip protection or through one of the external solutions, the data stored in the nonvolatile array is secure. Having thought the problem through to this degree of understanding, one issue frequently arises as a question (and a good one at that) yet rarely is an actual problem:

What If the Power Fails During the 10 ms Nonvolatile Write Cycle?

The answer tends to be quite favorable in the vast majority of systems. It turns out that due to the system capacitance, the actual power-down time is many, many times longer than the 10 ms required to complete the nonvolatile write cycle. Consequently, in the unlikely event of a power failure occurring while a nonvolatile write cycle is in progress, the write cycle would most probably complete long before the power supply drops to V_{WI}. On EXEL E²PROMs, V_{WI} is the point below which the on-chip charge pump is disabled and any write cycle in progress is aborted. The possibility exists that a nonvolatile write cycle could be initiated as power is falling off and approaching V_{WI}. In this case the cycle would be aborted during execution.

Small systems which have very little capacitance might, however, have the V_{CC} roll off in less than 10 ms. It is useful, therefore, for designers to have insight into the potential hazards of power-crash aborted nonvolatile write cycles. Figure 16 shows the internal sequence of events and *approximate* timings of each. The internal charge pump is disabled whenever $V_{CC} \leq V_{WI}$, so the sequence will run its course until the V_{WI} threshold is crossed. After this time, there is no longer the high voltage present which is necessary to cause nonvolatile data alterations.

Only the Byte (or Page) Being Operated Upon is At Risk!

Many of the competing E²PROM manufacturers will not guarantee any particular performance, or resultant data pattern, if power fails during a nonvolatile write cycle. They say that the final data (throughout the array) is unpredictable, rendering such a situation to be (as far as the data is concerned) a catastrophic failure. They also say that they are not responsible since you are operating their device in an out-of-spec application.

EXEL memory designers took this problem into account during the design phase to ensure that only the addressed locations would be affected by a power failure when a write cycle is in progress. To accomplish this, they ensured that both the data and address latches operate reliably until V_{CC} is well below V_{WI}.

Figure 17 shows a simple circuit which may be used to provide power to the E²PROM to make sure that nonvolatile write cycles are completed even if interrupted by a power failure. The capacitor is charged up to 5 V during normal power-up and steady state operation. Once power fails, the super capacitor discharges through the E²PROM, providing I_{CC} for 10 ms so that the nonvolatile write cycle may be completed. Note that this design renders the on-chip V_{CC} lockout protection circuit useless during any power-down phase since the E²PROM V_{CC} will lag the system V_{CC}. This particular approach would be ideally suited to the XL28C64 due both to its sophisticated software controlled inadvertent write protection and to its low power consumption.

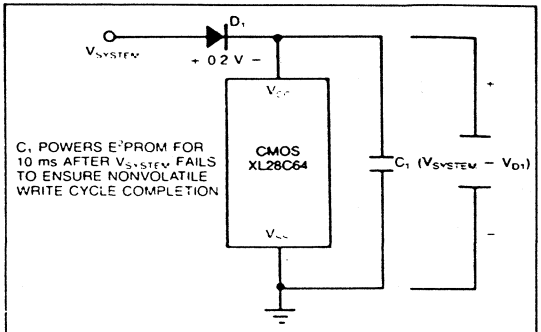


Figure 17. Power Crash Protection

EXAMPLE (XL28C64):

1) Recall $I = C\ dv/dt$

2) Use $I = I_{CCW}$
(max current during nonvolatile write cycle)

$I_{max} = 60$ mA

3) Use $dV = (V_{SYST} - V_{D1}) - 4.5$ V

where: $(V_{SYST} - V_{D1})$ is V_{CC} at the start of crash

4.5 V is the minimum specified operating voltage

$V_{D1} = .2$ V (germanium)

4) Use $dt = t_{NW} = 10$ ms

5) Solve for C_1

$C_1 = I\ dt/dV$

$C_1 = 60$ mA * 10 ms / 300 mV

$C_1 = 2000\ \mu F$

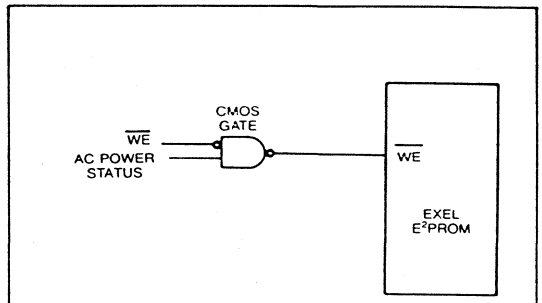


Figure 18. Power Status Conditioned $\overline{WE}$ Signal

Power Status Conditioned Write Signal

Another approach to the remote hazard of a power-down during a write cycle is to condition the initiation of write cycles with power status information. For example, Figure 18 shows the $\overline{WE}$ signal from the control bus conditioned by the presence of AC at the power supply input. If the AC is not present then the write cycle will not be initiated and if it is present then a write cycle will have time to complete since, if the AC failed in the next moment, the system capacitance would carry the nonvolatile write cycle to completion. This AC signal could also be tied to an interrupt which initiates a power-crash routine and prevent nonvolatile write cycles through software.

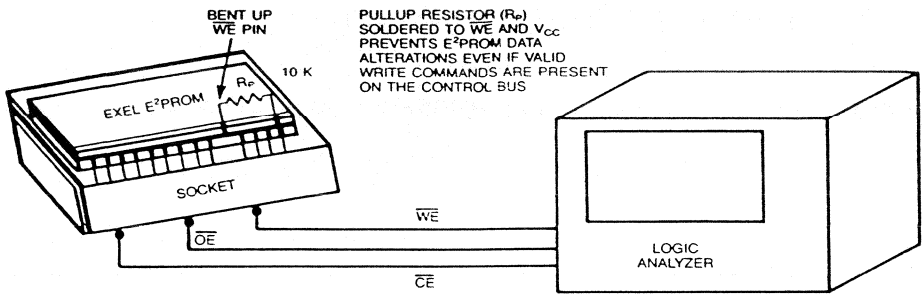


Figure 19. Troubleshooting Test Setup

TROUBLESHOOTING INADVERTENT WRITE COMMANDS

The elimination of inadvertent write commands in a system with operational hardware may require pinpointing and identifying their occurrence. They often have a random nature which can frustrate even the best debuggers. Fortunately, there are two simple ways to find them.

Protecting E²PROM Endurance

Since the inadvertent write phenomenon occurs on the system bus independently of the E²PROM, unnecessary memory write cycling may be prevent by removing the device from its socket during the testing procedure. In systems where the E²PROM data is required for system operation (i.e., control store programmed into the E²PROM), you may eliminate any write cycles from altering the E²PROM data by bending the $\overline{WE}$ pin up out of the socket and tying it to V_{CC} via a pullup resistor. This allows the E²PROM to be read while preventing any data alterations.

Logic Analyzer Method

Pinpointing inadvertent write commands can be easily accomplished through the use of an advanced logic analyzer by connecting it to the control bus which operates the E²PROM $\overline{OE}$, $\overline{CE}$, and $\overline{WE}$ pins. By setting the trigger condition to be $(\overline{OE} \geq V_{IH}) \cdot (\overline{CE} \leq V_{IL}) \cdot (\overline{WE} \leq V_{IL})$, the logic analyzer will trip whenever a valid write command is encountered on the system bus.

Procedure

1. Allow the system to operate in a region of control store where no E²PROM write commands are issued (i.e., an endless loop performing some other function).

2. Switch the system on and off several times, watching for the logic analyzer to trigger. This will cycle the test system circuitry through its power-up and power-down transitions, while you watch for unintended write commands to trigger the logic analyzer.

3. If many on/off cycles do not provide a valid write command, you may want to implement a clock to control the system power supply, switching it on and off every several seconds and letting it run over an extended period. Inadvertent write commands on the control bus may be due to random signals and bus contentions which only produce a valid write command once in many, many power transition cycles. To ensure a reliable system design without providing additional hardware protection, it is important to cycle several system samples extensively, while monitoring the control bus for hazards.

If any inadvertent write commands is observed, you can zero in on its timing and source by repeating the cycling while systematically reducing the logic analyzer ranges. Once the problem and its timing is pin-pointed, an appropriate protection mechanism may be implemented to block it. When this protection installation is complete, repeat the cycling until you are confident that the problem has been eliminated.

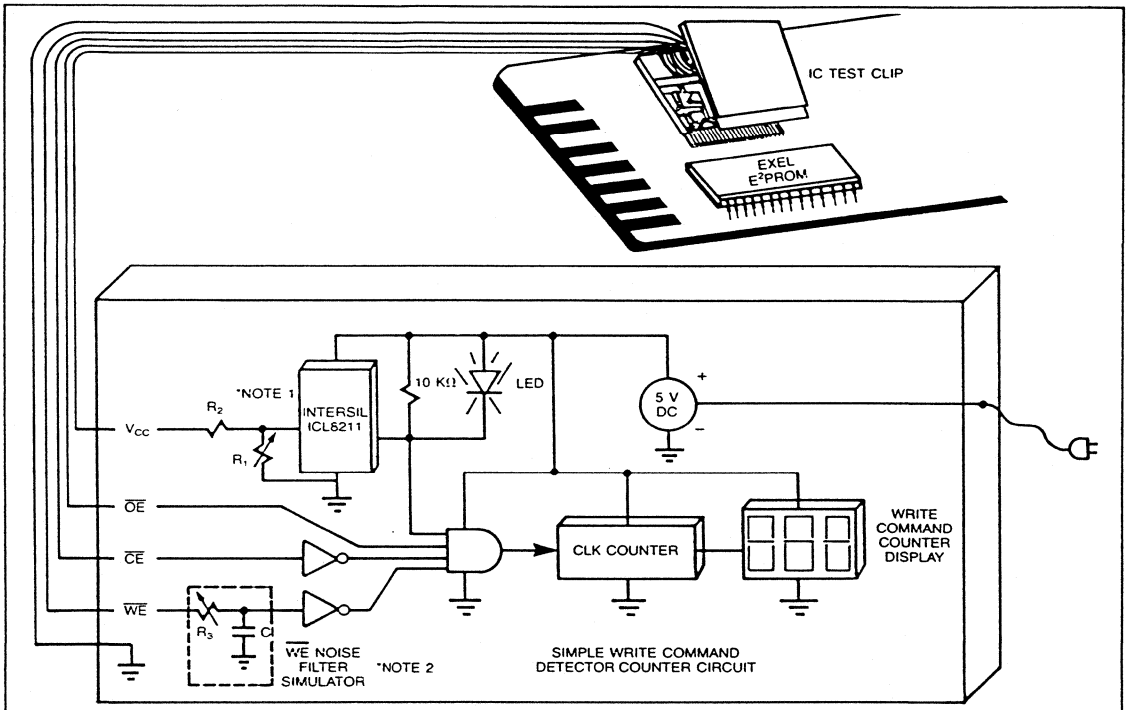


Figure 20. Circuit Recognizes Control Bus/V_{CC} Conditions Which Could Initiate a Nonvolatile Write Cycle

*NOTE 1: $V_{THRESHOLD}$ = Input level trip voltage which changes output state.

$$V_{THRESHOLD} = \frac{(R_1 + R_2)}{R_1} (1.15\,V)$$

*NOTE 2: RC Filter is adjusted to block $\overline{WE}$ low pulses of ≤20 ns duration; use pulse generator and scope to trim R_3.

Write Command Detector/Counter

In the absence of a sophisticated logic analyzer, a simple circuit can be built to detect and count valid write commands issued to the E²PROM. Figure 20 shows a logic configuration which emulates the E²PROM's internal protection mechanisms to avoid counting write cycles which would be blocked out by the integrated protection and counts only those which might initiate a nonvolatile write cycle, causing nonvolatile data changes.

The counter will advance whenever a valid write command is detected.

Valid write command = $(\overline{OE} \geq V_{IH}) \cdot (\overline{CE} \leq V_{IL}) \cdot (\overline{WE} \leq V_{IL}$ for ≥ 20 ns$) \cdot (V_{CC} \geq V_{THRESHOLD})$

R_1 is adjusted to set the ICL8211 threshold voltage to a desired level (3.0 V for XL2816, 4.0 V for XL2864A, etc.). This threshold voltage may also be systematically varied so that the voltage at which the problem write cycles begin can be determined.

ECL or equivalently fast components should be used in building the detector to ensure recognition of short (20 ns) pulses. Use a separate 5 V supply, so that the detector/counter circuitry will operate reliably while the test system power supply is cycled on and off.

The detector/counter is used by connecting the clip contacts to the V_{CC}, V_{SS}, $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ pins on an in-circuit E²PROM. The system is run and its power cycled while the counter is monitored for E²PROM write commands. If the detector counts more write cycles than the system software is intended to issue, then either a software bug or hardware hazard is indicated.

SECTION 5 Table of Contents

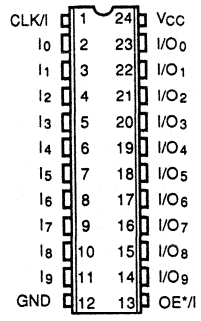
Multi-Level E²PLDs

FEATURES

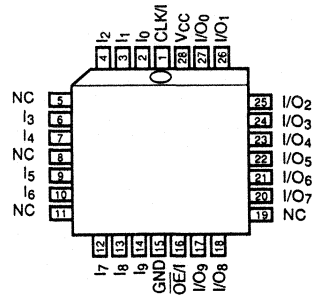
- 600-800 Gate Equivalent Logic Complexity
- Industry-Standard Data I/O ABEL™ PLD Design Tool Compatibility
- Advanced ERASIC Architecture
  - — True gate array style logic integration
  - — From 1 to 42 internal logic levels without using a pin
  - — Eliminates 2-level logic restriction of conventional PLDs
  - — 10 Buriable JK/T/D Flip-Flops
  - — Flip-flops may be connected to any logic level
  - — 2 term-controlled 4-bit input latches
  - — 64-way Programmable I/O Macrocell
- 2-Micron E²CMOS Technology
- Electrically Erasable and Programmable
  - — Reprogrammable 10,000 times (min.)
  - — Reprogrammable in plastic packages
  - — Reprogramming time less than 5 seconds, including erase and verify
  - — 100% Factory Tested
- Security Plus Provides Design Security Plus 100% Verification Capability
- High Performance
  - — 35ns Maximum One-level Propagation Delay
  - — 50ns Maximum Two-level Propagation Delay
  - — 15ns Maximum Internal Propagation Delay Per Level
- Low Power
  - — 20mA current for typical designs at 10MHz
  - — Uses power only for logic used
- Pin-compatible with 24-pin PAL® Devices
- Windowless 24-pin 300-mil DIP
- TTL and CMOS Compatible Inputs and Outputs
- 8mA/4mA Output Sink and Source Capability
- Programmable on Conventional PLD Programmers
- 5V Operation

PIN CONFIGURATION

24 Pin Skinny DIP
Type "P3" Package



28 Pin PLCC
Type "D" Package



PIN NAMES

I0...I9	Inputs
I/O0...I/O9	Inputs/Outputs
$\overline{OE}$/I	Output Enable/Input
CLK/I	Clock/Input

APPLICATIONS

- Programmable replacement for conventional logic families
- -LSTTL, ALS, CMOS
- Fast-turnaround, low-risk gate array alternative
- Low-power, high-functionality alternative to existing Programmable Logic Devices. One device may replace 3-4 PALs.

DESCRIPTION

The ERASIC XL78C800 is an electrically-reprogrammable CMOS ASIC component with multi-level logic capabilities. Designed to integrate a wide variety of user-defined logic functions onto a single package, this fast-turnaround ASIC device is an ideal choice when time-to-market, board space and power are at a premium.

The XL78C800 features an equivalent gate complexity of 600-800 gates packaged in a space-saving 300-mil 24-pin package. Fabricated using EXEL's high-performance double-metal E² -CMOS process, the XL78C800 typically requires a supply current of less than 20mA and may be electrically erased and programmed in less than five seconds total.

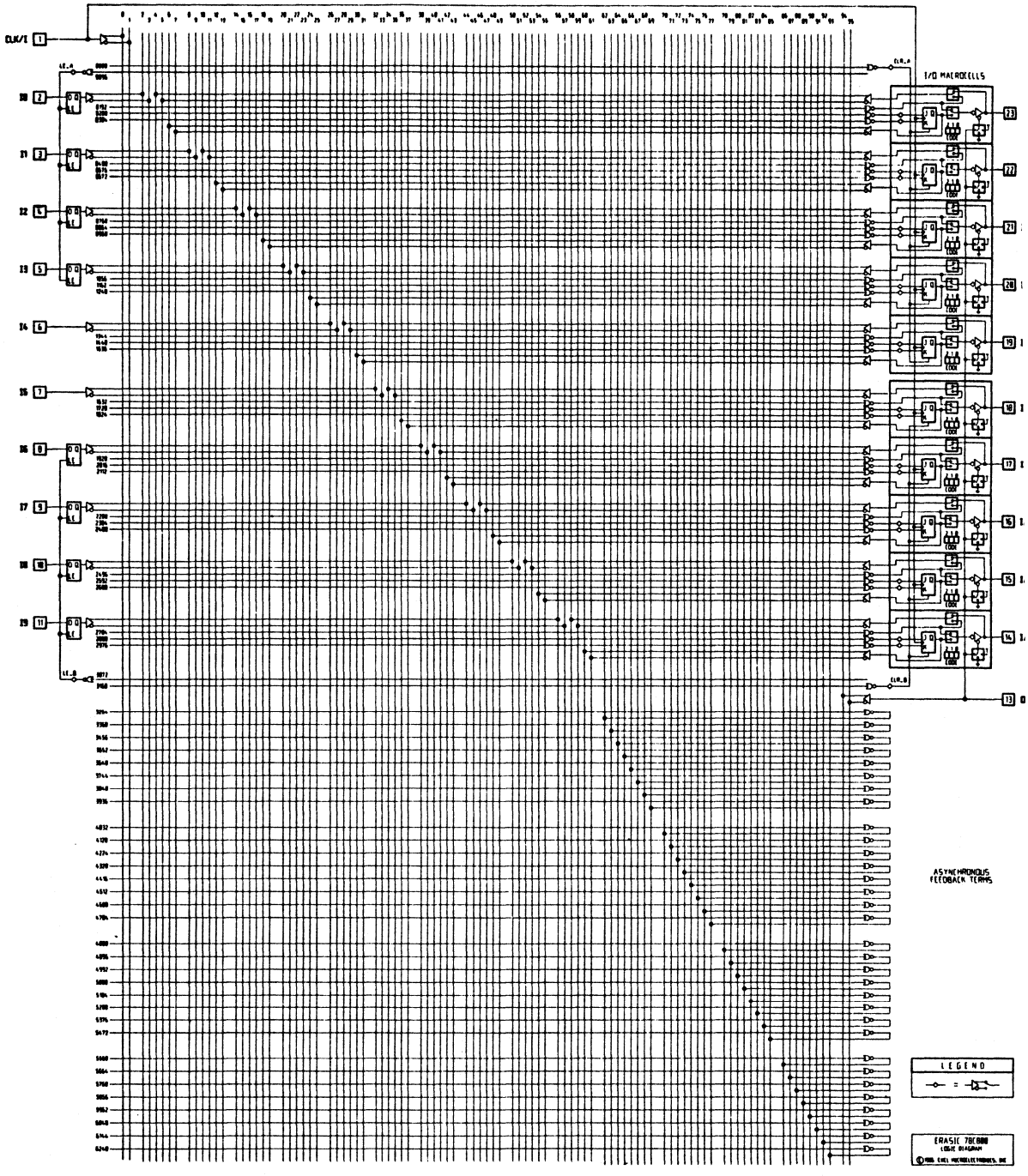


FIGURE 2. ERASIC XL78C800 LOGIC DIAGRAM

ERASIC XL78C800

The ERASIC XL78C800 is an advanced electrically-reprogrammable ASIC component designed for integration of complex user-defined logic. The XL78C800 offers multi-level logic and buriable JK Flip-Flops, thereby enhancing logic design options, increasing integration and maximizing performance.

Architectural Overview

At the heart of the ERASIC XL78C800's multi-level capabilities is the Folded-NOR architecture. This architecture, consisting of a single programmable NOR plane, can generate N internal levels of logic with N passes through the NOR plane. The folded terms, called asynchronous feedback terms, act as both array outputs and inputs, and are used to generate the multiple internal logic levels. The XL78C800 implements all combinatorial logic by using one or more NOR functions along with programmable input and output polarity.

Advantages of Multi-Level Logic
■ increases design flexibility ■ increases integration ■ allows TTL-type design ■ higher PLD utilization ■ eliminates unnecessary I/O delays ■ enhances design security

ERASIC XL78C800 ARCHITECTURE

The diagram in Figure 2 illustrates the key elements of the ERASIC XL78C800 architecture. The electrically-erasable NOR array consists of 96 inputs (vertical columns) by 66 terms (horizontal rows). Each term generates a NOR function of its enabled input lines. Inputs can be selectively enabled by programming the E^2PROM memory cell at the associated intersection. Each term, by selecting proper input and output polarity, can be made to operate logically (via DeMorgan's Theorem) as any 1-Level Boolean function, hence the name 'term,' not 'product term.'

Since each term can generate a generic one-level function, multi-level logic is generated simply by cascading multiple terms. The bottom-most 32 terms of the logic diagram are dedicated to this purpose. These asynchronous feedback terms feed back their output into the array as input, and allow creation of sum-of-products, product-of-sum, or higher-complexity multi-level logic functions.

The asynchronous feedback terms feed back only the NOR sense of their output and do not provide programmable output polarity. This is sufficient since next-level asynchronous logic functions which would require the OR output are easily transformed to eliminate this requirement. This transformation process is performed automatically by EXEL's AdET 1.0 software.

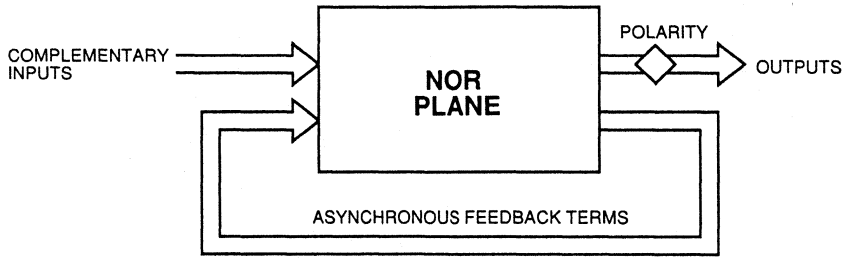


FIGURE 3A. SIMPLIFIED FOLDED-NOR ARCHITECTURE

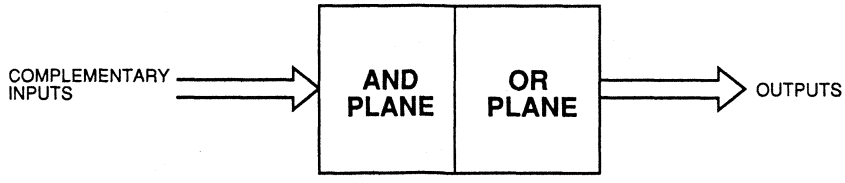
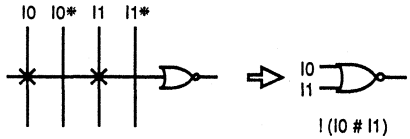


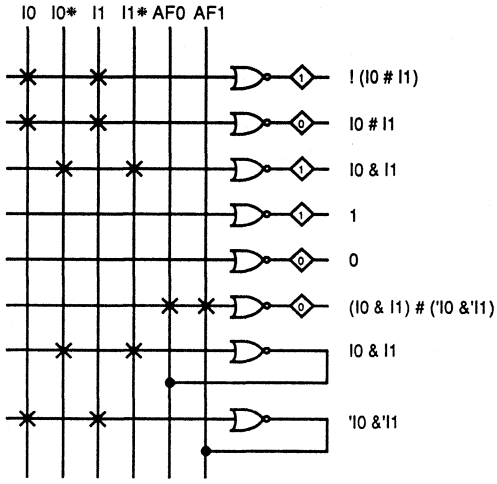
FIGURE 3B. SIMPLIFIED AND-OR ARCHITECTURE

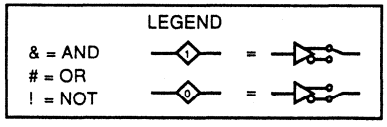
Logic Diagram Functionality

The XL78C800 logic diagram describes logic functionality in a manner similar to conventional PLD logic diagrams. An 'X' drawn at an intersection of term and input lines indicates that the input is enabled for that term. Since the XL78C800 is NOR-based, the inputs represent inputs to a NOR gate.



Addition of Polarity Control Elements (PCEs) and asynchronous feedbacks completes the basic set of array logic operators.





I/O MACROCELL ARCHITECTURE

The XL78C800's ten I/O Macrocells form an integral part of the device's logic capabilities. The three terms feeding the I/O Macrocell are called the J, K and O terms. J and K terms feed the JK Flip-Flop, while the O term is used for asynchronous output and/or asynchronous feedback. By providing dual synchronous and asynchronous logic paths, the XL78C800 allows the Flip-Flop to be used even if the I/O pin is used as an asynchronous input or output.

The I/O Macrocell architecture is detailed in Figure 4. In addition to the JK Flip-Flop, its major components are three programmable multiplexers and three polarity control elements. Each Macrocell may be independently configured via six architecture fuses. Three of the fuses set the state of the Polarity Control Elements, which are shown as diamonds. The PCE's act as inverters if their fuses are programmed to a "0," and as non-inverting buffers if programmed to a "1."

CONFIGURING THE I/O MACROCELLS

The remaining three architecture fuses C0, C1 and C2, set the state of the three multiplexers. The Out Mux selects either the O term or the Flip-Flop Q signal for output to the pin. The In Mux selects either the O term or the pin as an array input. The $\overline{OE}$ Mux selects either the $\overline{OE}$ input (pin 13), a fixed 0, or a fixed 1 as the output driver enable. The C2, C1 and C0 fuses are logically decoded into the four required Mux control signals, allowing the Macrocells to be configured simply by selecting a 3-bit code. The eight Macrocell configurations and their fuse codes are summarized below and illustrated in Figure 5. Note the availability of the 0 term as an additional asynchronous feedback in many of the configurations.

I/O Macrocell Fuse Codes

CONFIGURATION	CODE [C2, C1, C0]
O Term Output	011
O Term 3-State Output	111
Q Output	010
Q 3-State Output	110
Pad Input	000
Pad Input/O Term 3-State Output	101
Pad Input/Q 3-State Output	100
No Connect	001

The $\overline{OE}$ input pin is used as the Output Enable for Macrocell configurations with 3-State Outputs. When asserted, $\overline{OE}$ enables the selected outputs; when negated, $\overline{OE}$ disables the selected outputs (Hi-Z). $\overline{OE}$ has no effect on Macrocells in other configurations.

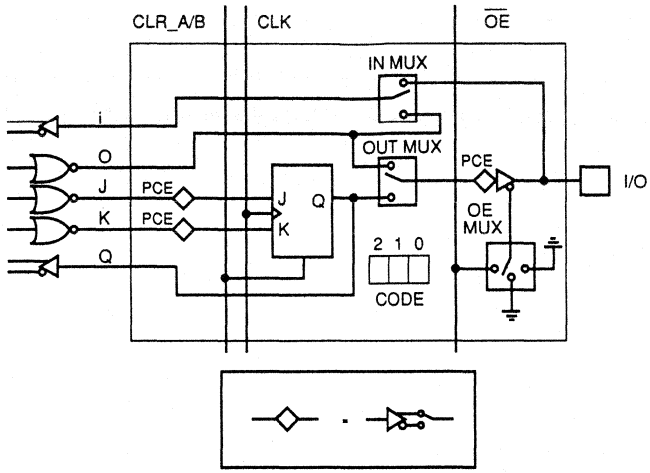


FIGURE 4. XL78C800 I/O MACROCELL

JK FLIP-FLOP OPERATION

The JK Flip-Flop is positive-edge triggered. The J and K inputs are driven by the J and K Terms, whose polarity is configured via two polarity control elements. The Q output is unconditionally fed back into the array and may additionally drive the pad via the programmable output driver. All Flip-Flops are initialized at power-up with Q set to 0. In addition, two asynchronous clear terms can be used to clear the Flip-Flops during logic operation. CLR_A clears the Flip-Flops within Macro-cells 0 through 4, while CLR_B clears the Flip-Flops within Macrocells 5 through 9.

JK Flip-Flop Operation

CLEAR	J	K	CLK	Q
1	X	X	X	0
0	0	0	↑	hold
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	toggle

The JK Flip-Flop can easily emulate either a D or T Flip-Flop. For a D Flip-Flop, the J and K inputs are supplied with the D and $\overline{D}$ values respectively. Similarly, for a T Flip-Flop, the J and K inputs are both supplied with the T input value. The JK-to-D translation is done automatically in the AdET 1.0 design tool software.

TERM-CONTROLLED INPUT LATCHES

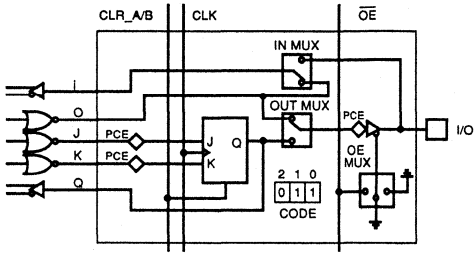
Inputs I0..I3 and I6..I9 serve as latchable 4-bit input ports. The latching of these ports is controlled by the LE_A and LE_B Terms, respectively. When LE is LOW, the latches are transparent and the Q outputs asynchronously follow the D inputs. When LE goes HIGH, data at the D inputs will be retained at the Q outputs until LE returns LOW.

The Latchable Input Ports are designed to provide a "snapshot" capability for asynchronously changing input signals that must be sensed at a particular point in time. The ports contain specially designed latches which quickly resolve the input levels when LE is asserted, providing unconditional stability regardless of the input signal characteristics.

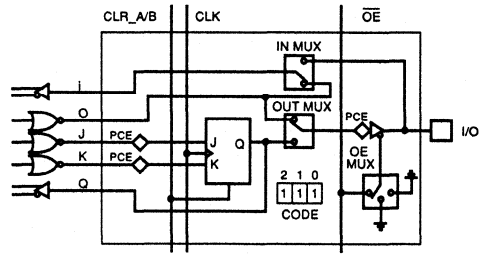
Each LE Term has programmable polarity via a Polarity Control Element. Additionally, if a Latchable Input Port is not required for a particular design, it can be made permanently transparent by programming its LE Term to a fixed LOW. Input latches are not cleared at power-up.

SECURITYPLUS SYSTEM

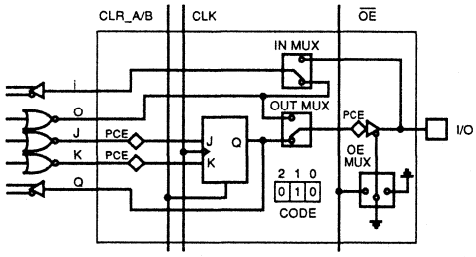
The XL78C800 incorporates an advanced design security system which offers a high-level of design copy-protection while maintaining 100% programming verification. SecurityPlus can be enabled by setting a special security E^2 cell during programming. When activated, it prevents the logic configuration from being read out or from being



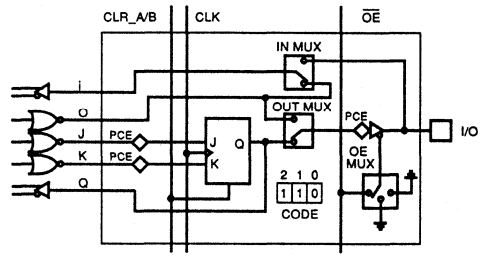
O Term Output



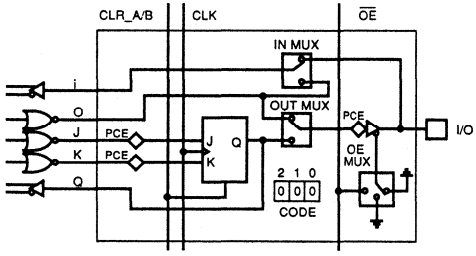
O Term 3-State Output



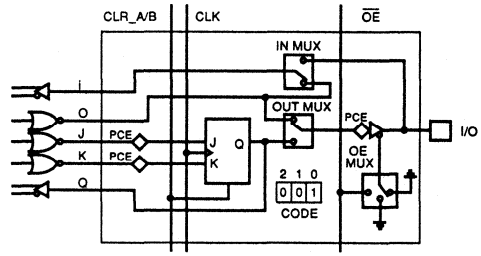
Q Output



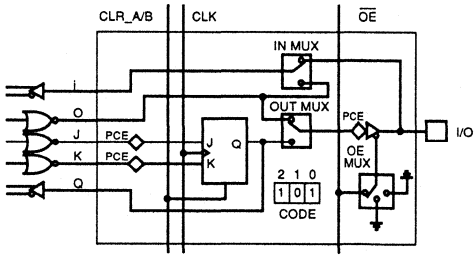
Q 3-State Output



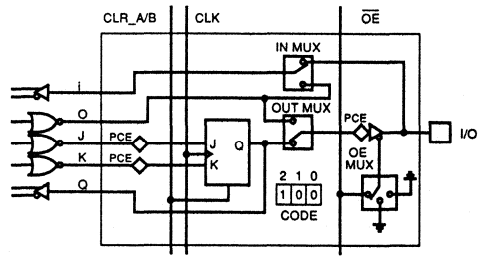
Pad Input



No Connect



O Term 3-State Output/Pad Input



Q 3-State Output/Pad Input

FIGURE 5. I/O MACROCELL CONFIGURATIONS

modified via additional programming. Only a complete erasure will disable the security. In addition, the XL78C800's E^2PROM technology eliminates the possibility of reverse-engineering via optical inspection, since programming does not create the blown fuses of bipolar fuse-link PLDs.

The SecurityPlus system is not activated until the first power-up following programming of the security bit. This allows the entire device, including the security bit itself, to be read out and verified as long as V_{CC} is maintained.

REGISTER PRELOAD

The XL78C800 incorporates an externally controlled preload function. Raising the CLOCK input to 12V causes any currently enabled outputs to be disabled. A preload value can then be placed on the I/O pins and will be preloaded into the JK Flip-Flops in the I/O Macrocells at the next rising edge of the clock. Thereafter, the device will return to normal operation.

ERASIC DESIGN TOOLS

Logic designs using the ERASIC XL78C800 can be created with the AdET 1.0 programmable logic development software. AdET is available from EXEL Microelectronics.

ERASIC PROGRAMMING TOOLS

The ERASIC XL78C800 may be programmed via industry-standard PLD programmers such as those offered by DATA I/O. The Data I/O Generic PLD adapter (Version 3) is required for the XL78C800.

EXEL also offers an ERASIC programming system for IBM-PC, XT, AT and compatibles and Sun Workstations. For further information please contact EXEL directly.

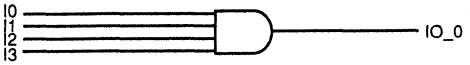
LOGIC DESIGN WITH THE ERASIC XL78C800

Logic design techniques for the ERASIC XL78C800 are illustrated in the 'ERASIC Sampler' circuit of Figure 6. This single-chip design contains numerous circuits ranging in complexity, and is shown in AdET form, along with schematics for reference.

One-Level Logic

The first Sampler circuit is a basic 4-input AND gate, in which IO_0 is the AND of I0..I3. The AdET notation for this circuit is simply:

IO_0 = I0 & I1 & I2 & I3; "AND"



Thus, pin 23 (which has been named IO_0) will be an AND function of pins 2, 3, 4 and 5 (which have been named 10, 11, 12, and 13). That is all that's needed, as polarity and I/O Macrocell architecture are derived automatically in the design software.

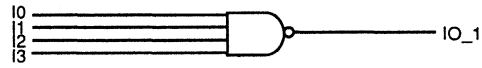
For those unfamiliar with AdET notation, the symbology is as follows:

& = AND
# = OR
! = NOT
$ = XOR

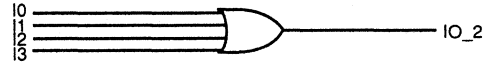
"comment" or /* comment */

The next three circuits are similar, except they perform the NAND, OR and NOR functions, and are output on IO_1..IO_3. Like the AND, these one-level functions require a single term for implementation.

IO_1 = !(I0 & I1 & I2 & I3); "NAND"



IO_2 = I0 # I1 # I2 # I3; "OR"

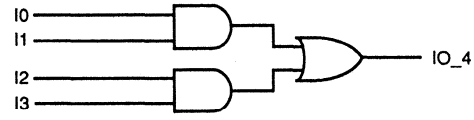


IO_3 = !(I0 # I1 # I2 # I3); "NOR"

Two-Level Logic

For two-level Sum-of-Products (SOP) functions, one enters equations as with conventional two-level PLDs.

IO_4 = (I0 & I1) # (I2 & I3);
"Sum-of-Products"



AdET automatically assign asynchronous feedbacks to achieve this two-level function. Feedbacks generate the first-level product terms. These terms are then summed by the 0 term and output to the pin. Much like conventional AND-OR PLDs, the default implementation for complex logic functions in the XL78C800 is minimized sum-of-products. That is, if one defines an output pin as a function of various input pins, and that function is not a one-level

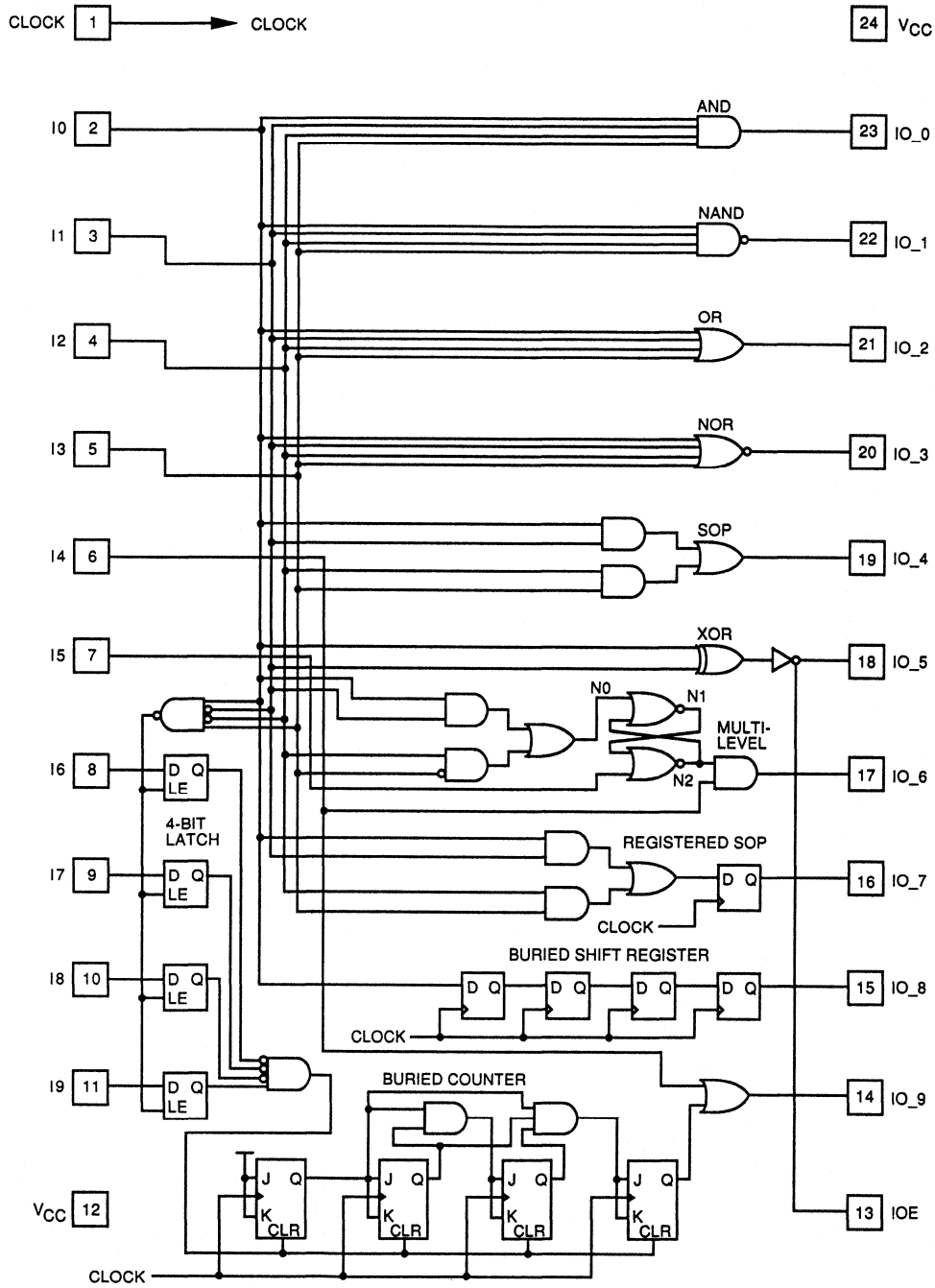


FIGURE 6. ERASIC SAMPLER SCHEMATIC

function (i.e. AND, NAND, OR, NOR), the function will be implemented as a two-level sum-of-products.

A Sum-of-Products function with an active-LOW output (AND-NOR) can be implemented by using the '!'operator on the left-hand side of the equation.

!IO_4 = (I0 & I1) # (I2 & I3);
"SOP, active-LOW output"

This function is the logical complement of previous active-high SOP function, being identical in implementation except for a complemented output polarity fuse. The Sampler design uses the active-high SOP function.

Another useful two-level function is the Exclusive-OR, which is described using the convenient XOR operator:

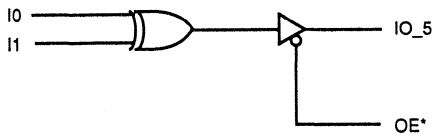
IO_5 = I0 $ I1; "XOR"

The XOR function is automatically implemented in sum-of-products form, in this case **!IO & I1 # I0 & !I1.**

If IO_5 is to be enabled only when the $\overline{OE}$ pin is brought LOW, and three-stated otherwise, one adds the statement:

Enable IO_5 = $\overline{OE}$;

IO_5 is now enabled only when the $\overline{OE}$ signal is a 1. The fact that the $\overline{OE}$ pin is active-LOW is handled in the pin declaration by the '!' preceding the '$\overline{OE}$', allowing $\overline{OE}$ to be treated as an active-HIGH signal. (Note the distinction between pin and signal.) Any or all I/O pins can made three-state and/or bidirectional using this technique.

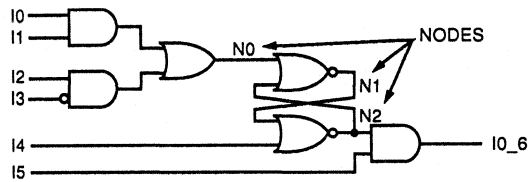


Multi-Level Logic

There are many circuits which are impossible or inefficient to implement in two or fewer levels of logic. In many cases, these circuits can be constructed using multi-level logic. Multi-level logic is logic composed of a variety of levels and interconnected in non-sequential fashion. Multi-level logic need not be a specific number of levels (e.g. two-level) and it need not be interconnected in a pre-determined, sequential fashion (e.g. AND->OR->AND->OR). It is, in effect, 'random-logic' as applied to PLDs.

Construction of multi-level logic circuits relies on the concept of nodes. Nodes are like pins, but are buried inside the device. Nodes can be given names, assigned logic functions and then used in the definition of other nodes or pins. This allows familiar PLD logic constructs to be cascaded and or interconnected in virtually any way. In addition, logic signals not needed outside the chip can stay inside, where they avoid delay and pin-usage. As an example, consider the asynchronous Set-Reset latch circuit below. Here, a cross-coupled pair of NORs is cleared when 14 is HIGH, and set when I0 and I1 are HIGH or I2 and I3 are HIGH and LOW respectively. IO_6 then outputs the latch value, asynchronously conditioned by I5. Describing this circuit requires three nodes, arbitrarily named N0, N1 and N2.

```
N0  = (I0 & I1) # (I2 &!I3);   "SR latch Set function"
N1  = (N0 # N2);               "SR latch NOR gate 1"
N2  = (I4 # N1);               "SR latch NOR gate 2"
IO_6 = I5 & N2;                "output AND function"
```

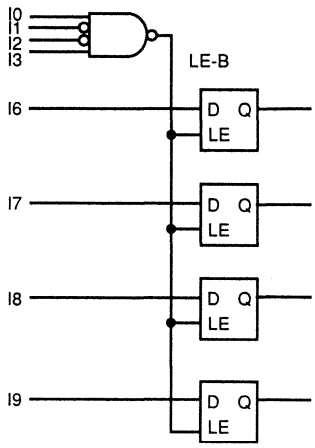


Node names are assigned in the AdET declaration section in a manner similar to pin name assignment. As is evident in the example circuit, multi-level logic is as easy to implement as fixed two-level logic, yet facilitates design of gate array and TTL-type circuits.

Input Latches

To demonstrate the use of the input latches, the Sampler adds input latches to inputs I6..I9. The latch-enable term named LE_B controls the latching, and is set into action via the statement:

LE_B = !(I0 & !I1 & !I2 & I3);



Thus, when I0..I3 are in the 1001 state, LE_B will be LOW and I6..I9 will asynchronously flow through the latches. When they are not in this state, I6..I9 will be latched. LE_B is used, in effect, as a LOW-going write strobe. Such latch constructs are especially useful when a byte or nibble needs to be latched from a data bus. Input latches are also useful in creating pipelined synchronous systems.

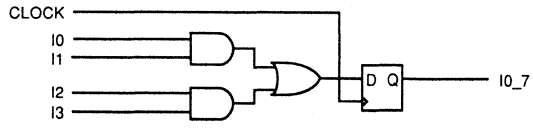
The input latches are defaulted to a fixed non-latching state. They are activated only when the LE terms are defined in the equation section. LE_A, for instance is not defined in the equation section, making I0..13 unlatched by default.

The latches are used as part of the last Sampler circuit, and are diagrammed again in that circuit.

Synchronous Logic

Synchronous logic design using the XL78C800's JK flip-flops is illustrated in three circuits. The first circuit is a registered 2-level logic function, employing an AdET notation identical to that used with conventional registered AND-OR PLDS.

```
IO_7 := (I0 & I1) # (I2 & I3);
```

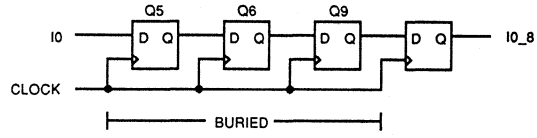


This is the implied synchronous notation of AdET, where the ' := ' operator signifies that IO_7 will be a registered function of the inputs on the right-side of the equation. The design software automatically configures the JK flip-flop as a D type, and sets the I/O Macrocell to the Q-Output configuration.

For reference, all XL78C800 flip-flops are clocked by pin 1 and are positive-edge triggered. They are cleared at power-up, and can be asynchronously cleared thereafter using the CLR_A or CLR_B terms. As with the Latch-Enable terms, the Clear terms are defaulted to a fixed inactive state when not assigned equations.

The second synchronous circuit is a 'buried' 4-bit shift register. It is so named because the flip-flops (except the last stage), are buried within the device, not requiring the use of any pins. Again, simple D flip-flops are used, but in this case, because they are buried, node names are used to identify the first three flip-flops. They are named Q5, Q6 and Q9, with the last stage outputting to the pin named IO_8. Note that because the flip-flop of I/O Macrocell 7 is used in the previous circuit, the shift register goes around that macrocell. Note also that flip-flops Q5..Q9 are cleared only a power-up, since CLR_B is defaulted to the inactive state.

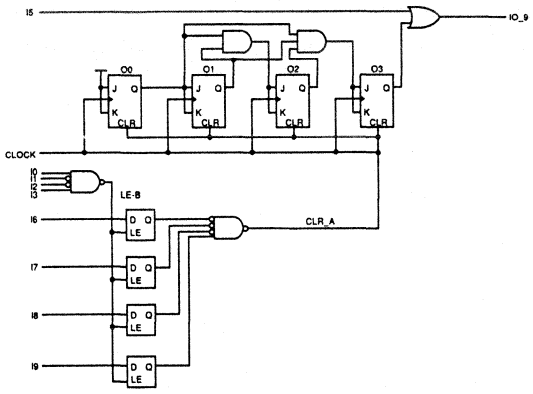
```
Q5 := 10;     "shift register stage 1"
Q6 := Q5;     "shift register stage 2"
Q9 := Q6;     "shift register stage 3"
IO_8 := Q9;   "shift register stage 4, output to pin"
```



The third and final synchronous circuit is a divide-by-16 circuit, featuring a buried 4-bit synchronous up-counter with an asynchronous 'force-HIGH' on the output. This circuit generates a frequency 1/16th that of the system clock (pin 1) on pin 14. The design uses JK flip-flops, which are assigned nodes names Q0 through Q3. The flip-flops are asynchronously cleared at power-up, or when the 4-bit latch of I6..I9 contains the nibble '0001.'

```
[ Q0.J ] := 1;                "counter stage 1"
[ Q0.K ] := 1;
[ Q1.J ] := Q0;               "counter stage 2"
[ Q1.K ] := Q0;
[ Q2.J ] := Q0 & Q1;          "counter stage 3"
[ Q2.K ] := Q0 & Q1;
[ Q3.J ] := Q0 & Q1 & Q2;     "counter stage 4"
[ Q3.K ] := Q0 & Q1 & Q2;
```

```
IO_9 = Q3 # 15;                "OR gate to output pin
Clr_A = !I6 & !I7 & !I8 & I9;
```



The J and K nodes of the flip-flop are identified using the .J and .K suffixes to the node name. Conceptually the JK flip-flop is given a node name, and then the J and K inputs of the flip-flop are individually identified via the suffixes. Even though J and K inputs themselves are not synchronous, AdET syntax requires them to be assigned functions using the ' := ' operator. If the flip-flop node name is given an equation directly (no suffixes), the flip-flop will be implemented as the default D type, as in the previous shift-register circuit.

AdET DESIGN FILE DESCRIPTION

As with any computer language, the AdET language requires certain constructs to occur in certain places. These constructs are highlighted in the ERASIC Sampler AdET design file (Figure 8). At the top are the module statement, a design title, the device name (what the JEDEC file will be called), and the device type. Following that are the pin and node name assignments. Each pin and node is assigned a unique, unchanging number. (Pin and node numbers for the ERASIC XL78C800 are detailed in Figure 7.) These numbers are then used to give the various entities names particular to the user-design. (In the Sampler, for instance, pin 1 is given the name 'Clock,' while node 49 is given the name 'NO.') Thereafter comes the EQUATION section, with the various Sampler circuits described, followed by the keyword END, completing the design.

Additional AdET Techniques

In addition to the equation-oriented design of the Sampler, AdET offers high-level constructs such as truth tables and state machines. With these constructs, only the 'what' of the design need be described, with the 'how' left to the software. High-level constructs allow logic functions to be treated as black boxes, with the derivation of the boxes' internal gate-level implementations left to AdET. The ERASIC XL78C800 fully supports all AdET high-level constructs. Additionally, it enhances the usefulness of such constructs, since it allows more of them to be placed on the same PLD, and lets them be interconnected in ways not before possible. More information on using high-level AdET design techniques is contained in the AdET manual.

Flip-Flops

```
Q0,Q1,Q2,Q3,Q4          node    47,45,43,41,39;
Q5,Q6,Q7,Q8,Q9          node    37,35,33,31,29;
```

Asynchronous Feedback Terms

```
AF00,AF01,AF02,AF03     node    49,50,51,52;
AF04,AF05,AF06,AF07     node    53,54,55,56;
AF08,AF09,AF10,AF11     node    57,58,59,60;
AF12,AF13,AF14,AF15     node    61,62,63,64;
AF16,AF17,AF18,AF19     node    65,66,67,68;
AF20,AF21,AF22,AF23     node    69,70,71,72;
AF24,AF25,AF26,AF27     node    73,74,75,76;
AF28,AF29,AF30,AF31     node    77,78,79,80;
```

Control Terms

```
CLR_A,CLR_B             node    27,28;
LE_A,LE_B               node    25,26;
```

Note: Flip-Flops Q0..Q9 are in Macrocells 0..9, respectively. Asynchronous feedback term AF00 is the topmost, AF31 the bottom-most.

FIGURE 7. XL78C800 INTERNAL NODE IDENTIFICATION IN AdET

```
module ERASIC_Sampler;

title 'ERASIC Sampler Design
       Design uses one 78C800 and contains various circuits which
          illustrate ABEL design techniques.

       Erich Goetting
       EXEL Microelectronics, Inc.'

 Sampler device 'XL78C800';

"pin declarations"

        Clock           pin 1;

        I0,I1,I2,I3     pin 2,3,4,5;      "latchable inputs"
        I4,I5           pin 6,7;
        I6,I7,I8,I9     pin 8,9,10,11;    "latchable inputs"

        IO_0, IO_1      pin 23,22;        "input/output pins"
        IO_2, IO_3      pin 21,20;
        IO_4, IO_5      pin 19,18;
        IO_6, IO_7      pin 17,16;
        IO_8, IO_9      pin 15,14;

        !OE             pin 13;           "output enable"

"node declarations"

        00,01,02,03,04    node  47,45,43,41,39;   "flip-flops"
        05,06,07,08,09    node  37,35,33,31,29;

        N0,N1,N2          node 49,50,51;  "for multi-level circuit"
        Clr_A,Clr_B       node 27,28;     "flip-flop clear terms"
        LE_A,LE_B         node 25,26;     "latch enable terms"


equations

"one-level circuits"

  IO_0 =   I0 & I1 & I2 & I3 ;   "AND"

  IO_1 = !(I0 & I1 & I2 & I3);   "NAND"

  IO_2 =   I0 # I1 # I2 # I3 ;   "OR"

  IO_3 = !(I0 # I1 # I2 # I3);   "NOR"

"two-level circuits"

  IO_4 = (I0 & I1) # (I2 & I3);  "Sum-of-Products"

  IO_5 = I0 $ I1;                "XOR"
  Enable IO_5 = OE;              "make XOR output three-state

"multi-level circuit"

    N0 = (I0 & I1) # (I2 & !I3);    "SR latch Set Function"
    N1 = !(N0 # N2);                "SR latch NOR gate 1"
    N2 = !(I4 # N1);                "SR latch NOR gate 2"
  IO_6 = I5 & N2;                   "output AND function"

"input latches"

   LE_B = !(I0 & !I1 & (I2 & I3);


"synchronous circuits"

  "registered 2-level function"

  IO_7 := (I0 & I1) # (I2 & I3);

  "buried 4-bit shift register"

  05    := I0;                  " shift register stage 1"
  06    := 05;                  " shift register stage 2"
  09    := 06;                  " shift register stage 3"
  IO_8 := 09;                   " shift register stage 4, output to pin"

  "divide-by-16 circuit"

  [00.J] := 1;                  "counter stage 1"
  [00.K] := 1;
  [01.J] := 00;                 "counter stage 2"
  [01.K] := 00;
  [02.J] := 00 & 01;            "counter stage 3"
  [02.K] := 00 & 01;
  [03.J] := 00 & 01 & 02;       "counter stage 4"
  [03.K] := 00 & 01 & 02;

  IO_9    = 03 # I5;            "OR gate to output pin"
  Clr_A   = !I6 & !I7 & !I8 & I9;

end
```

FIGURE 8. ERASIC SAMPLER AdET DESIGN FILE

XL78C800 PROGRAMMING

The XL78C800's CMOS E^2PROM technology provides the highest level of PLD programming features currently available. Electrically-erasable technology offers 100% testability and high-speed reprogrammability in plastic packages. As a result, users can perform a single incoming test procedure on these devices, regardless of their final logic configuration.

The XL78C800 employs a special ruggedized E^2PROM cell configuration, allowing it to be reprogrammed a minimum of 10,000 times, with a logic retention period of 10 years.

The XL78C800 can be erased, programmed, and verified in less than five seconds. Since all pins are used for logic functions, the XL78C800 uses the presence of V_{PP} on pin 6 (PMODE) to place the device into programming mode. Once in this mode, erase, programming, and verify operations are controlled via standard TTL-level signals.

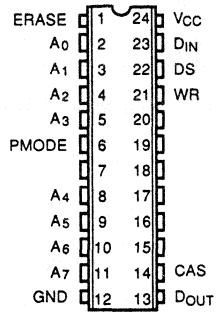


FIGURE 9. XL78C800 PIN CONFIGURATION IN PROGRAMMING MODE

PLD 5 P'DCTS

PROGRAMMING MODE PIN FUNCTIONALITY

Name	Type	Pin(s)	Description
PMODE	I	6	Programming Mode. Raising this input to V_{PP} volts places the device in the programming mode, thereby activating the pin functionality described below. If this input is below 6.0 volts, the device is in the logic mode.
A0..A3 A4..A7	I I	2..5 8..11	Address Inputs. Addresses used to select both the column and row address of all programmable cells.
CAS	I	14	Column Address Strobe. When asserted, this pin latches the current A0-A7 values into the Column Address Register, thereby selecting the column to be programmed or read. It must be asserted for the duration of any operation requiring a specific column address. When negated, CAS causes the output of the Column Address Register to asynchronously follow the A0-A7 values.
DS	I	22	Data Strobe. A LOW-HIGH-LOW transition of this pin latches the value of the Din pin into the Row Data Latch whose address is concurrently specified on A0-A7.
Din	I	23	Data Input. Data input for device programming.
Dout	0	13	Data Output. Data output for device programming verification. Valid except when WR is asserted.
ERASE	I	1	Write mode select and data latch clear. This pin has two functions. The first function is to condition the operation of the WR pin. If this pin is HIGH while WR is asserted, the chip will be unconditionally erased. If this pin is LOW while the WR pin is asserted, the data stored in the 66 Data Latches is written into the currently specified column. The second function is to clear the data latches. Whenever this pin is brought HIGH all 66 data latches will be cleared to the logic "0" state.
WR	I	21	Write. A LOW-HIGH-LOW pulse on this input causes the E^2 cells to be written, as conditioned by the state of the ERASE pin,
Vcc	I	24	+5V Power Supply. Vcc must be supplied during programming mode.
GND	I	12	Signal and Power Ground.

XL78C800 PROGRAMMING-MODE ARCHITECTURE

Referring to Figure 10, the primary programming-mode feature of the XL78C800 is the E^2 cell array. This single array stores all information defining the logic configuration of the device. The array is organized as a matrix of 66 rows by 162 columns. The 66 rows correspond to the 66 Terms in the array. The 162 columns are comprised of the 96 array input lines of the logic diagram, the architecture column, and 65 hidden 'don't care' columns. The 'don't care' columns do not appear in the logic diagram.

The address inputs, A_0-A_7, are used to specify the unique Column-Row address pair of each E^2 cell. Cells are accessed on a column-major basis. The Column Address is applied first and latched into the Column Address Register via the CAS input. The Column Address Register, in turn, selects one of the 162 columns via the Column Decoder. Following Column Address latching, Row Addresses applied to A_0-A_7 will asynchronously select E^2 cell addresses within the selected column.

Writing to the E^2 cells of a particular column is accomplished by first latching the Column Address, then strobing data into the 66 Data Latches, and then transferring the data values to the E^2 cells in the column. The Data Latches store a single bit for each of the 66-rows. Before writing new data, the Data Latches must be cleared by strobing the ERASE input. This action sets all latches to a logic "0." Each latch is written by applying the data to the Din input, applying its Row Address to A_0-A_7 and strobing the DS input. The Data Latches can be written in any order. Data Latches not written will default to a "0." Once a Data Latch is set to a "1," it can only be reset to a "0" via the ERASE strobe. When all 66 latches contain the desired data, the data is written to the E^2 cells of the selected column by pulsing the WR pin while holding ERASE at a logic "0." Columns having identical logic values for all 66 Data Latches may be written without re-entering the Data Latch values.

The 65 'don't care' columns are programmed with the NAND of the corresponding input columns, as defined in the Input Address section. A row in a don't care column is programmed to a "0" if all corresponding inputs are programmed to a "1," the logical don't care state.

Reading of the array is accomplished in a manner similar to writing. First, the ERASE pin must be strobed HIGH to enable readout. The column address is then applied and latched. Thereafter, the state of any E^2 cell within the selected column is presented asynchronously on the Dout pin.

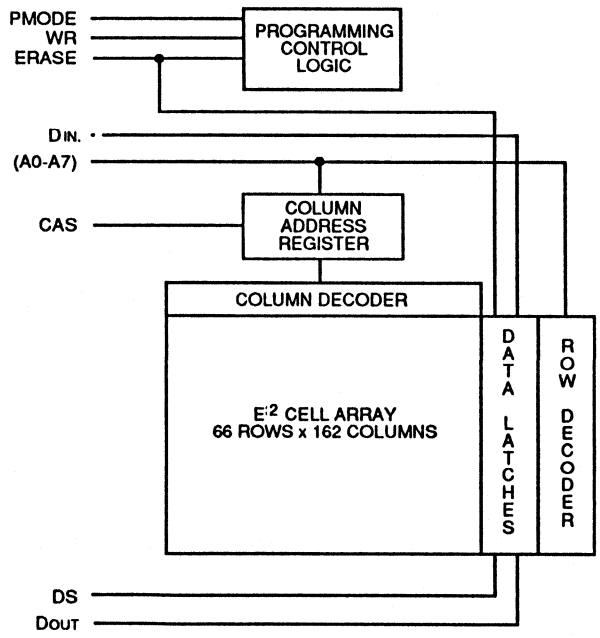


FIGURE 10. XL78C800 PROGRAMMING ARCHITECTURE

XL78C800 EE-FUSE ADDRESSES

Input Addresses

Input Name -> Column Address (HEX)

CLK	$3C	I5	$CD	AF0	$40	AF16	$8A
CLK*	$3D	I5*	$CE	AF0—	$41	AF16—	$8B
CLK—	$3E	I5—	$CF	AF1	$3A	AF17	$88
		i5	$83	AF1—	$3B	AF17—	$89
I0	$3F	i5*	$86	AF2	$38	AF18	$84
I0*	$42	i5—	$87	AF2—	$39	AF18—	$85
I0—	$43	Q5	$80	AF3	$34	AF19	$96
i0	$33	Q5*	$81	AF3—	$35	AF19—	$97
i0*	$36	Q5—	$82	AF4	$2E	AF20	$94
i0—	$37	I6	$C8	AF4—	$2F	AF20—	$95
Q0	$30	I6'	$C9	AF5	$2C	AF21	$90
Q0*	$31	I6—	$CC	AF5—	$2D	AF21 —	$91
Q0—	$32	i6	$8F	AF6	$28	AF22	$A2
I1	$44	i6*	$92	AF6—	$29	AF22—	$A3
I1*	$45	i6—	$93	AF7	$22	AF23	$AO
I1—	$46	Q6	$8C	AF7—	$23	AF23—	$A1
i1	$27	Q6'	$8D	AF8	$20	AF24	$9C
i1*	$2A	Q6—	$8E	AF8—	$21	AF24—	$9D
i1—	$2B	I7	$C7	AF9	$1C	AF25	$AE
Q1	$24	I7'	$CA	AF9—	$1D	AF25—	$AF
Q1*	$25	I7—	$CB	AFI0	$16	AF26	$AC
Q1—	$26	i7	$9B	AF10—	$17	AF26—	$AD
I2	$47	i7*	$9E	AF11	$14	AF27	$A8
I2*	$4A	i7—	$9F	AF11—	$15	AF27—	$A9
I2—	$4B	Q7	$98	AF12	$10	AF28	$BA
i2	$1B	Q7'	$99	AF12—	$11	AF28—	$BB
i2*	$1E	Q7—	$9A	AF13 .	$0A	AF29	$B8
i2—	$1F	I8	$C4	AF13—	$0B	AF29—	$B9
Q2	$18	I8'	$C5	AF14	$08	AF30	$B4
Q2*	$19	I8—	$C6	AF14—	$09	AF30—	$B5
Q2—	$1A	i8	$A7	AF15	$04	AF31	$C0
I3	$48	i8*	$AA	AF15—	$05	AF31—	$C1
I3*	$49	i8—	$AB				
I3—	$4C	Q8	$A4			OE	$BD
i3	$0F	Q8*	$A5			$\overline{OE}$	$BC
i3*	$12	Q8—	$A6			OE—	$BE
i3—	$13	I9	$BF				
Q3	$0C	I9*	$C2				
Q3*	$0D	I9—	$C3				
Q3—	$0E	i9	$B3				
I4	$4D	i9,	$B6				
I4*	$4E	i9—	$B7				
I4—	$4F	Q9	$B0				
i4	$03	Q9'	$B1				
i4*	$06	Q9—	$B2				
i4—	$07						
Q4	$00						
Q4*	$01						
Q4—	$02						

Legend: XX is true input, XX* is false input, XX— is don't care input.

Term Addresses

Term Name ->Row Address (HEX)

CLR_A	$1F	O5	$41	AF0	$14	AF17	$3B
LE_A	$20	J5	$2C	AF1	$13	AF18	$3A
O0	$04	K5	$2B	AF2	$12	AF19	$39
J0	$1D	O6	$40	AF3	$11	AF20	$38
K0	$1E	J6	$2A	AF4	$10	AF21	$37
O1	$03	K6	$29	AF5	$0F	AF22	$36
J1	$1B	O7	$3F	AF6	$0E	AF23	$35
K1	$1C	J7	$28	AF7	$0D	AF24	$34
O2	$02	K7	$27	AF8	$0C	AF25	$33
J2	$19	O8	$3E	AF9	$0B	AF26	$32
K2	$1A	J8	$26	AF10	$0A	AF27	$31
O3	$01	K8	$25	AF11	$09	AF28	$30
J3	$17	O9	$3D	AF12	$08	AF29	$2F
K3	$18	J9	$24	AF13	$07	AF30	$2E
O4	$00	K9	$23	AF14	$06	AF31	$2D
J4	$15	LE_B	$21	AF1 5	$05		
K4	$16	CLR_B	$22	AF16	$3C		

ARCHITECTURE FUSE ADDRESSES

All Architecture Information is accessed via Columns $D0 and $D1, with $D0 containing the TRUE information and $D1 containing the complement information. The row addresses of the architecture and polarity bits within these columns are given below.

O,J,K Polarity,	C2,C1,C0 for Mcell 0	$04,$1D,$IE,	$13,$12,$11
O,J,K Polarity,	C2,C1,C0 for Mcell 1	$03,$1B,$1C,	$10,$0F,$0E
O,J,K Polarity,	C2,C1,C0 for Mcell 2	$02,$19,$1A,	$0D,$0C,$0B
O,J,K Polarity,	C2,C1,C0 for Mcell 3	$01,$17,$18,	$0A,$09,$08
O,J,K Polarity,	C2,C1,C0 for Mcell 4	$00,$15,$16,	$07,$06,$05
O,J,K Polarity,	C2,C1,C0 for Mcell 5	$41,$2C,$2B,	$3C,$3B,$3A
O,J,K Polarity,	C2,C1,C0 for Mcell 6	$40,$2A,$29,	$39,$38,$37
O,J,K Polarity,	C2,C1,C0 for Mcell 7	$3F,$28,$27,	$36,$35,$34
O,J,K Polarity,	C2,C1,C0 for Mcell 8	$3E,$26,$25,	$33,$32,$31
O,J,K Polarity,	C2,C1,C0 for Mcell 9	$3D,$24,$23,	$30,$2F,$2E
CLR_A,CLR_B,	LE_A,LE_B	$1F,$22,	$20,$21
Security Fuse	$2D (column $00 only)		

Note:

[1] No E^2 Cells are present at the following silicon addresses, and therefore these addresses will always read as a "1":

1. Column: D0 Row: 14
2. Column: D1 Row: 14
3. Column: D1 Row: 2D

PROGRAMMING PROCEDURES

Programming and verification of the XL78C800 can be accomplished using the following procedures:

1. Enter Programming Mode
2. Chip Erase
3. Chip-Erase Verify
4. Column Write
5. Column Read (verification)
6. Exit Programming Mode

All procedures except 'Enter Programming Mode' must be performed while in Programming Mode. All Programming Mode control inputs (i.e. ERASE, CAS, DS, and WR) are defaulted to a negated state (OV) unless otherwise stated. The term 'strobe' is used to signify a negated-asserted-negated transition of a pin which is in the negated state. Unless otherwise stated, strobe is 10 microseconds in duration.

Enter Programming Mode

The chip is put into programming mode as follows:

1. Vcc = 4.75 to 5.25V
2. Delay = t_{PMD}
3. PMODE = V_{PP}
4. Delay = t_{CPD}

Chip Erase

Before the chip can be programmed with a new logic configuration, it must be erased to return all E^2 cells to their unprogrammed state. The chip is erased as follows:

1. ERASE = V_{IH}
2. Strobe WR for 1/2*t_{WRE}
3. Exit Programming Mode
4. Delay t_{REC}
5. Enter Programming Mode
6. ERASE = V_{IH}
7. Strobe WR for 1/2*t_{WRE}

Chip-Erase Verify

The All-Ones condition of an erased XL78C800 may be verified as follows:

1. Set address [A7:AO] = FF (hex)
2. Strobe Erase
3. Delay t_{DED}
4. If D_{OUT} = V_{IH}, then device is erased

Column Write

The Erasic device is programmed by a sequence of write operations. All columns must be correctly programmed for the device to function correctly. Each of the 162 columns in the device is written as follows:

1. Set address [A7: A0] = Column Address
2. Assert CAS to latch address into Column Address Register
3. Strobe ERASE for t_{YLSW} to clear Data Latches —this may be done concurrently with Step 2.
4. For each Row from 00 (hex) to 41 (hex):
   a. Set address [A7:A0] = Row Address
   b. Din = Data
   c. Strobe DS to latch data
5. Strobe WR for t_{WRW}
6. Delay t_{REC}
7. Negate CAS

Column Read

Programming of the device should be verified to assure proper device operation. All columns must be programmed before verification. Each of the 162 columns in the chip is verified as follows:

1. Set address [A7:A0] = Column Address
2. Assert CAS to latch address into Column Address Register
3. Strobe ERASE
4. For each row from 00 (hex) to 41 (hex):
   a Set address [A7:A0] = Row Address
   b. Delay t_{DD}
   c. Read D_{OUT}
   d. Verify if D_{OUT} = Data

Exit Programming Mode

Following Chip Erase, Chip Programming and Verifi- cation, the chip must be powered down in the following sequence.

1. ALL Control and Address pins brought to 0V This excludes PMODE, Vcc and $\overline{OE}$ (see Note)
2. PMODE = 0V
3. Delay t_{PMS}
4. $\overline{OE}$, Vcc = 0V

At all subsequent power-ups, all logic, architecture and security features will be activated.

NOTE: When PMODE is made inactive, the I/O Macrocells will again drive the pins in accordance with the configuration present at power up. In accordance with the programming procedures specified here, this will be the completely erased configuration, in which all I/O's will be in the 3-state output mode controlled by the $\overline{OE}$ pin.

Logic contention should be avoided at the D_{IN}, D_S, WR, and CAS during the period after which PMODE has been deactivated and Vcc is still active.

XL78C800 JEDEC FILE INFORMATION

Figure 11 illustrates a sample JEDEC Fuse Map for XL78C800. Each row in the Fuse Map corresponds to a Term in the logic diagram. The first 66 rows correspond to the main NOR array, with each row representing a Term. The total number of fuses in this section is 66 x 96 = 6336 fuses, with JEDEC addresses ranging from 0000 to 6335.

The 65 Architecture Fuses begin at fuse number 6336. Each I/O Macrocell is described by 6 Architecture Fuses (O polarity, J Polarity, K Polarity, C2, C1, and C0). Thereafter, four fuses describe the CLR_A, CLR_B, LE_A and LE_B Polarity control. The optional Security Fuse feature may be described in the "G" field.

L6336	
111011	(O, J, and K Polarity, C2, C1, C0 for I/O Macrocell 0)
:	
:	
001011	(O, J, and K Polarity, C2, C1, C0 for I/O Macrocell 9)
1000*	(CLR_A, CLR_B, LE_A, and LE_B Polarity)
G0*	(Security Enabled)

Architecture Fuse Detail

```
AdBT 1.00 - JEDEC      30-Oct-90 11:54 AM
JEDEC File For: xl78c800

+-----------------------------------------------------+
| Design uses one 78C800 and contains various         |
| circuits which illustrate ABEL design techniques    |
+-----------------------------------------------------+
| Gabriel Jordan, EXEL Microelectronics               |
+-----------------------------------------------------+ *
QP24*      N Number of pins*
QP6400*    N Number of fuses*

N Fuse  RAM  Data*

L0000 11111111111111111111111111111111111111111111101111101111011111011111111111111111111111111111111111*
L0096 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0192 11101111101111101111101111111111111111111111111111111111111111111111111111111111111111111111111111*
L0288 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0384 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0480 11101111101111101111101111111111111111111111111111111111111111111111111111111111111111111111111111*
L0576 11111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0672 11111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0768 11011110111110111111011111111111111111111111111111111111111111111111111111111111111111111111111111*
L0864 11111110111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L0960 11111110111101111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1056 11011111011111011111011111111111111111111111111111111111111111111111111111111111111111111111111111*
L1152 11111110111110111101111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1248 11111110111110111101111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1344 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111001111*
L1440 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1536 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1632 11111111111111111111111111111111111111111111101111101111111111111111111111111111111111111111111111*
L1728 11011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1824 11011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L1920 11111111111111111111111111111111011111101111111111111111111111111111111111111111111111111111110111*
L2016 11111111111111111111111111111111111101111111111111111111111111111111111111111111111111111111111111*
L2112 11111111111111111111111111111111111011111111111111111111111111111111111111111111111111111111111111*
L2208 11101111011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2304 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111001111*
L2400 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111001111*
L2496 11011111011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2592 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2688 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L2784 11111111111111111111111101111110111111111111111111111111111111111111111111111111111111111111111111*
L2880 11111111111111111111111111111111111111111111111101111111111111111111111111111111111111111111111111*
L2976 11111111111111111111111111111111111111111111111011111111111111111111111111111111111111111111111111*
L3072 11101111011111011111101111111111111111111111111111111111111111111111111111111111111111111111111111*
L3168 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3264 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3360 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3456 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3552 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3648 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3744 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3840 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L3936 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4032 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4128 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4224 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4320 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4416 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4512 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4608 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4704 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4800 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4896 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L4992 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5088 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5184 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5280 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5376 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5472 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5568 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5664 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5760 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5856 11101111011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111*
L5952 11111111111111101111101111111111111111111111111111111111111111111111111111111111111111111111111111*
L6048 11111111111111111111111101111111111111111111111111111111111111111111111111111111111111111111110111*
L6144 11111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111101010111*
L6240 11111111111111101111011111111111111111111111111111111111111111111111111111111111111111111111111111*
L6336 111011*
L6342 000011*
L6348 011011*
L6354 111011*
L6360 000011*
L6366 001111*
L6372 101011*
L6378 101010*
L6384 101010*
L6390 001011*
L6396 1000*
CDF64*
A0B2
```

FIGURE 11. SAMPLE JEDEC FUSE MAP

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Ambient Temperature Under Bias .....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Voltage on Any Pin (Except Pins 1, 6)* (Note 2) .....-0.5V to +7.0V
Programming Mode Pin Voltage (Pin 6)* .....-0.5V to +21.25V
Preload Voltage (Pin 1)* .....-0.5V to +13.0V
DC Output Current 50mA
*With respect to ground

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Notes 3, 8, 10)

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Condition	Device Grades	Limits			Unit
				Min.	Typ.	Max.	
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		Vcc	V
I_{OL}	Output Low Current	V_{OL} = 0.5V		12	16		mA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-8		mA
I_{OH}	Input Leakage Current-High	V_{IN} = V_{CC}				10	µA
I_{IL}	Input Leakage Current-Low	V_{IN} = 0V				-10	µA
I_{LO}	Output Leakage Current, 3-state	V_O = 0 to V_{CC}		-10		10	µA
I_{CC}	Power Supply Current	V_{IN} < 0.2V or V_{IN} > (V_{CC}-0.2V) f_{CLK} = 0 Hz to 10MHz	-35, -45		17 15	35 30	mA mA
V_{PP}	Programming Mode Voltage on PMode	(Pin 6)		20.75	21	21.25	V
I_{PP}	Programming Supply Current					1.0	mA
V_{PL}	Preload Mode Voltage on Pin 1			11	12	13	V
I_{PL}	Preload Supply Current					1.0	mA

CAPACITANCE

Symbol	Parameter	Plastic DIP/PLCC Package			Ceramic Side Brazed Package			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
C_{IN}	Input Pin Capacitance		4	6		5	7	pF
C_{ID}	I/O Pin Capacitance		4	6		5	7	pF
C_{CLK}	Clock Pin Capacitance		5	7		6	8	pF

AC ELECTRICAL CHARACTERISTICS-LOGIC MODE (Notes 4, 5, 6)

Symbol	Parameter	XL78C800-35 LIMITS Min.	Typ.	Max.	Unit
AGGREGATE TIMINGS					
tPD1L	Input Pad to Output Pad Delay, One Level Asynchronous (tPDI + tPDT + tPDO)			35	ns
tPD2L	Input Pad to Output Pad Delay, Two Level Asynchronous (tPDI + 2*tPDT + tPDO)			55	ns
tOEL	OE* Pin LOW to Output LOW-Z			15	ns
tOEH	OE* Pin HIGH to Output HIGH-Z			15	ns
tPDQP	CLK Input Pad to Q Output at I/O Pad (tPDQ + tPDO)			25	ns
tCKL	Clock LOW Time	20			ns
tCKH	Clock HIGH Time	20			ns
tCKRF	Clock Rise and Fall Time			5	ns
tCKP1	Clock Period (1 Level State Machine)	50			ns
tCLK1	Clock Frequency (1 Level State Machine)			20.0	ns
tCKP2	Clock Period (2 Level State Machine)	70			ns
tCLK2	Clock Frequency (2 Level State Machine)			14.2	ns
COMPONENT TIMINGS					
Input Timing					
tPDI	Input Buffer or Transparent Latch (LE negated) Delay			5	ns
tIS	Latch Input Set-up Time to LE Term Asserted			5	ns
tIH	Latch Input Hold Time from LE Term Asserted			0	ns
Term Timing					
tPDT	Term Input to Output Delay			20	ns
I/O Macrocell Timing					
tPDIO	Input Buffer Delay			5	ns
tPDO	Output Buffer Delay			10	ns
tJKS	J and K Input Set-up Time to Clock Pin HIGH			5	ns
tJKH	J and K Input Hold Time from Clock Pin HIGH	0			ns
tPDQ	Q Output Delay from Clock Pin HIGH			15	ns
tPDR	CLR Term Asserted to Q=O Delay			5	ns
tRR	CLR Term Negated Before Clock Pin HIGH			5	ns
tCLR	Clear Term Pulse Width (Note 9)	20			ns
Register Preload Timing					
tPLCKH	Preload Clock (Clock = VPL) HIGH Time	100			ns
tPLZ	Preload Clock HIGH to Outputs in HIGH-Z			50	ns
tPLS	Preload Data on I/O Pin Set-up Time to Clock HIGH	20			ns
tPLH	Preload Data on I/O Pin Hold Time from Clock HIGH	5		15	ns
Power-up Timing (Note 7)					
tINIT	Power-up Initialization Time			5	ms

AC ELECTRICAL CHARACTERISTICS-PROGRAMMING MODE (Note 8)

Symbol	Parameter	XL78C800 LIMITS Min.	Typ.	Max.	Unit
Program Mode Access					
t_{PMD}	V_{CC} Active to PMODE Active	5			ms
t_{CPD}	PMODE Active to any Control Pin Active	5			ms
t_{REC}	WR LOW to Any Input Change	1			ms
t_{CPS}	Control Pin Deactive to PMODE Deactive	1			ms
t_{PMS}	PMODE Deactive to V_{CC} Deactive	1			ms
Chip Erase					
t_{EWS}	ERASE Set-up Time to WR Rising Edge	200			ns
t_{DED}	Chip Erase Verify to Output Valid			200	ns
t_{WRE}	WR Pulse Width for Chip Erase	100			ms
t_{REC}	WR LOW to Any Input Change	1			ms
Row Data Latch Write Sequence					
t_{YLSW}	ERASE Pulse Width for Clearing Data Latches	100			ns
t_{EDS}	ERASE LOW to DS HIGH	100			ns
t_{AS}	Row Address Set-up Time to DS Rising Edge	100			ns
t_{AH}	Row Address Hold Time from DS Falling Edge	100			ns
t_{DIS}	D_{IN} Set-up Time to DS Pulse Rising Edge	100			ns
t_{DIH}	D_{IN} Hold Time from DS Pulse Falling Edge	100			ns
t_{DSW}	DS Pulse Width	100			ns
Column Write Cycle					
t_{CAS}	Column Address Set-up Time to CAS Rising Edge	100			ns
t_{CWS}	CAS Set-up Time to WR Rising Edge	100			ns
t_{WRW}	WR Pulse Width for Program	10			ms
t_{REC}	WR LOW to Any Input Change	1			ms
Column Read Sequence					
t_{DD}	Data Output Valid from Row Address			200	ns
Power-up Timing					
t_{INIT}	Power-up Init Time			5	ms

NOTES:

1. Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the Electrical Characteristics section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltage larger than the rated maxima.

3. All voltages are referenced to ground (GND). Parameters are valid over the specified temperature and operating supply ranges. Typical values are at 25°C, typical supply voltage and typical processing parameters.

4. The Aggregate Timing data specifies input pad to output pad delay paths for common end-user designs. Timing is characterized independently for the Input, Term, and I/O Macrocell circuits to allow the timing characteristics of arbitrary user-circuits to be ascertained. Because of the internal nature of these circuits, their propagation delays are not directly tested, but are guaranteed via pad-to-pad delay testing methodologies.

5. For AC testing, input signal levels are 0.0V and 3.0V with a transition time of 6ns maximum. All time measurements are referenced at input and output voltages of 1.5V.

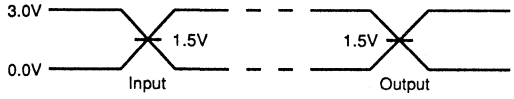
6. Delay times specified include delays through inverters, programmable inverters and multiplexers where appropriate.

7. Initialization occurs automatically at device power-up. Proper initialization requires a monotonic rise of Vcc from a voltage of 0.25V or less to the specified minimum V_{CC} voltage. Power-up initialization Time (t_{INIT}) is with respect to the point at which V_{CC} first reaches the specified minimum voltage. During the initialization period, all outputs are unconditionally placed in a high impedance state and logic operation is suspended. Once initialized, the chip will not reinitialize for V_{CC} of 3V or greater.

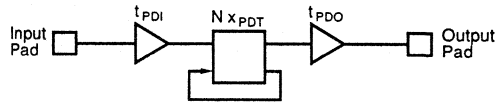
8. Programming mode voltage on PMODE Pin (6) = V_{PP}. Programming parameters are valid at temperatures of +5°C to +45°C, and at Vcc levels of 4.75 to 5.25V.

9. Minimum Clear Pulse width is always less than a one-level logic delay. Thus, one-level pulse generators can be used to clear the flip-flops.

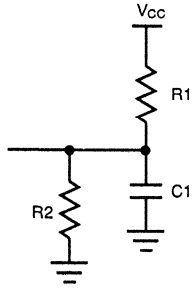
10. Maximum supply current specifications are based on test designs using all 66 terms, with a minimum of 46 terms in the LOW state at all times. Because terms which are unused or are in the HIGH state do not use current, designs which use fewer terms or which have fewer terms simultaneously LOW than the test circuit will have a lower maximum current.



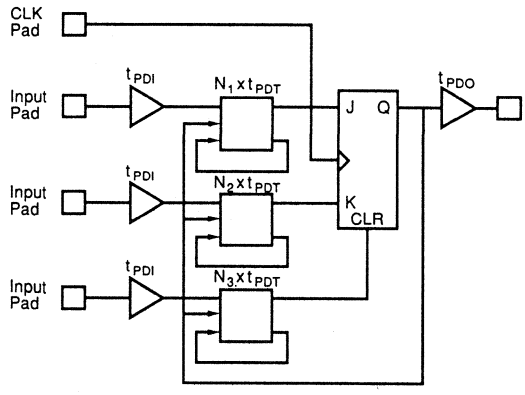
AC TESTING INPUT, OUTPUT WAVEFORM



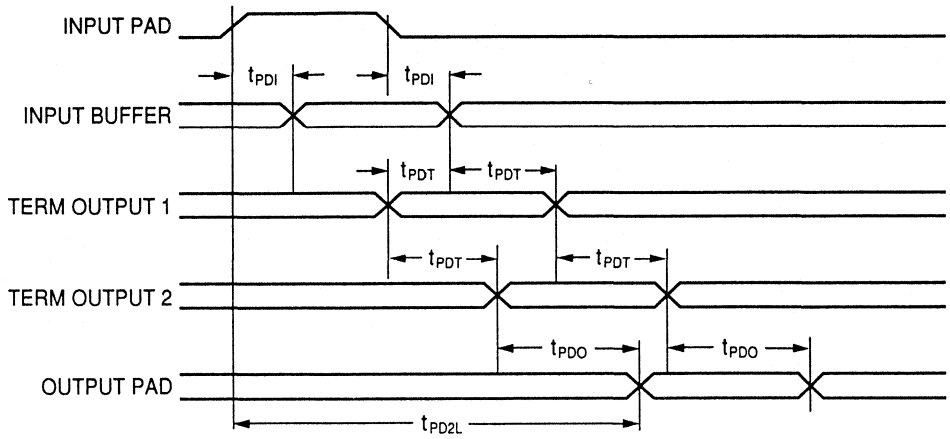
AGGREGATE INPUT PAD TO OUTPUT PAD DELAY MODEL



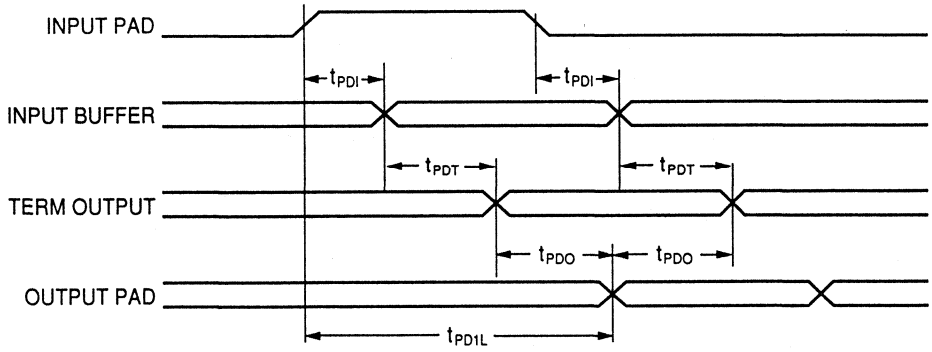
AC TESTING LOAD CIRCUIT



AGGREGATE SYNCHRONOUS DELAY MODEL



AGGREGATE INPUT PAD TO OUTPUT PAD TIMING (2-LEVEL ASYNCH)



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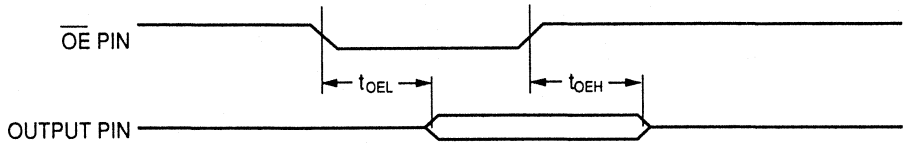
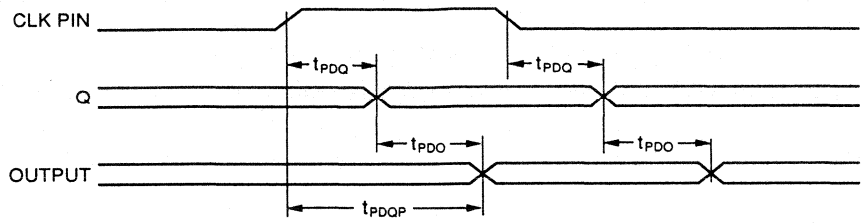
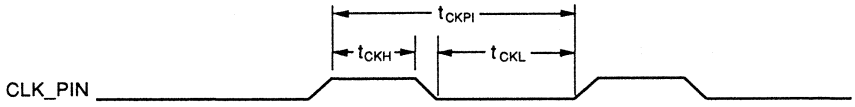


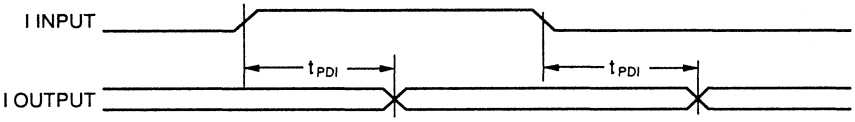
OUTPUT ENABLE DELAY



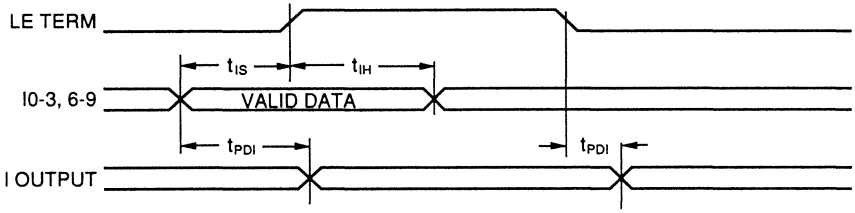
FLIP-FLOP TIMING



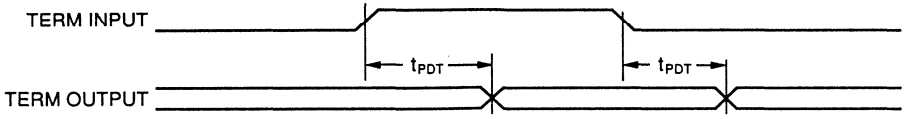
CLOCK TIMING



INPUT DELAY

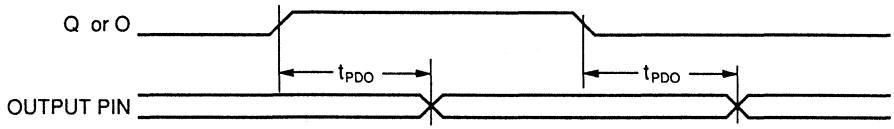


LATCH ENABLE TIMING

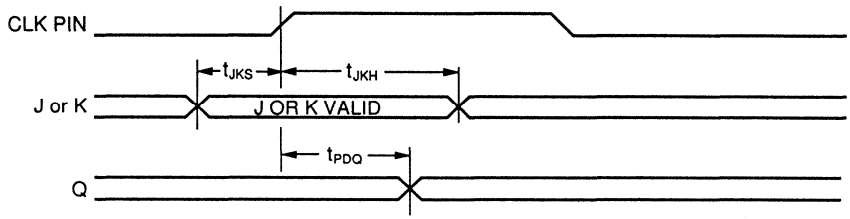


ARRAY DELAY

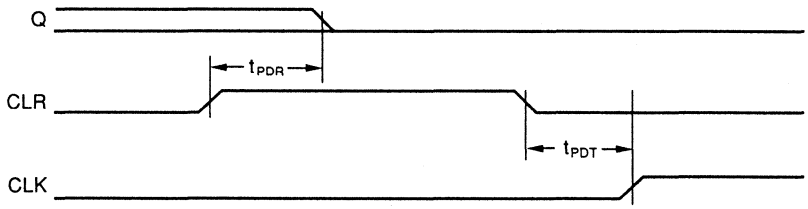
PLD 5 P'DCTS



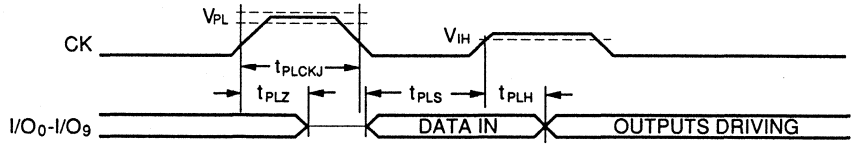
MACROCELL OUT DELAY



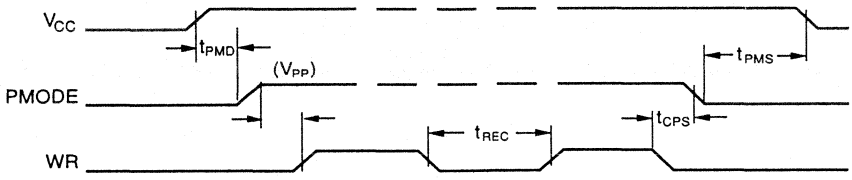
CLOCK IN TO Q OUTPUT TIMING



FLIP-FLOP RESET TIMING

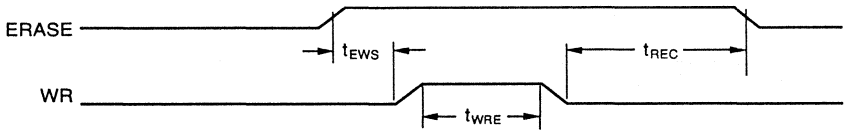


PRELOAD TIMING

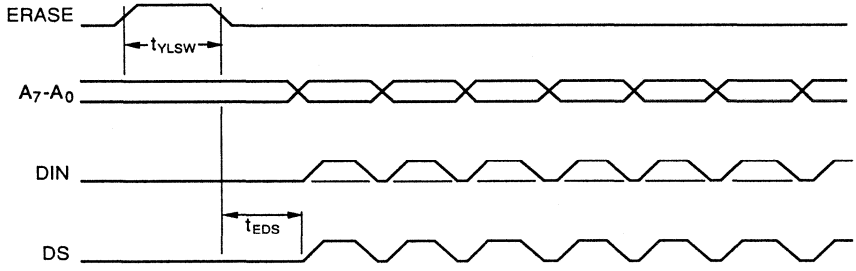


(Note: All subsequent programming timelines assume PMODE is at VPP

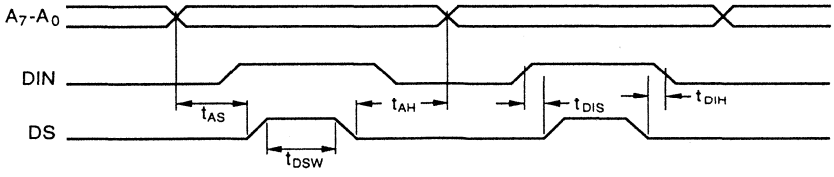
PROGRAM MODE ACCESS



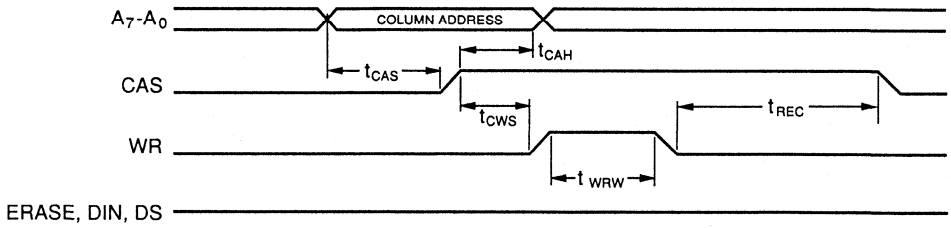
CHIP ERASE



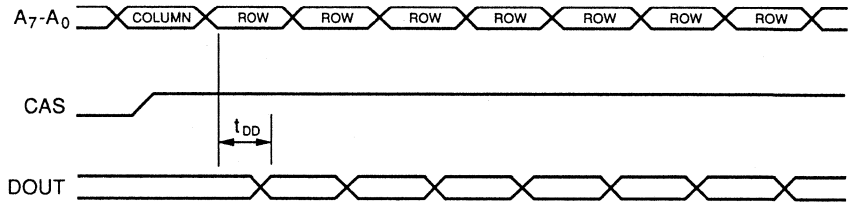
ROW DATA LATCH WRITE SEQUENCE



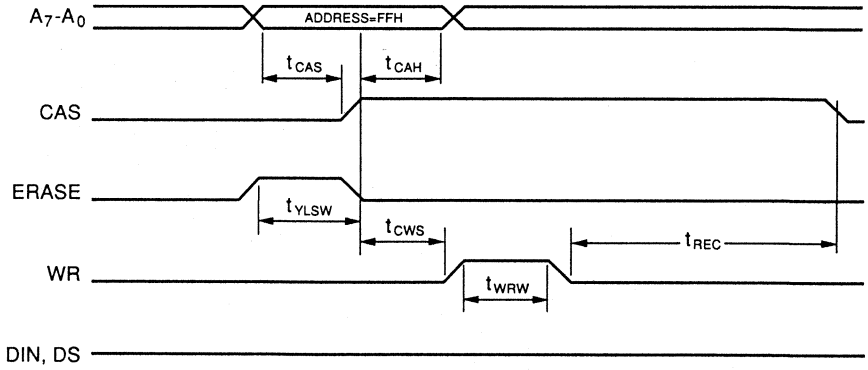
EXPANDED ROW DATA LATCH WRITE SEQUENCE



COLUMN WRITE CYCLE (NONVOLATILE WRITE)



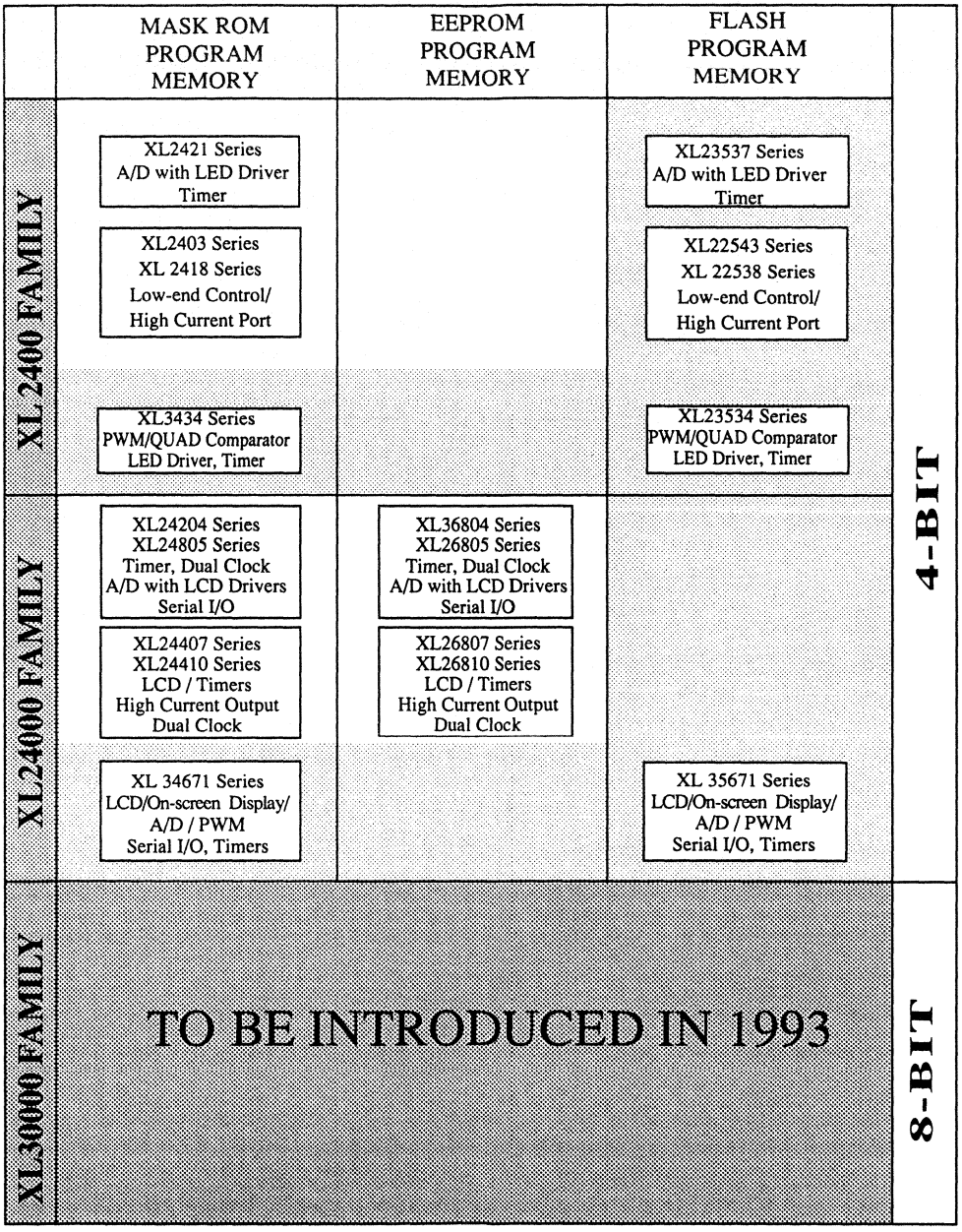
COLUMN READ SEQUENCE



CHIP PROGRAM (ALL E^2 CELLS SET TO Lo Vt)

SECTION 6 Table of Contents

PRODUCT LINE OVERVIEW



Shaded area under development

XL2400 FAMILY

Device Series	Package	3V	5V	FLASH
XL2403 Series	SOP18	XL2403/43/63	XL3403/43/63	XL22543
	DIP18	XL2404/44/64	XL3404/44/64	XL22544
	SDIP18	XL2402/45/65	XL3402/45/65	XL23545
	SOP16	XL2428/46/66	XL3428/46/66	NA
XL2418 Series	SOP22	XL2418/38/58	XL3418/38/58	XL22538
	DIP22	XL2419/39/59	XL3419/39/59	XL22539
	SDIP22	XL2422/40/60	XL3422/40/60	XL22540
	SOP20	XL2430/41/61	XL3430/41/61	XL22541
	DIP20	XL2431/42/62	XL3431/42/62	XL22542
XL2421 Series	SDIP32	NA	XL3437	
	QFP32	NA	XL3447	
				XL23537
				XL23547
XL3434 Series	SOP24	NA	XL3434	XL23534

XL24000 FAMILY

Device Series	VDD	ROM	Package	STANDARD PRODUCTION ROM Version 1.2um	STANDARD PRODUCTION ROM Version 1.0um	SOFTWARE DEVELOPMENT AND PROTOTYPES (5Vonly)	
						MTP Version	FLASH Version
XL24204 Series	2 - 5.5V	2Kx8	QFP64	XL34204	XL34224	-	-
		4Kx8	QFP64	XL34404	XL34424	-	-
		8Kx8	QFP64	NA		XL36804/ XL36824	NA
XL24407 Series	2 - 5.5V	4Kx8	QFP64	XL24407	XL24421	-	-
		8Kx8	QFP64	XL24807	XL24821	XL26807/ XL26821	NA
XL24410 Series	2 - 5.5V	4Kx8	SQFP80	XL24410	XL24422	-	-
		8Kx8	SQFP80	XL24810	XL24822	XL26810/ XL26822	NA
XL24805 Series	2 - 5.5V	8Kx8	SQFP80	XL24805	XL24823	XL26805/ XL26823	-
							NA
XL24870 Series	5V	6Kx8	SDIP42		XL34671	NA	XL35671

Shaded area under development

UICK REFRENCE SUMMARY

	XL2400 FAMILY			XL24000 FAMILY			
DEVICE	XL2403 SERIES	XL2418 SERIES	XL2421 SERIES	XL24204 SERIES	XL24805 SERIES	XL24407 SERIES	XL24410 SERIES
Power Supply	2.0 - 5.5V	2.0 - 5.5V	4.5 - 5.5V	2.0 - 5.5V	2.0 - 5.5V	2.0 - 5.5	2.0 - 5.5V
Standby Power (uA)	<1µA	<1µA	<1µA	<10µA	<10µA	<10µA	<10µA
Oscillator 1	300KHZ - 1MHZ		400KHZ-4.0MHZ	300KHZ-4.5MHZ	300KHZ-2.0MHZ	300KHZ-1.0MHZ	300KHZ-2.0MHZ
Oscillator 2					30-50KHZ	30-50KHZ	30-50KHZ
Instructions	40	43	38	100	100	100	100
Nesting Levels	2	3	3	8	8	8	8
Interrupts	-	-	-	4	6	4	5
HALT Mode Current (Vdd=3.3V)	-	-	-	600µA	30µA	15µA	30µA
Operating Mode Current (Vdd=3.3V)	300µA	300µA	1mA	1mA	4mA	1mA	4mA
ROM	640 x 8	1K x 8	1K x 8	2K x 8/ 4K x 8	8K x 8	4K x 8 8K x 8	4K x 8 8K x 8
RAM	16 x 4	32 x 4	64 x 4	128 x 4/ 256 x 4	256 x 4	128 x 4/ 256 x 4	128 x 4/ 256 x 4
Watch-Dog Timer	YES	YES	YES	YES	YES	YES	YES
Timers with Prescalers	NO	NO	1 x 8 bit	2 x 8 bit	2 x 8 bit	1 x 8 bit / 1 x 10 bit	1 x 8 bit/ 1 x 10 bit
A/D	NO	NO	2 x 8 bit (D/A)	8 x 8 bit	8 x 8 bit	NO	NO
Display	NO	NO	8 x 3 LED	24 x 4 LCD	8 x 3 LCD	28 x 4 LCD	36 x 4 LCD
Serial Interface	NO	NO	NO	YES	YES	NO	YES
MTP Version (Multiple time Programable)	OCT92 (FLASH)	OCT92 (FLASH)	APR93 (FLASH)	YES (EEPROM)	YES (EEPROM)	YES (EEPROM)	YES (EEPROM)

KEY FEATURES

- **Cost effective 4-bit microcontroller**
- **CMOS process for low current drain**
- **12.5μs instruction time (480KHz)**
- **Halt mode for low standby current (1μA)**
- **Low voltage, single power supply**
  - **— VDD = 2.0 ~ 5.5V**
- **640 x 8 bytes ROM / 16 x 4 bytes RAM**
- **Operating frequency: 300KHz~1MHz**
- **40 flexible instructions**
- **2 Subroutine nesting levels**
- **12 I/O pins**
  - **— 4 general purpose input pins**
  - **— 8 general purpose output pins**
- **Multi-input external HALT mode release**
- **Built in carrier generator with selectable frequencies and duties**
- **Programmable delay timer (up to 64 machine cycles)**
- **Built in watchdog timer (WDT)**
- **Form, fit, function emulator**
- **18 or 16-pin SOP, DIP, and SDIP packages**

OVERVIEW

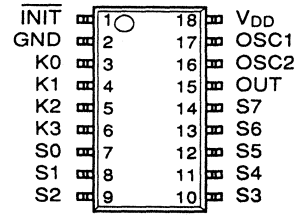
The XL2403 series is a mask-programmable, CMOS microcontroller. Its 4-bit architecture and small package size contribute to system cost reduction. Since few external components are required to operate the device, system costs are minimized. The device consists of an accumulator and two registers, supported with built-in ROM, RAM and a powerful 40-instruction set. Additionally, independent controllable Input and Output ports, a high current output port driver, a Watch-Dog Timer, and a built-in carrier output are available.

APPLICATIONS

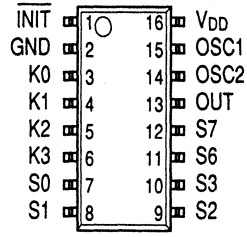
The XL2403 series is ideal for applications where system flexibility and cost-effectiveness are required. The device is ideal for small control systems such as thermostat and temperature controls, automotive cruise control, medical alert or home security systems.

PIN CONFIGURATIONS

18-PIN DIP



16-PIN SOP



KEY FEATURES

- **Cost effective 4-bit microcontroller**
- **CMOS process for low current drain**
- **12.5μs instruction time (480KHz)**
- **Halt mode for low standby current (1μA)**
- **Low voltage, single power supply**
  - **— VDD = 2.0 ~ 5.5V**
- **1024 x 8 bytes ROM / 32 x 4 bytes RAM**
- **Operating frequency: 300KHz~1MHz**
- **43 flexible instructions**
- **3 Subroutine nesting levels**
- **16 I/O pins**
  - **— 4 general purpose input pins**
  - **— 4 general purpose I/O pins**
  - **— 8 general purpose output pins**
- **Multi-input external HALT mode release**
- **Built in carrier generator with selectable frequencies and duties**
- **Programmable delay timer (up to 64 machine cycles)**
- **Built in watchdog timer (WDT)**
- **Form, fit, function emulator**
- **22 or 20-pin SOP, DIP, and SDIP packages**

OVERVIEW

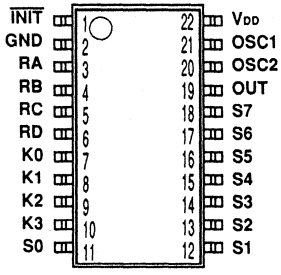
he XL2418 series is a mask-programmable, CMOS microcontroller. Its 4-bit architecture and small package size contribute to system cost reduction. Since few external components are required to operate the device, system costs are minimized. The device consists of an accumulator and two registers, supported with built-in ROM, RAM and a powerful 43-instruction set. Additionally, independent controllable Input and Output ports, a high current output port driver, a Watch-Dog Timer, and a built-in carrier output are available.

APPLICATIONS

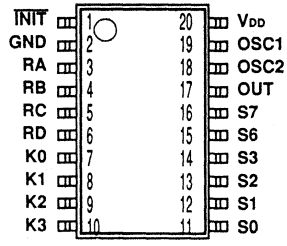
The XL2418 series is ideal for applications where system flexibility and cost-effectiveness are required. The IC was designed for small system control, such as thermostat and temperature controllers, automotive cruise control or a transmitter/encoder for the remote control systems in medical and home security systems.

PIN CONFIGURATION

22-PIN DIP



20-PIN DIP



ASEC 6

KEY FEATURES

- **Cost effective 4-bit microcontroller**
- **CMOS process for low current drain**
- **1.5μs instruction time (4MHz)**
- **Halt mode for low standby current (10μA)**
- **Low voltage, single power supply**
  - **— VDD = 4.5 ~ 5.5V**
- **1024 x 8 bytes ROM / 64 x 4 bytes RAM**
- **Operating frequency: 400KHz~4MHz**
- **8-bit programmable timer with programmable prescaler**
- **38 flexible instructions**
- **3 Subroutine nesting levels**
- **8 I/O pins**
  - **— 4 general purpose input pins**
  - **— 4 general purpose I/O pins**
- **External HALT mode release**
- **2-bit analog reference input**
- **Flexible 8-bit A/D converter**
  - **— may be used as internal D/A**
  - **— with external reference**
  - **— or as a comparator**
- **Built in 8 segment x 3 common LED controller/ driver**
  - **— 6 x 4 display RAM**
  - **— 4 software selectable clock divisions**
- **Built in watchdog timer (WDT)**
- **Form, fit, function emulator**
- **32-pin QFP and SDIP packages**

OVERVIEW

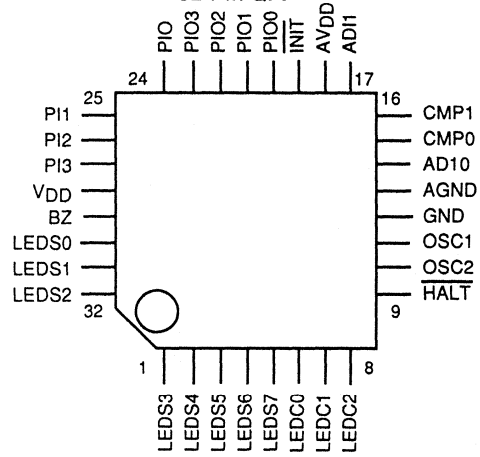
The XL2403 series is a mask-programmable, CMOS microcontroller. Its 4-bit architecture and multiple features makes the device ideal for a wide variety of thermostat and temperature control applications. This low cost IC consists of an 8-bit A/D converter, an 8-bit internal timer, an 8x3 LED controller, a modulated buzzer output, I/O ports, 64 nibbles of RAM and 1K of program ROM.

APPLICATIONS

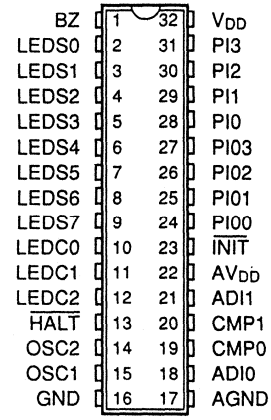
The XL2421 series is a 5V IC suited for many applications. The 8-bit resolution A/D converter is well suited for thermostat and temperature control and voltage monitoring. The LED controller and buzzer outputs make the user interface simple and low cost. System implementation with this single IC reduces system costs, production costs and failure rates.

PIN CONFIGURATIONS

32-Pin QFP



32-Pin SDIP



KEY FEATURES

- Cost effective 4-bit microcontroller
- CMOS process for low current drain
- 1.5μs instruction time (4MHz)
- Two low power modes
  - — Halt mode: 600μA (max)
  - — Stop mode: 10μA (typical)
- Low voltage, single power supply:
  - — VDD=2.0~5.5V
- 2048 x 8 bytes ROM/128 x 4 bytes RAM(XL24204)
- 4096 x 8 bytes ROM/256 x 4 bytes RAM(XL24404)
- Operating frequency: 400KHz - 4.5 MHz
- 8-bit programmable timer with 6 software selectable clock sources
- Four interrupts
  - — 1 external
  - — 3 internal (timer/counter, clock timer, serial I/O)
- 8-bit stack pointer
- 100 flexible instructions
- 8 Subroutine nesting levels
- 10 general purpose I/O pins
- External HALT/STOP mode release
  - — interrupt pin
  - — edge selectable input pin
- Built in 24 segment x 4 common LCD controller/driver
  - — Bias ratio: 1/2, 1/3
  - — Duty ratio: 1/2, 1/3, 1/4
- 8-bit Serial I/O
- 8-channel 8-bit A/D conventer
- Built in watchdog timer (WDT)
- Form, fit, function emulator
- 64-pin SQFP package

OVERVIEW

The XL24204 series is a mask programmable CMOS microcontroller. The device allows system optimization into a single integrated circut by incorporating a wide variety of peripheral functions such as a 24x4 LCD driver, 8-bit serial I/O interface, 8-bit 8-channel A/D, two internal timers, two low power modes, 4-bit I/O ports, internal and external interrupts, and 100 flexible instructions.

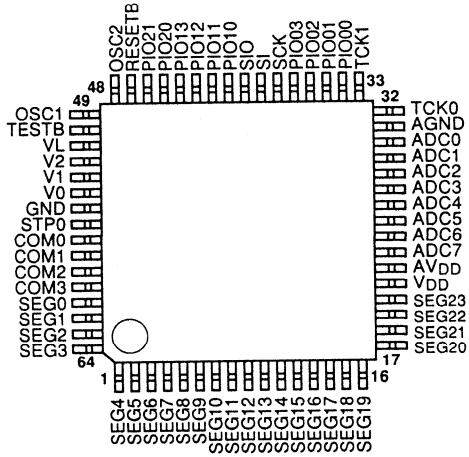
APPLICATION

The XL24204 series is ideal for applications where system flexibility and cost-effectiveness are required. The low V_{CC} operation and the two low power modes are important power saving features. Other features enable real time operations, LCD displays, A/D and serial I/O. The IC was designed for small system control such as thermostat and temperature controllers.

ASEC 6

PIN CONFIGURATION

64-PIN SQFP



KEY FEATURES

- Cost effective 4-bit microcontroller
- CMOS process for low current drain
- 6μs instruction time (1MHz)
- Two low power modes
  - — Halt mode: 10μA (max)
  - — Stop mode: 30μA (typical)
- Low voltage, single power supply:
  - — VDD=2.0~5.5V
- 4096 x 8 bytes ROM/128 x 4 bytes RAM(XL24407)
- 8192 x 8 bytes ROM/256 x 4 bytes RAM(XL24807)
- Dual oscillator
  - — Main clock: 300KHz - 1MHz
  - — Subclock: 30KHz - 50KHz
- 10-bit clock generating timer/counter with prescaler
- 8-bit programmable timer with 6 software selectable clock sources
- Four interrupts
  - — 2 external
  - — 2 internal (timer/counter, clock timer)
- 10-bit stack pointer
- 100 flexible instructions
- 8 Subroutine nesting levels
- 8 input pins
- 10 general purpose I/O pins
- External HALT/STOP mode release
  - — interrupt pin
  - — edge selectable input pin
- Built in 28 segment x 4 common LCD controller/driver
  - — Bias ratio: static, 1/2, 1/3
  - — Duty ratio: 1/2, 1/3, 1/4
- Built in carrier generator, software selectable frequency and duty cycle
  - — fosc/8 @1/2 Duty
  - — fosc/11 @4/11 Duty
  - — fosc/12 @1/2 or 1/3 Duty
- Large current P-channel output port (Ioh=-15A, Voh=2.0V, Vdd=3.0V)
- 8-channel 8-bit A/D conventer
- Built in watchdog timer(WDT)
- Form, fit, function emulator
- 64-pin SQFP package

OVERVIEW

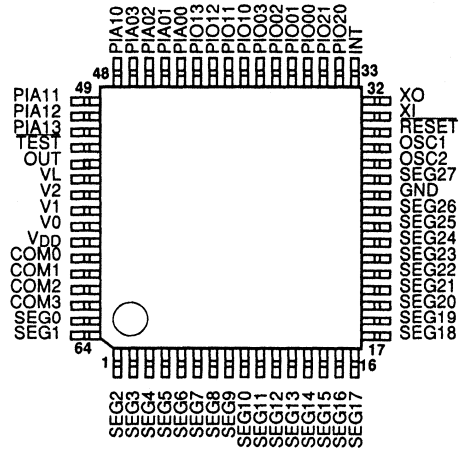
The XL24407 series is a mask programmable CMOS micro-controller. The device allows system optimization into a single IC by incorporating a wide variety of I/O blocks such as a 28x4 LCD driver, a high current modulated output port, dual clock operation, internal timers, two low power modes, 4-bit I/O ports, internal and external interrupts, and 100 flexible instructions.

APPLICATION

The XL24407 series is ideal for applications where system flexibility and cost-effectiveness are required. The low V_{CC} operation and the two low power modes are important power saving features. Other features enable real time operations, LCD displays, and modulated high current output and suit battery-operated applications.

PIN CONFIGURATION

64-PIN SQFP



KEY FEATURES

- Cost effective 4-bit microcontroller
- CMOS process for low current drain
- 3μs instruction time (2MHz)
- Two low power modes
  - — Halt mode: 10μA (max)
  - — Stop mode: 30μA (typical)
- Low voltage, single power supply:
  - — VDD=2.0~5.5V
- 4096 x 8 bytes ROM/256 x 4 bytes RAM(XL24410)
- 8192 x 8 bytes ROM/256 x 4 bytes RAM(XL24810)
- Dual oscillator
  - — Main clock: 300KHz - 2MHz
  - — Subclock: 30KHz - 50KHz
- 10-bit clock generating timer/counter with prescaler
- 8-bit programmable timer with 6 software selectable clock sources
- Five interrupts
  - — 2 external
  - — 3 internal (timer/counter, clock timer, serial I/O)
- 10-bit stack pointer
- 100 flexible instructions
- 8 Subroutine nesting levels
- 16 general purpose I/O pins
- 8-bit Serial I/O
- External HALT/STOP mode release
  - — interrupt pin
  - — edge selectable input pin
- Built in 36 segment x 4 common LCD controller/driver
  - — Bias ratio: 1/2, 1/3
  - — Duty ratio: 1/2, 1/3, 1/4
- Built in carrier generator, software selectable frequency and duty cycle
  - — fosc/8 @1/2 Duty
  - — fosc/11 @4/11 Duty
  - — fosc/12 @1/2 or 1/3 Duty
- Large current P-channel output port (Ioh=-15A, Voh=2.0V, Vdd=3.0V)
- 8-channel 8-bit A/D conventer
- Built in watchdog timer (WDT)
- Form, fit, function emulator
- 80-pin SQFP package

OVERVIEW

The XL24410 series is a mask programmable CMOS microcontroller. The device allows system optimization into a single IC by incorporating a wide variety of I/O blocks such as a 36x4 LCD driver, a high current modulated output port, dual clock operation, internal timers, two low power modes, 4-bit I/O ports, internal and external interrupts and 100 flexible instructions.

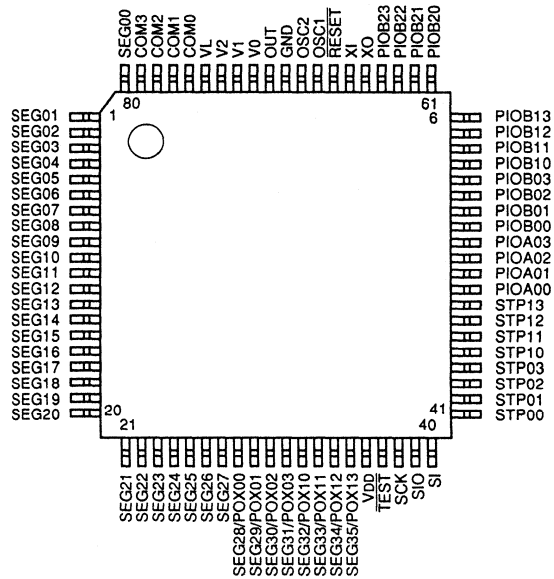
APPLICATION

The XL24410 series is ideal for applications where system flexibility and cost-effectiveness are required. The low V_{CC} operation, and the two low power modes, are ideal power saving features. Other features enable real time operations, LCD displays, and modulated high current output and sail battery-operated applications.

ASEC 6

PIN CONFIGURATION

80-PIN SQFP



KEY FEATURES

- Cost effective 4-bit microcontroller
- CMOS process for low current drain
- 3μs instruction time (2MHz)
- Two low power modes
  - — Halt mode: 10μA (max)
  - — Stop mode: 30μA (typical)
- Low voltage, single power supply:
  - — VDD=2.0~5.5V
- 8195 x 8 bytes ROM/256 x 6 bytes RAM
- Dual Oscillator
  - — Main clock: 300KHz - 2MHz
  - — Subclock: 30KHz - 50KHz
- 10-bit clock generating timer/counter with prescaler
- 8-bit programmable timer with 6 software selectable clock sources
- Six interrupts
  - — 2 external
  - — 4 internal (2 timer/counter, clock timer, serial I/O)
- 10-bit stack pointer
- 100 flexible instructions
- 8 Subroutine nesting levels
- 12 Schmitt input pins
- 4 CMOS inputs
- 20 general purpose I/O pins
- 8 LED drivers
- 8-bit serial I/O
- 8-channel 8-bit A/D converter
- External HALT/STOP mode release
  - — interrupt pin
  - — edge selectable input pin
- Built in watchdog timer (WDT)
- Form, fit, function emulator
- 80-pin SQFP package

OVERVIEW

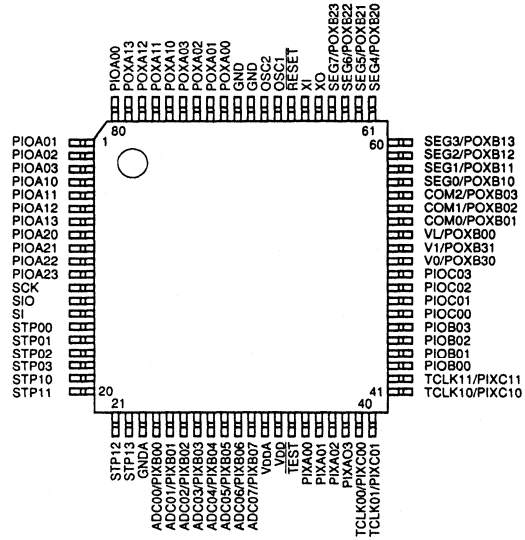
The XL24805 series is a mask programmable CMOS microcontroller. The device allows system optimization into a single IC by incorporating a wide variety of I/O blocks such as an 8-channel 8-bit A/D, 8-bit serial I/O, dual clock operation, internal timers, two low power modes, 4-bit I/O ports, internal and external interrupts, and 100 flexible instructions.

APPLICATION

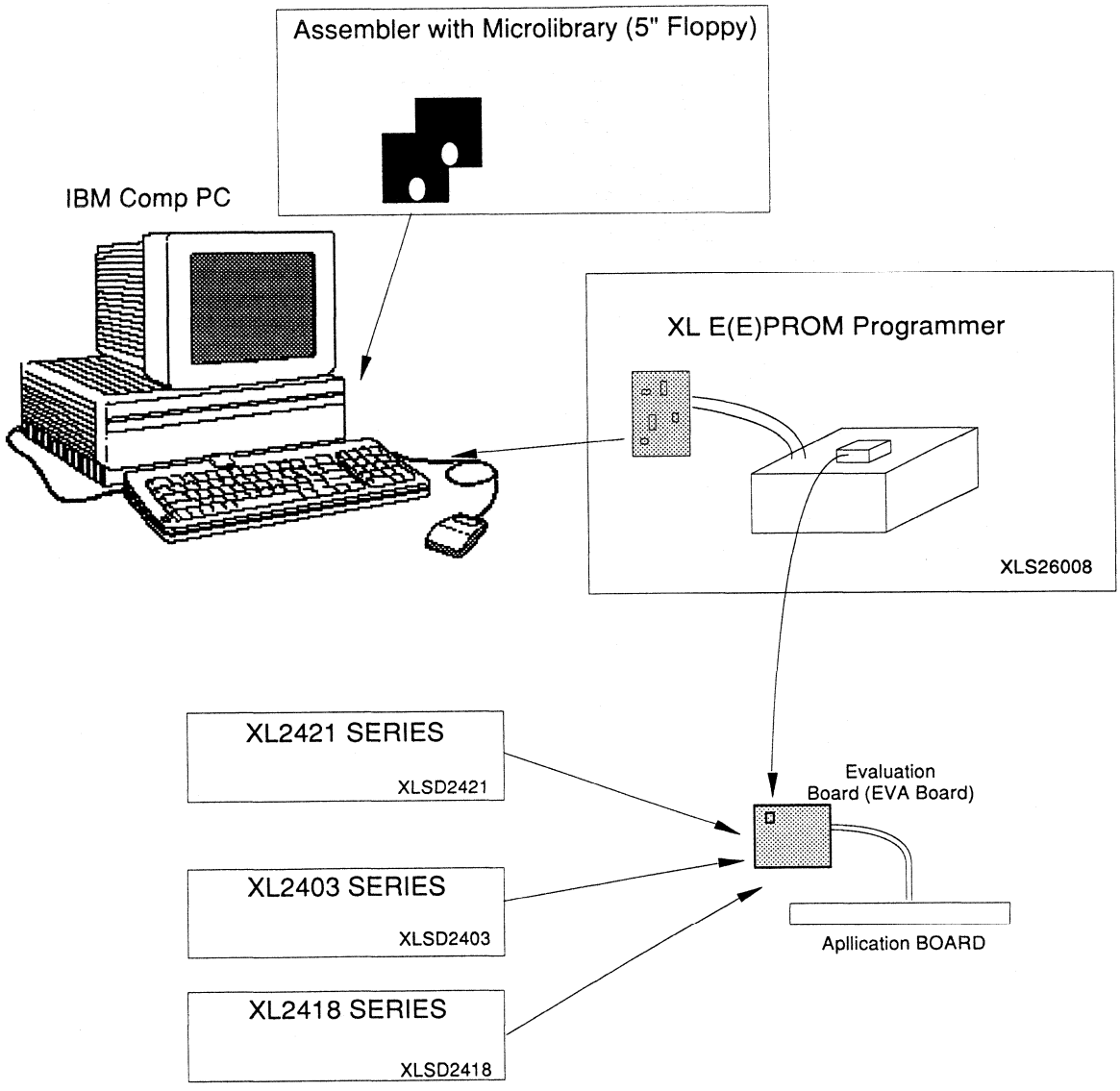
The XL24805 series is ideal for applications where system flexibility and cost-effectiveness are required. The low V_{CC} operation and the two low power modes are ideal power saving features. Other features enable real time operations, LCD display, A/D and serial I/O for battery operated applications.

PIN CONFIGURATION

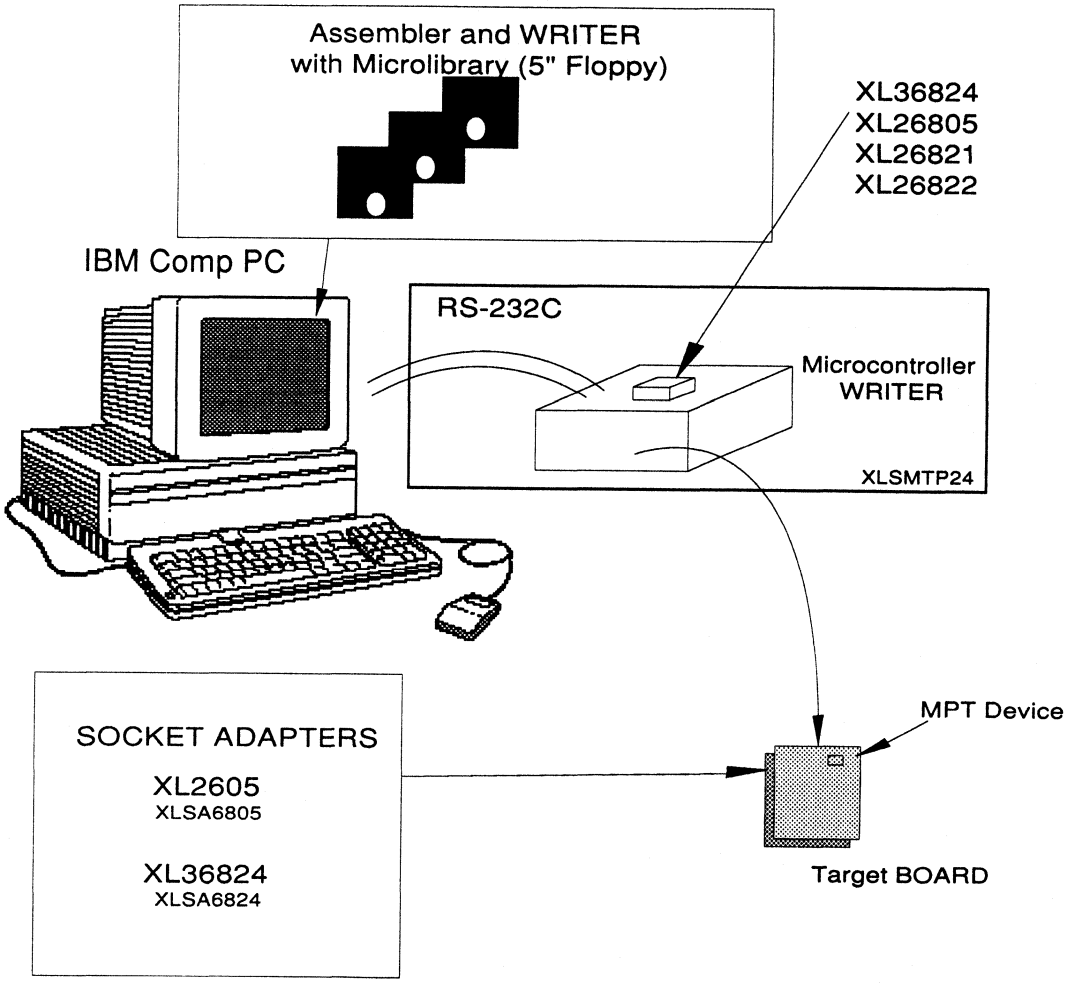
80-PIN SQFP



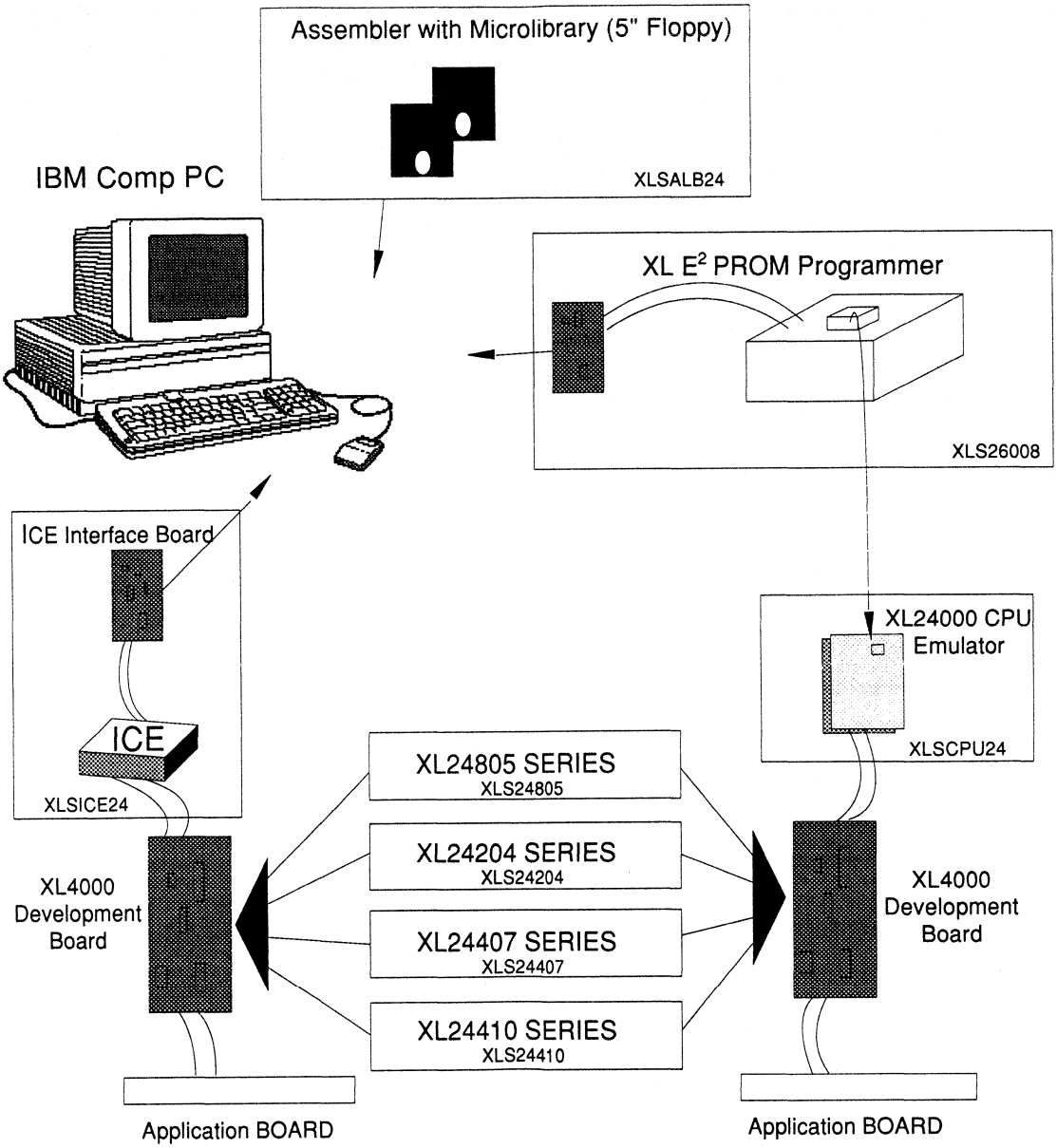
XL2400 FAMILY DEVELOPMENT



MULTIPLE TIME PROGRAMMABLE (MTP) TOOLS



XL24000 FAMILY DEVELOPMENT SYSTEM



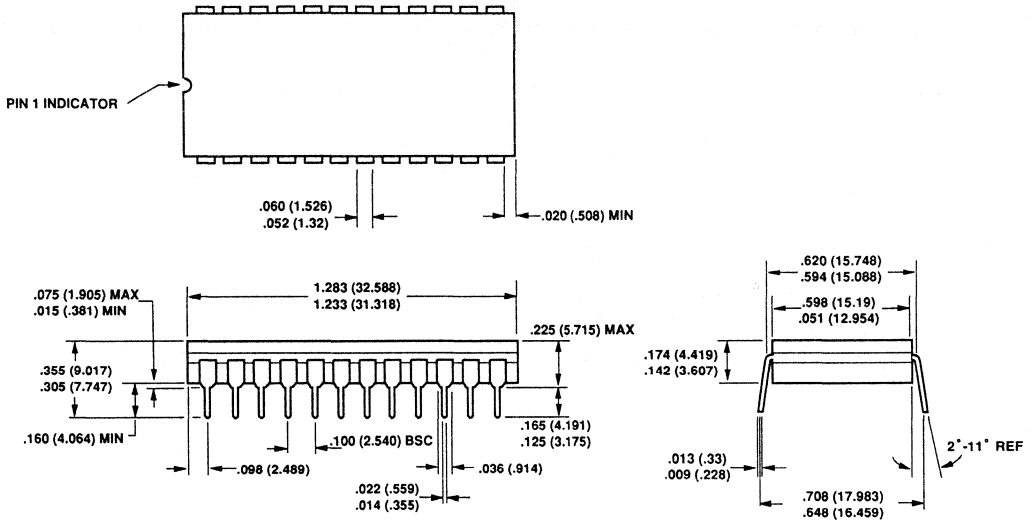
APPENDIX A Table of Contents

This section contains drawings of the more popular packages used on EXEL products. Drawings should be interpreted as follows:

1. Dimensions are shown in the form: Inches (millimeters).
2. Where given, the maximum and minimum for a dimension are shown one above the other.
3. A tolerance of .010 (.25) is allowed, unless otherwise specified.
4. Mold flash (not included in dimensions) is not to exceed .010 (.25).
5. Thickness on solder-dipped leads is not to exceed .020 (.51).

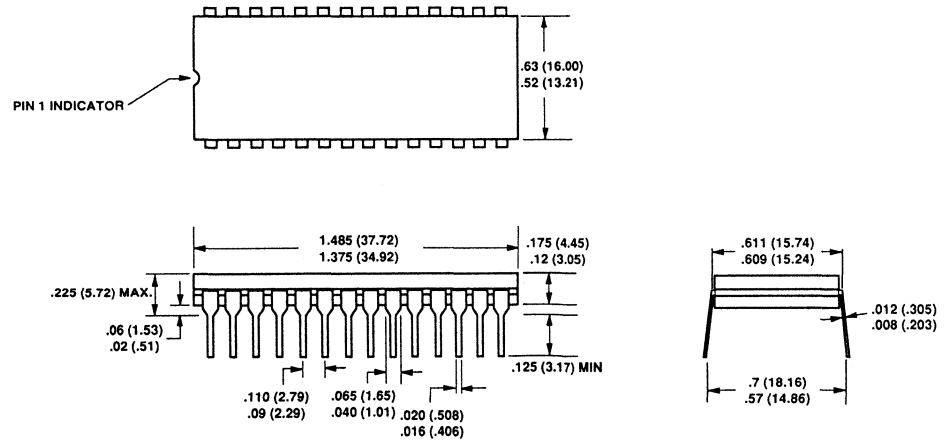
Please contact the factory for additional information, or if you have other packaging requirements.

24 Pin CERDIP (Type "C") Package

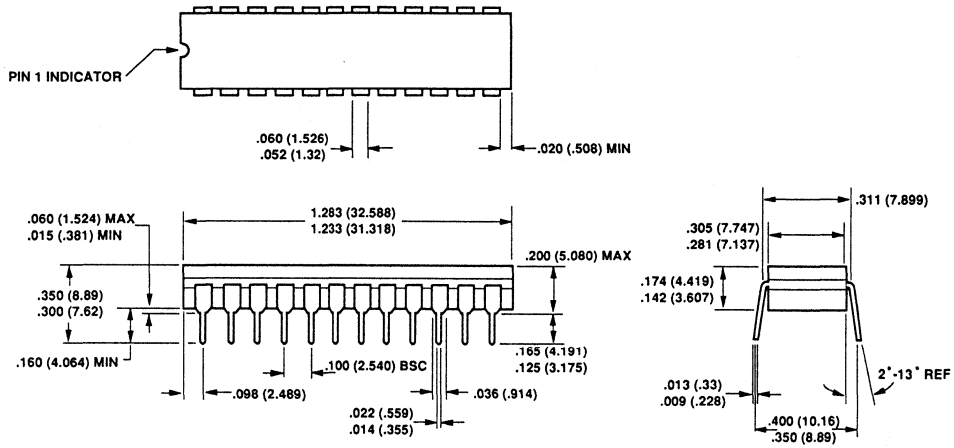


PKG A INFO

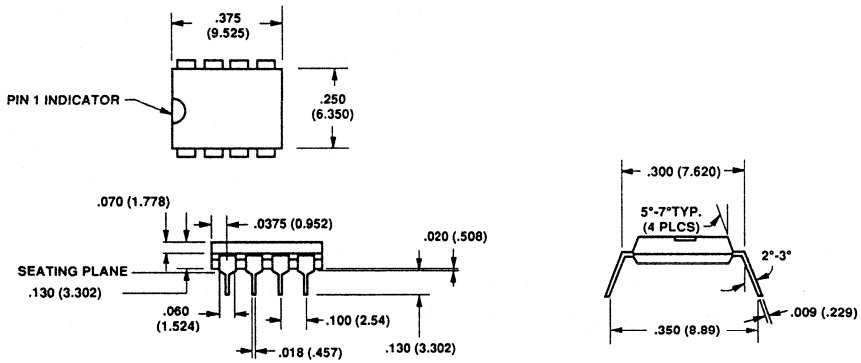
28 Pin CERDIP (Type "C") Package



24 Pin CERDIP Skinny (Type "C3") Package



8 Pin PDIP (Type "P") Package



PKG
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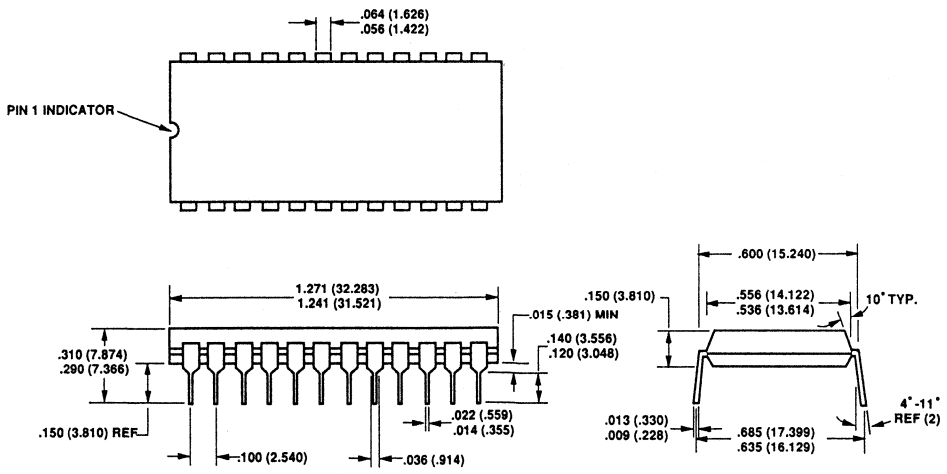
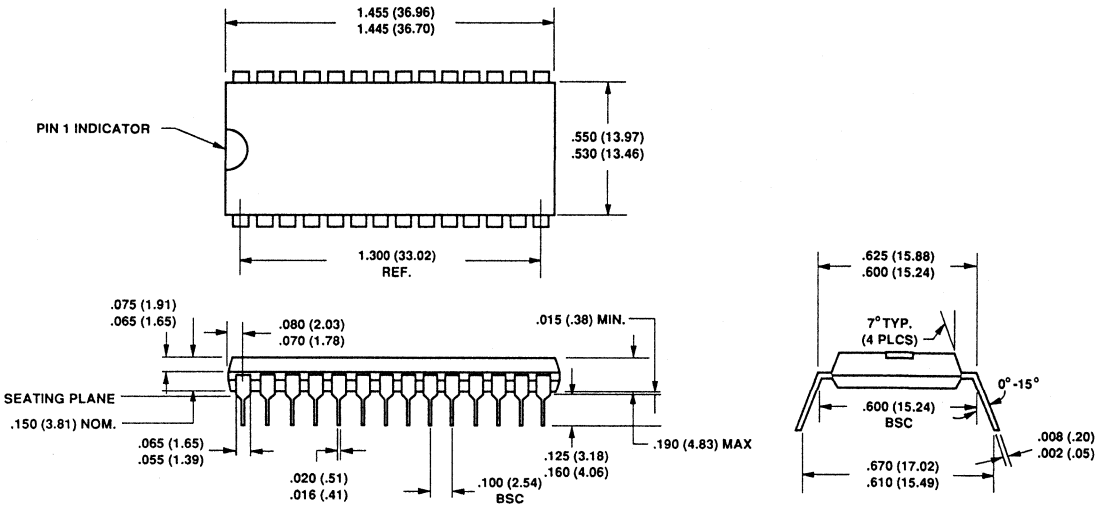
INFO

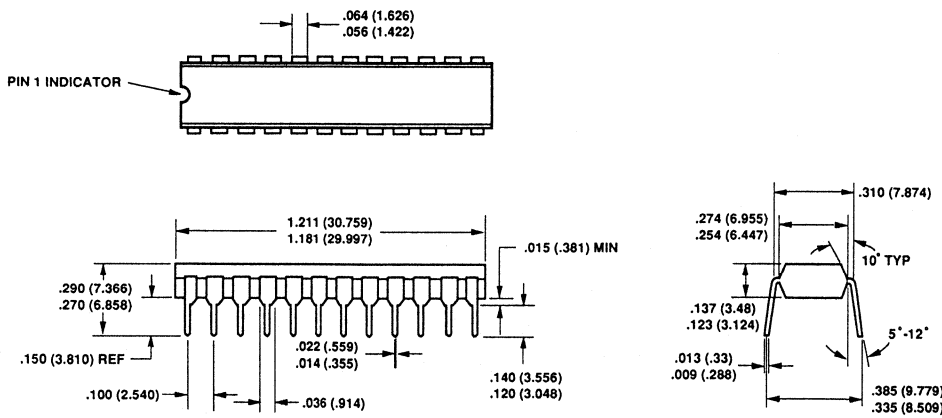
24 Pin PDIP (Type "P") Package



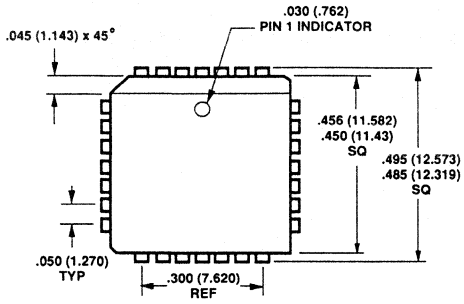
28 Pin PDIP (Type "P") Package

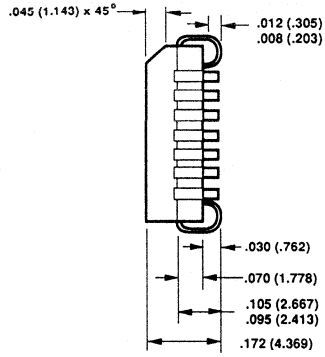


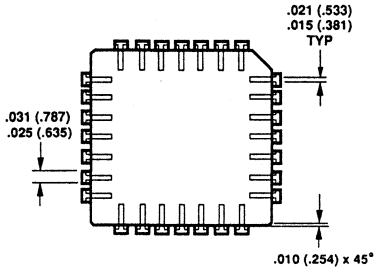
24 Pin Skinny DIP (Type "P3") Package

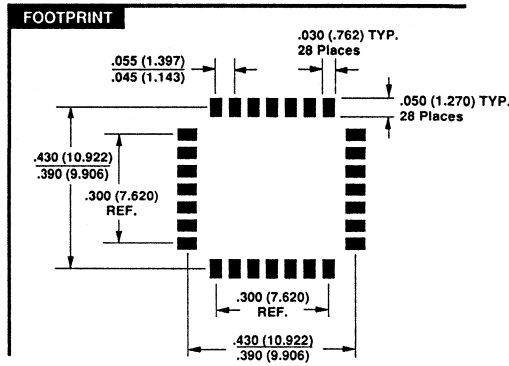


28 Pin PLCC (Type "D") Package



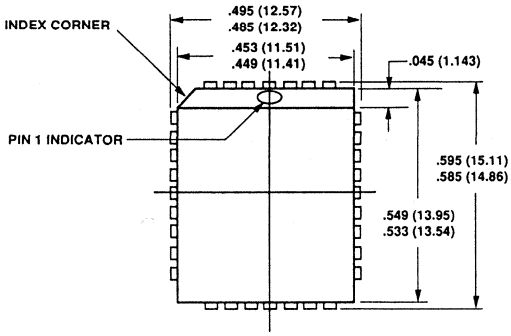


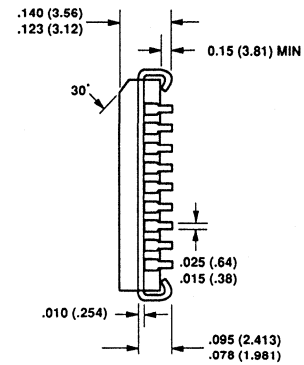


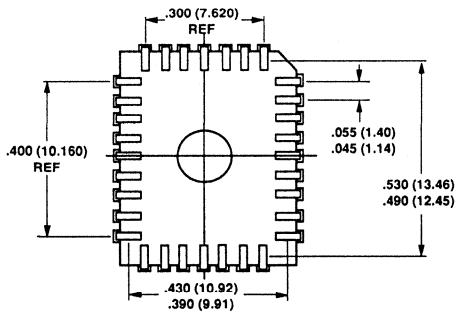


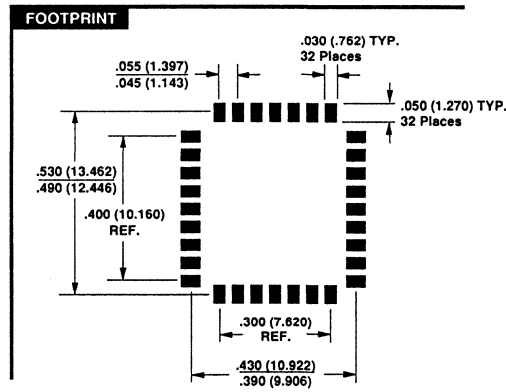
PKG A INFO

32 Pin PLCC (Type "D") Package

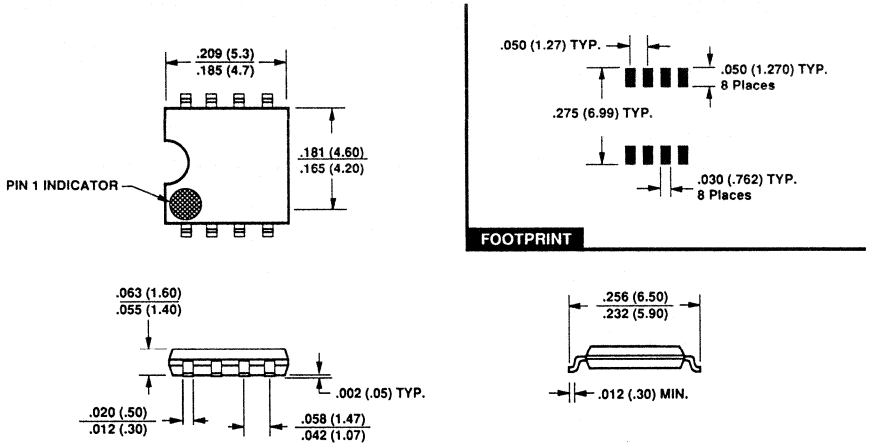








8 Pin EIAJ (Type "J" and "JR") SOIC Package*



PKG
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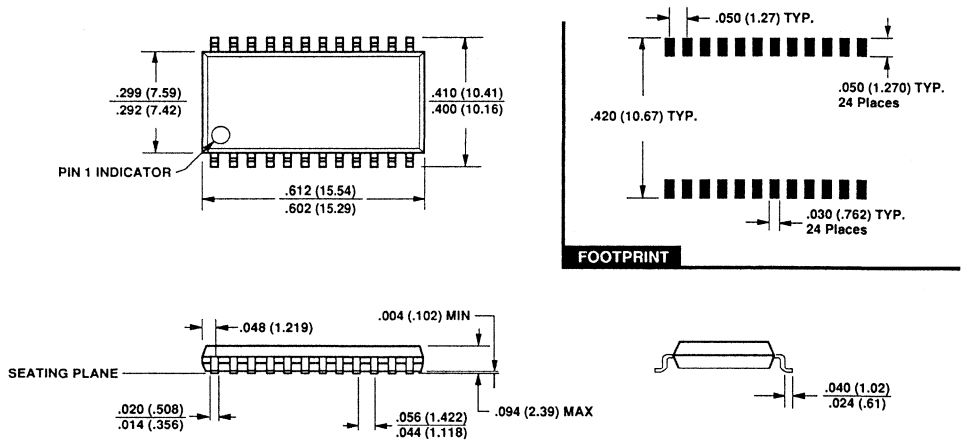
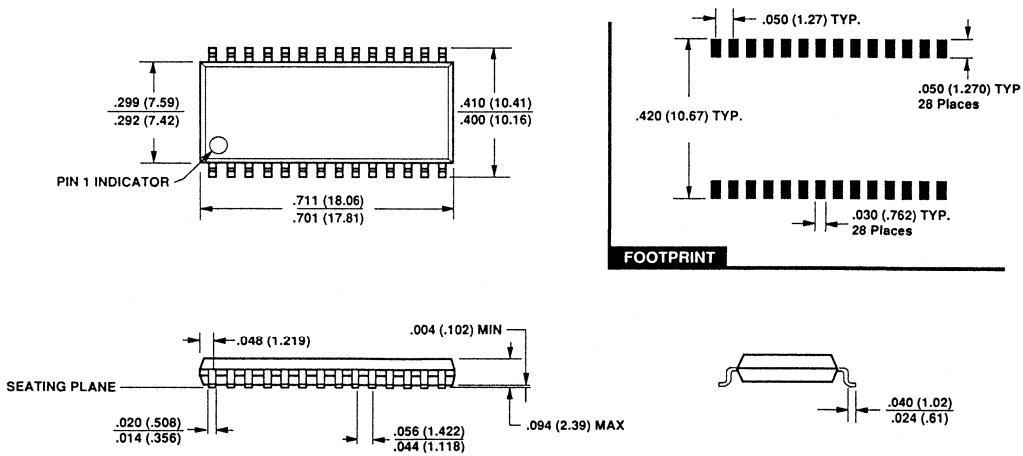
INFO

*See data sheets for pinout options.

24 Pin JEDEC (Type "J") SOIC Package



28 Pin JEDEC (Type "J") SOIC Package



APPENDIX B Table of Contents

Serial E^2PROMs

TEMP	EXEL	PKG	SPEED	ATMEL	CATALYST	MICROCHIP	NATIONAL	SGS-THOMPSON	SIEMENS	SIGNETICS	XICOR
XLS	24C01A	P	100KHz			24C01AP 85C72P		ST24C01B1	SDA2216 SDA2516	PCB8581P	X24C01P X24C01AP X24C01P-3.5
	24C01A	JR	100KHz			24C01ASN 85C72SN		ST24C01M1	SDA2216 SDA2516	PCB8581T	X24C01S X24C01AS X24C01S-3.5
XLE	24C01A	P	100KHz			24C01AIP 85C721P		ST24C01B6	SDA2216 SDA2516	PCF8581P	X24C01PI X24C01API X24C01PI-3.5
	24C01A	JR	100KHz			24C01AISN 85C72ISN		ST24C01M6	SDA2216 SDA2516	PCF8581T	X24C01SI X24C01ASI X24C01SI-3.5
XLS	24C01A-3	P	100KHz			24LC01P 24LH01P				PCB8581CP	X24C01/AP-3
	24C01A-3	JR	100KHz			24LC01SN 24LH01SN				PCB8581CT	X24C01/AS-3
XLE	24C01A-3	P	100KHz			24LC01IP 24LH01IP				PCF8581CP	X24C01/API-3
	24C01A-3	JR	100KHz			24LC01ISN 24LH01ISN				PCF8581CT	X24C01/API-3
XLS	24C02	P	100KHz	AT24C02-10PC	CAT24C02P	24C02AP 85C82P	NM24C02N	ST24C02AB1	SDA2526	PCB8582AP PCB8582BP	X2402P (NMOS) X24C02P
	24C02	JR	100KHz	AT24C02-10SC	CAT24C02J	24C02ASN 85C82SN	NM24C02M	ST24C02AM1	SDA2526	PCB8582AT PCB8582BT	X2402S(NMOS) X24C02S
XLE	24C02	P	100KHz	AT24C02-10PI	CAT24C02IP	24C02AIP 85C82IP	NM24C02EN	ST24C02AB6	SDA2526	PCF8582AP PCF8582BP	X2402PI (NMOS) X24C02PI
	24C02	JR	100KHz	AT24C02-10SI	CAT24C02IJ	24C02AISN 8582ISN	NM24C02EM	ST24C02AM6	SDA2526	PCF8582AT PCF8582BT	X2402SI (NMOS) X24C02SI
XLS	24C02-3	P	100KHz	AT24C02-10PC-2.7 AT24C02-10PC-2.5	CAT24LC02P	24LC02P 24LH02P		ST25C02AB1		PCB8582CP	X24C02P-3
	24C02-3	JR	100KHz	AT24C02-10SC-2.7 AT24C02-10SC-2.5	CAT24LC02J	24LC02SN 24LH02SN		ST25C02AM1		PCB8582CT	X24C02S-3
XLE	24C02-3	P	100KHz	AT24C02-10PI-2.7 AT24C02-10PI-2.5	CAT24LC02IP	24LC02IP 24LH02IP		ST25C02AB6		PCF8582CP	X24C02PI-3
	24C02-3	JR	100KHz	AT24C02-10SI-2.7 AT24C02-10SI-2.5	CAT24LC02IJ	24LC02ISN 24LH02ISN		ST25C02AM6		PCF8582CT	X24C02SI-3

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	ATMEL	CATALYST	MICROCHIP	NATIONAL	SGS-THOMPSON	SIEMENS	SIGNETICS	XICOR
XLS	24C04	P	100KHz	AT24C04-10PC	CAT24C04P	24C04AP 85C92P	NM24C04N	ST24C04B1	SDA2546		X2404P (NMOS) X24C04P X24C04P-3.5
	24C04	JR	100KHz	AT24C04-10SC	CAT24C04J	24C04ASN 85C92SN	NM24C04M	ST24C04M1	SDA2546		X2404S (NMOS) X24C04S X24C04S-3.5
XLE	24C04	P	100KHz	AT24C04-10PI	CAT24C04IP	24C04AIP 85C92IP	NM24C04EN	ST24C04B6	SDA2546		X2404PI (NMOS) X24C04PI X24C04PI-3.5
	24C04	JR	100KHz	AT24C04-10SI	CAT24C04IJ	24C04AISN 85C92ISN	NM24C04EM	ST24C04M6	SDA2546		X2404SI (NMOS) X24C04SI X24C04SI-3.5
XLS	24C04-3	P	100KHz	AT24C04-10PC-2.7 AT24C04-10PC-2.5	CAT24LC04P	24LC04P 24LH04P		ST25C04B1			X24C04P-3
	24C04-3	JR	100KHz	AT24C04-10SC-2.7 AT24C04-10SC-2.5	CAT24LC04J	24LC04SN 24LH04SN		ST25C04M1			X24C04S-3
XLE	24C04-3	P	100KHz	AT24C04-10PI-2.7 AT24C04-10PI-2.5	CAT24LC04IP	24LC04IP 24LH04IP		ST25C04B6			X24C04PI-3
	24C04-3	JR	100KHz	AT24C04-10SI-2.7 AT24C04-10SI-2.5	CAT24LC04IJ	24LC04ISN 24LH04ISN		ST25C04M6			X24C04SI-3
XLS	24C16	P	100KHz	AT24C16-10PC	CAT24C16P						X24C16P
	24C16	JR	100KHz	AT24C16-10SC	CAT24C16J						X24C16S
XLE	24C16	P	100KHz	AT24C16-10PI	CAT24C16IP						X24C16PI
	24C16	JR	100KHz	AT24C16-10SI	CAT24C16IJ						X24C16SI
XLS	24C16-3	P	100KHz	AT24C16-10PC-2.7 AT24C16-10PC-2.5	CAT24LC16P	24LC16P					X24C16P-3.5 X24C16P-3
	24C16-3	JR	100KHz	AT24C16-10SC-2.7 AT24C16-10SC-2.5	CAT24LC16J	24LC16SN					X24C16S-3.5 X24C16S-3
XLE	24C16-3	P	100KHz	AT24C16-10PI-2.7 AT24C16-10PI-2.5	CAT24LC16IP	24LC16IP					X24C16PI-3.5 X24C16PI-3
	24C16-3	JR	100KHz	AT24C16-10SI-2.7 AT24C16-10SI-2.5	CAT24LC16IJ	24LC16ISN					X24C16SI-3 X24C16SI-3

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	CATALYST	HYUNDAI	ICT	MICROCHIP	NATIONAL	OKI	ROHM	SAMSUNG
XLS	93LC06 93LC06 93LC06	P J JR	1MHz 1MHz 1MHz				93C06-/P 93C06-/SN	NMC93C06N NMC9306M8			
XLE	93LC06 93LC06 93LC06	P J JR	1MHz 1MHz 1MHz				93C06-I/P 93C46-I/SN	NMC93C06EN NMC9306EM8			
XLS	93LC46 93LC46 93LC46	P J JR	1MHz 1MHz 1MHz	CAT59C11P CAT59C11AP CAT93C46P CAT93C46AP CAT59C11K CAT59C11AK CAT93C46K CAT93C46AK	HY93C46S HY93C46J	93C46P 93C46AP 93CX46P 93C46S 93C46AS 93C46AK	59C11-/P ER5911-/P 93C46-/P 93C46X-/SN 93C46-/SN	NMC9314N NMC9346N NMC93C46N NMC93C46N3 NMC9346M8	MSM16811	BR93C46	KM93C46P
XLE	93LC46 93LC46 93LC46	P J JR	1MHz 1MHz 1MHz	CAT59C11PI CAT93C46PI CAT93C46API CAT59C11KI CAT93C46KI CAT93C46AKI	HY93C46ES HY93C46EJ	93C46PI 93C46API 93CX46PI 93C46SI 93C46ASI 93C46AKI	59C11-I/P ER5911-I/P 93C46-I/P 93C46X-I/SN 93C46-I/SN	NMC9346EN NMC93C46EN NMC93C46EN3 NMC93C46EM8	MSM16811P		KM93C46PI
XLS	93LC46-3 93LC46-3 93LC46-3	P J JR	1MHz 1MHz 1MHz			93CX46P 93CX46K		NMC93C46N3 (14 pins)			
XLE	93LC46-3 93LC46-3 93LC46-3	P J JR	1MHz 1MHz 1MHz			93CX46PI 93CX46KI		NMC93C46EN3 (14 pins)			
XLS	93C46 93C46	P J	1MHz 1MHz	CAT93C46P CAT93C46AP CAT59C11P CAT59C11AP CAT93C46K CAT93C46AK CAT59C11K CAT59C11AK	HY93C46S HY93C46J	93C46P 93C46AP 93CX46P 93C46S 93C46AS	59C11-/P 93C46-/P ER5911-/P 93C46X-/SN	NMC93C46N NMC9346N NMC9314N NMC93C46N3	MSM16811	BR93C46	KM93C46P
XLE	93C46 93C46	P J	1MHz 1MHz	CAT93C46PI CAT93C46API CAT59C11PI CAT93C46KI CAT93C46AKI CAT59C11KI	HY93C46ES HY93C46EJ	93C46PI 93C46API 93CX46PI 93C46SI 93C46ASI	59C11-I/P 93C46-I/P ER5911-I/P 93C46X-I/SN	NMC93C46EN NMC9346EN NMC93C46EN3	MSM16811P		KM93C46PI
XLS	93C46-3 93C46-3	P J	1MHz 1MHz			93CX46P		NMC93C46N3			
XLE	93C46-3	P J	1MHz 1MHz			93CX46PI		NMC93C46EN-3			

CROSS B REF

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	CATALYST	HYUNDAI	ICT	MICROCHIP	NATIONAL	OKI	ROHM	SAMSUNG
XLS	93CS46 93CS46	P J	1MHz 1MHz					NMC93CS46N		BR93CS46	
XLE	93CS46 93CS46	P J	1MHz 1MHz					NMC93CS46EN			
XLS	93CS46-3 93CS46-3	P J	1MHz 1MHz					NMC93CS46N3			
XLE	93CS46-3 93CS46-3	P J	1MHz 1MHz					NMC93CS46EN3			
XLS	93LC56 93LC56 93LC56	P J JR	1MHz 1MHz 1MHz	CAT35C102P		93C56AP 93CX56P		NMC93C56N NMC93C56N3			
XLE	93LC56 93LC56 93LC56	P J JR	1MHz 1MHz 1MHz	CAT35C102PI		93C56API 93CX56PI		NMC93C56EN NMC93C56EN3			
XLS	93LC56-3 93LC56-3 93LC56-3	P J JR	1MHz 1MHz 1MHz	CAT33C102P		93CX56P		NMC93C56N3			
XLE	93LC56-3 93LC56-3 93LC56-3	P J JR	1MHz 1MHz 1MHz	CAT33C102PI		93CX56PI		NMC93C56EN3			
XLS	93C56 93C56	P J	1MHz 1MHz			93C56AP 93CX56		NMC93C56N		BR93C56	
XLE	93C56 93C56	P J	1MHz 1MHz			93C56API 93CX56PI		NMC93C56EN			

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	MITSUBISHI	ROHM						
XLS	90C21 90C21	P J	1MHz 1MHz	M6M80021P	BR9021						
XLE	90C21 90C21	P J	1MHz 1MHz								

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	CATALYST	HYUNDAI	ICT	MICROCHIP	MITSUBISHI	NATIONAL	ROHM
	93LC66	P	1MHz	CAT35C104P CAT35C204P		93C66AP			NMC93C66N	
XLS	93LC66	J	1MHz	CAT35C104K CAT35C204K						
	93LC66	JR	1MHz			93C66AK				
	93LC66	P	1MHz	CAT35C104PI		93C66API			NMC93C66EN	
XLE	93LC66	J	1MHz	CAT35C104KI						
	93LC66	JR	1MHz			93C66AKI				
	93LC66-3	P	1MHz	CAT33C104P		93CX66P			NMC93C66N3	
XLS	93LC66-3	J	1MHz	CAT33C104K						
	93LC66-3	JR	1MHz							
	93LC66-3	P	1MHz			93CX66PI			NMC93C66EN3	
XLE	93LC66-3	J	1MHz							
	93LC66-3	JR	1MHz							
	93C66	P	1MHz	CAT35C104P						
	93C66	P							NMC93C66N	
XLS				CAT35C204P						
	93C66	J	1MHz	CAT35C104K CAT35C204K						
XLE	93C66	P	1MHz	CAT35C104PI		93C66PI			NMC93C66EN	
	93C66	J	1MHz	CAT35C104KI						

CROSS B REF

Serial E²PROMs

TEMP	EXEL	PKG	SPEED	CATALYST	HYUNDAI	ICT	MICROCHIP	MITSUBISHI	NATIONAL	ROHM
XLS	90C41	P	1MHz					M6M80041P		
	90C41	J	1MHz							
XLE	90C41	P	1MHz							

Parallel E²PROMs

TEMP	EXEL	PKG	SPEED	ATMEL	HUGHES	MICROCHIP	ROHM	SAMSUNG	SEEQ	XICOR
	2804A	P	250	AT28C04-25		PC28C04A-25/P	BR2804A-250		PQ2804A-250	X2804AP-25
XLS	2804A	P	300		HC3104ACP-300		BR2804A-300		PQ2804A-300	X2804AP
	2804A	P	350				BR2804A-350		PQ2804A-350	X2804AP-35
	2804A	P	450				BR2804A-450			X2804AP-45
	2816A	P	250			28C04A-25I/P	BR2816A-250	KM2816APC-25	PQ2816A-250 PQ5516A-250	X2816AP-25
	2816A	P	300				BR2816A-300	KM2816APC-30	PQ2816A-300 PQ5516A-300	X2816AP
	2816A	P	350				BR2816A-350	KM2816APC-35	PQ2816A-350 PQ5516A-350	X2816AP-35
	2816A	P	450		HC3248CP		BR2816A-450			X2816AP-45
	2816A	C	250			28C04A-25I/P			DQ2816A-250 DQ5516A-250	X2816AD-25
XLS	2816A	C	300						DQ2816A-300 DQ5516A-300	X2816AD
	2816A	C	350						DQ2816A-350 DQ5516A-350	X2816AD-35
	2816A	C	450		HC3248CD					X2816AD-45
	2816A	D	250							
	2816A	D	300							
	2816A	D	350							
	2816A	D	450							
	2816A	P	250							X2816API-25
	2816A	P	300							X2816API
	2816A	P	350							X2816API-35
XLE	2816A	P	450		HI3248CD					X2816API-45
	2816A	C	250						DE2816A-250	X2816ADI-25
	2816A	C	300							X2816ADI
	2816A	C	350						DE2816A-350	X2816ADI-35
	2816A	C	450							X2816ADI-45

Parallel E²PROMs

TEMP	EXEL	PKG	SPEED	ATMEL	CATALYST	MICROCHIP	OKI	ROHM	SAMSUNG	SEEQ	XICOR
	28C16A	P	100					BR28C16-10			
	28C16A	P	150	AT28C16-15PC		28C16A-15/P	MSM28C16A	BR28C16-15	KM28C16PC-15		
	28C16A	P	200	AT28C16-20PC	CAT28C16AP-20	28C16A-20/P		BR28C16-20	KM28C16PC-20	PQ52B13-200	
	28C16A	P	250	AT28C16-25PC		28C16A-25/P		BR28C16-25	KM28C16PC-25	PQ52B13-250	X2816AP-25
										PQ52B13-350	X2816AP-35
	28C16A	C	100								
	28C16A	C	150	AT28C16-15DC		28C16A-15/J					
XLS	28C16A	C	200	AT28C16-20DC		28C16A-20/J				DQ52B13-200	
	28C16A	C	250	AT28C16-25DC		28C16A-25/J				DQ52B13-250	X2816AD-25
										DQ52B13-350	X2816AD-35
	28C16A	D	100								
	28C16A	D	150	AT28C16-15JC		28C16A-15/L					
	28C16A	D	200	AT28C16-20JC	CAT28C16AN-20	28C16A-20/L					
	28C16A	D	250	AT28C16-25JC		28C16A-25/L					
	28C16A	J	100								
	28C16A	J	150								
	28C16A	J	200								
	28C16A	J	250								
	28C16A	P	100								
	28C16A	P	150	AT28C16-15PI		28C16A-15I/P					
	28C16A	P	200	AT28C16-20PI	CAT28C16API-20	28C16A-20I/P					
	28C16A	P	250	AT28C16-25PI		28C16A-25I/P					X2816API-25
	28C16A	C	100								
	28C16A	C	150	AT28C16-15DI		28C16A-15I/J					
	28C16A	C	200	AT28C16-20DI		28C16A-20I/J					
XLE	28C16A	C	250	AT28C16-25DI		28C16A-25I/J				DE52B13-250	X2816ADI-25
										DE52B13-300	X2816ADI
										DE52B13-350	X2816ADI-35
	28C16A	D	100								
	28C16A	D	150	AT28C16-15JI		28C16A-15I/L					
	28C16A	D	200	AT28C16-20JI	CAT28C16ANI-20	28C16A-20I/L					
	28C16A	D	250	AT28C16-25JI		28C16A-25I/L					
	28C16A	J	100								
	28C16A	J	150								
	28C16A	J	200								
	28C16A	J	250								

Parallel E²PROMs

TEMP	EXEL	PKG	SPEED	CATALYST	MITSUBISHI	ROHM						
	46C15	P	55/V5			BR46C15-55						
XLS	46C15	P	60/V5			BR46C15-60						
	46C15	P	70/V5			BR46C15-70						
	46C15	P	85/V5			BR46C15-85						
	46C15	P	55/V5									
XLE	46C15	P	60/V5									
	46C15	P	70/V5									
	46C15	P	85/V5									

CROSS B REF

Parallel E²PROMs

TEMP	EXEL	PKG	SPEED	AMD	ATMEL	HITACHI	ROHM	SAMSUNG	SEEQ	XICOR
XLS	2864A	P	250		AT28PC64-25PC	HN58064P-25	BR2864A-250	KM2864APC-25	PQ52B33-250	X2864AP-25
	2864A	P	300			HN58064P-30	BR2864A-300	KM2864APC-30		X2864AP
	2864A	P	350				BR2864A-350		PQ52B33-350	X2864AP-35
	2864A	P	450				BR2864A-450			X2864AP-45
	2864A	C	250	Am2864AE-250DC Am2864AE-255DC	AT28PC64-25DC				DQ52B33-250	X2864AD-25
	2864A	C	300	Am2864AE-300DC Am2864AE-305DC						X2864AD
	2864A	C	350	Am2864AE-350DC Am2864AE-355DC					DQ52B33-350	X2864AD-35
	2864A	C	450							X2864AD-45
	2864A	D	250		AT28PC64-25JC					X2864AJ-25
	2864A	D	300							X2864AJ
	2864A	D	350							X2864AJ-35
	2864A	D	450							X2864AJ-45
XLE	2864A	P	250		AT28PC64-25PI					X2864API-25
	2864A	P	300							X2864API
	2864A	P	350							X2864API-35
	2864A	P	450							X2864API-45
	2864A	C	250	Am2864AE-250DI Am2864AE-255DI	AT28PC64-25DI				DE52B33-250	X2864ADI-25
	2864A	C	300	Am2864AE-300DI Am2864AE-305DI					DE52B33-300	X2864ADI
	2864A	C	350	Am2864AE-350DI Am2864AE-355DI						X2864ADI-35
	2864A	C	450							X2864ADI-45
	2864A	D	250		AT28PC64-25JI					X2864AJI-25
	2864A	D	300							X2864AJI
	2864A	D	350							X2864AJI-35
	2864A	D	450							X2864AJI-45

Parallel E²PROMs

TEMP	EXEL	PKG	SPEED	AMD	ATMEL	HITACHI	ROHM	SAMSUNG	SEEQ
	2865A	P	250		AT28C64-25PC	HN58C65P-25	BR2865A-250	KM2865APC-25	PQ2864-250
	2865A	P	300				BR2865A-300	KM2865APC-30	PQ2864-300
	2865A	P	350				BR2865A-350		PQ2864-350
	2865A	P	450				BR2865A-450		
	2865A	C	250	Am2864BE-250DC Am2864BE-255DC	AT28C64-25DC				DQ2864-250
XLS	2865A	C	300	Am2864BE-300DC Am2864BE-305DC					DQ2864-300
	2865A	C	350	Am2864BE-350DC Am2864BE-355DC					DQ2864-350
	2865A	C	450						
	2865A	D	250		AT28C64-25JC				NQ2864-250
	2865A	D	300						NQ2864-300
	2865A	D	350						NQ2864-350
	2865A	D	450						
	2865A	P	250		AT28C64-25PI				
	2865A	P	300						
	2865A	P	350						
	2865A	P	450						
	2865A	C	250	Am2864BE-250DI Am2864BE-255DI	AT28C64-25DI				DE2864-250
XLE	2865A	C	300	Am2864BE-300DI Am2864BE-305DI					DE2864-300
	2865A	C	350	Am2864BE-350DI Am2864BE-355DI					DE2864-350
	2865A	C	450						
	2865A	D	250		AT28C64-25JI				
	2865A	D	300						
	2865A	D	350						
	2865A	D	450						

Parallel E^2PROMs

TEMP	EXEL	PKG	SPEED	ATMEL	CATALYST	FUJITSU	MICROCHIP	NEC	SAMSUNG	SEEQ	XICOR
	28C64	P	150	AT28PC64-15PC	CAT28C64AP-150		28C64A-15/P		KM28C64PC-20	PQ28C64-250	X2864BP-15
			200	AT28PC64-20PC	CAT28C64AP-200		28C64A-20/P	μ PD28C64-20	KM28C64P-25	PQ28C64-300	X2864BP-18
			250	AT28PC64-25PC			28C64A-25/P	μ PD28C64-25		PQ28C64-350	
XLS	28C64	C	150	AT28PC64-15DC			28C64A-15/J			DQ28C64-250	X2864BD-15
			200	AT28PC64-20DC			28C64A-20/J	μ PD28C64-20		DQ28C64-300	X2864BD-18
			250	AT28PC64-25DC		MBM28C64-25	28C64A-25/J	μ PD28C64-25		DQ28C64-350	28C64D70
	28C64	D	150	AT28PC64-15JC	CAT28C64AN-150		28C64A-15/L			NQ28C64-250	X2864BJ-15
			200	AT28PC64-20JC	CAT28C64AN-200		28C64A-20/L	μ PD28C64-20		NQ28C64-300	X2864BJ-18
			250	AT28PC64-25JC-25		MBM28C64-25	28C64A-25/L	μ PD28C64-25		NQ28C64-350	28C64P70
	28C64	P	150	AT28PC64-15PI	CAT28C64API-150	28C64A-15I/P					X2864BPI-15
			200	AT28PC64-20PI	CAT28C64API-200	28C64A-20I/P					X2864BPI-18
			250	AT28PC64-25PI		28C64A-25I/P					X28C64PI-20
XLE	28C64	C	150	AT28PC64-15DI		28C64A-15I/J			DE28C64-250		X2864BDI-15
			200	AT28PC64-20DI		28C64A-20I/J			DE28C64-300		X2864BDI-18
			250	AT28PC64-25DI		28C64A-25I/J			DE28C64-350		X28C64DI-20
	28C64	D	150	AT28PC64-15JI	CAT28C64ANI-150	28C64A-15I/L					X2864BJI-15
			200	AT28PC64-20JI	CAT28C64ANI-200	28C64A-20I/L					X2864BJI-18
			250	AT28PC64-25JI		28C64A-25I/L					X28C64JI-20

APPENDIX C

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INTRODUCTION

At EXEL Microelectronics, quality is our number one priority. This commitment is stated in the EXEL Quality Manual (EQM) and implemented on a daily basis in every phase of our operation. The program is designed to meet or exceed all requirements of MIL-I-45208, Inspection System Requirements.

Quality improvement is recognized as an extremely effective method for reducing manufacturing costs. At EXEL Microelectronics every employee views quality as a basic requirement of job performance - not merely an external goal to be enforced by a separate organization.

Our goal is to achieve a level of quality equal to ROHM Company, Ltd., our parent organization. Through the years ROHM Company has continually demonstrated excellence in the quality and reliability of their products. In recognition of this achievement they have received numerous awards and honors as illustrated in Table 1.

In EXEL Microelectronics, quality is an interactive process consisting of four primary activities:

- Formal policies, procedures, and work instructions document quality standards and provide the vehicle for continuing process improvement.
- Networked computer systems share information throughout the company. Using a program data base with common interfaces, quality monitors can be compared with project estimates to increase the accuracy of quality and reliability predictions.
- Unique identifiers are used to monitor material, product, and processes and provide source traceability on any discrepancy.
- Item discrepancy records track quality attributes throughout each phase of production and trigger corrective action for continuous process improvement.

Interactive quality is both a system and structural discipline integrating design, production, and quality requirements in an environment that fosters creative process improvements. Interactive quality begins proactively on new programs and works reactively on old problems.

Figure 1 outlines the structure of the Product Assurance organization. This organization has the charter to develop a Total Quality Management program based on the requirements of the EQM. Table 2 summarizes the contents of the EQM with a cross reference to applicable military requirements.

TABLE 1. ROHM COMPANY, LTD. QUALITY ACHIEVEMENTS

CUSTOMER	AWARD
Chrysler Corporation	Quality Excellence Award Pentastar Award
Ford Motor Company	Q1 Preferred Vendor
American Telephone and Telegraph	Quality Leadership Award
General Motors	Targets for Excellence Program Preferred Supplier
Motorola	Partnership for Growth
Honeywell	Quality is Key Ship to Stock
Digital Equipment Corporation	Ship to Stock Quality Program
IBM	Preferred Source Primary Source Supplier

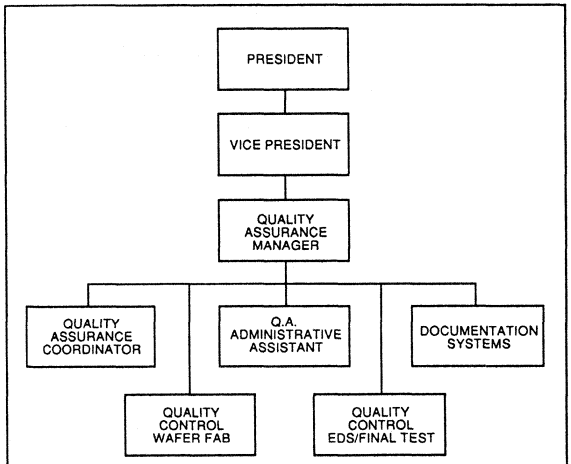

FIGURE 1. PRODUCT ASSURANCE ORGANIZATION

TABLE 2. EXEL QUALITY MANUAL

EQM SECTION		MILITARY REFERENCE		
		Mil-I-45208	Mil-Q-9858	Mil-M-38510
1.	Introduction			
2.	Quality Statement			20.1.3.1
3.	Organization			
4.	Product Assurance Department Charters			
5.	Cross Reference			
01.01	Inspection and Test Documentation	3.2.1	4.1	20.1.1.3
02.00	Specification/Order Review and Traveler Generation			
03.00	Quality Records	3.2.2	4.1	20.1.2
04.01	Corrective Action	3.2.4	3.5	20.1.1.11
05.00	Drawing Documentation and Change Control	3.2.4	4.1	10.1.2.4
06.01	Calibration	3.3	4.2	20.1.1.9
07.01	In-Process Quality Controls	3.4	6.2	20.1.2.6
08.00	Inspection Stamps	3.5	6.7	
09.01	Indication of Inspection Status	3.5	6.7	
10.01	Non-Conforming Material	3.7	6.5	
11.01	Sampling Inspection	3.9	6.6	30.0
12.01	Vendor Control/Receiving Inspection	3.12	5.1	20.1.1.3
13.00	Government/Customer Property	3.6	7.2	
14.01	Customer Returned Material			
15.00	Government/Customer Source Inspection	3.11	7.1	
16.01	Work Instructions			
17.00	Test and Inspection of Completed Materials			
18.01	Purchase Order Review	3.11	3.2	
19.01	Quality Audit			
10.01	Material Control and Handling			
21.01	Electrostatic Discharge Control			
22.01	Statistical Process Control			
23.00	Operator Training			
24.01	Cost of Quality			
25.00	Test Software Control			
26.01	Lot Control System			
27.00	Customer Initiated Corrective Action			
28.00	Customer Product Change Notification			
29.00	Failure Analysis			

RELIABILITY PROGRAM

The reliability program begins at the conceptual phase of a new project. Based on market analysis or customer requirements, fundamental decisions and trade-offs are made. Price, performance, and design are weighed against reliability; a model is developed that defines reliability goals and risks in a real world environment.

During the prototype stage of a program, reliability risks are reduced as concept becomes hardware. Actual prototypes are fabricated, designs are finalized and frozen, materials and processes are defined. At this stage of the program the objectives are to ensure that known good practices are applied, that deviations are detected and corrected, and that any areas of uncertainty are identified and investigated.

When the product is transferred to preproduction, a long term reliability study is developed. This ensures that the design, all materials and processes, and controls have the highest possible level of confidence. Data collection and analysis continue through the full scale production phase and into field applications.

Throughout the entire life of the product, reliability continues to be assessed: from initial predictions based on past experiences, to refined predictions based on current examination. An illustration of this reliability model is shown in Figure 2.

Based on the reliability of other EXEL E^2PROM products, EXEL performs a number of tests to evaluate the condition of devices after a greater-than-worst-case-application. These tests include:

- **Erase/Write Endurance Cycling**
  Devices are programmed, read, erased, and re-programmed with the original data pattern until the specified number of cycles is attained or the device begins to exhibit cell failures.

- **Electrostatic Discharge**
  This test generally employs circuitry equivalent to the human body model (e.g. a 100 pf. capacitor which is discharged through a 1500ohm resistor). Device pin specification limits are specified on all pins.

- **CMOS Latchup Test (SCR Effect)**
  Input and output pins are tested one at a time for both negative and positive current pulses. Output pins must be preconditioned to a logical HIGH state for positive current test, and preconditioned to a logical LOW state for negative current testing.

- **Mechanical Shock (6 Axis)**
  Devices under test are attached firmly to the inside of a cube, and dropped from a distance of approximately 2 1/2 feet. After test is completed, devices are tested electrically to ensure performance has not degraded.

- **Variable Frequency Vibration**
  Devices are firmly secured on a vibration platform. Frequency is varied logarithmically from 20Hz to 2000Hz and back four times per device in X, Y, and Z axes.

- **Lead Integrity**
  Device leads are bent several times through a given angle and returned to their original position. Devices are subsequently visually inspected under 10 X magnification for evidence of breakage, loosening or relative motion between the device body and the terminal lead.

- **Physical Dimensions**
  Devices are measured using micrometers, calipers, gauges, or other equipment capable of determining the actual device physical dimensions.

When a failure occurs, the device is analyzed to determine the cause and identify the remedy. Failure analysis is performed in accordance with procedure EQR001.

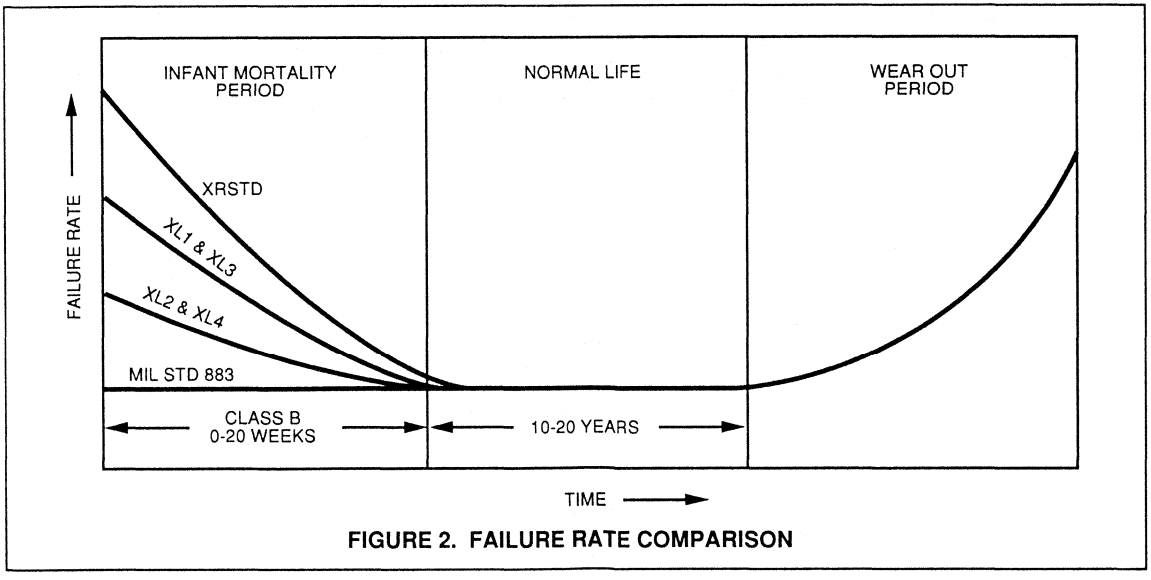

FIGURE 2. FAILURE RATE COMPARISON

REL & C Q.A.

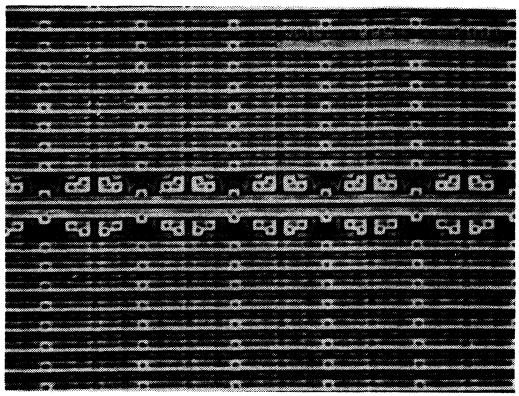

FIGURE 3A. SEM PHOTOGRAPH OF PARTIAL E^2PROM CELL ARRAY — TOP VIEW

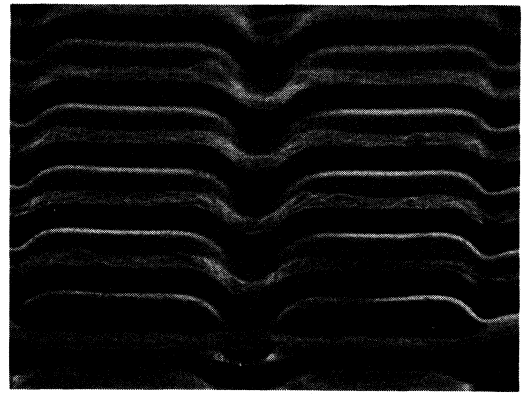

FIGURE 3B. SEM PHOTOGRAPH SIDE VIEW OF METAL LINES GOING OVER E^2PROM ARRAY

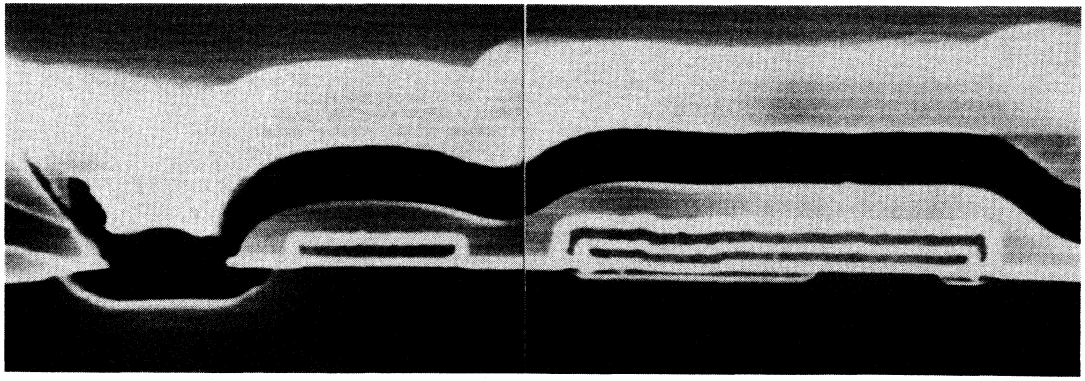

FIGURE 3C. SEM PHOTOGRAPH CROSS SECTION OF A TYPICAL E^2PROM CELL

To obtain a detailed look at the failed site, a Scanning Electron Microscope (SEM) is used. Using a magnification up to 20,000X, extremely fine details can be viewed and the failed mechanism can be studied and a cause assigned based on the morphology of the fail site. Figures 3A through 3C illustrate the resolution possible with this instrument.

Metallurgical problems can be studied at this magnification and process problems become very evident. Voltage contrast can electrically exercise the device to observe voltage levels as they propagate along the internal conducting lines. When a break in the voltage level occurs a fail site is identified. Electron Beam Induced Current (EBIC) analysis can also be employed to find degraded or damaged junctions which are not visible optically.

Cross sectioning is performed on both die failures and assembly defects. This technique reveals the entire profile of the process and delineates areas which are at or below the silicon surface. Staining can be used to show the depth of and damage to diffused junction below the silicon surface. Assembly failures are identified, electrical shorts between multiple level conductors can be seen, and interlevel oxide quality can be determined.

Electron Dispersive X-Ray (EDX) analysis is used to determine the elemental composition of the material being studied. Contaminants may have been introduced during die fabrication or in assembly operations. EDX can identify the contaminant and initiate corrective action at the appropriate production workcenter.

Following analysis the collected data is reviewed and a determination of the failure mode documented. All data and supporting documentation is forwarded to a reliability specialist for inclusion in future estimating and predictions.

DESIGN QUALITY

EXEL designers have combined the most desirable attributes of simpler memory types into state-of-the-art E^2PROM devices. EXEL devices are fast, reliable, easy-to-use, writable yet nonvolatile memory devices. Their effect on existing system design methodology is significant.

E^2PROMs achieve their nonvolatility through the use of a floating gate structure. To change the state of the charge stored on the floating gate, electrons are passed through a silicon dioxide insulator to or from the floating gate by means of a quantum mechanical phenomenon known as Fowler-Nordheim tunneling. When the electric field applied across an insulator exceeds approximately 10 megavolts per centimeter, a number of electrons from the negative electrode will acquire enough energy to pass a short distance through the "forbidden" gap band of the insulator and enter the conduction band where they will flow freely toward the barrier to get to the other side. In E^2PROM devices, the negative electrode is the floating gate, the insulator is silicon dioxide, and the positive electrode is the silicon substrate when the erase function is performed.

Fowler-Nordheim tunneling has been extensively modeled, and EXEL designers can accurately predict how many electrons pass from the negative electrode and move freely toward the positive electrode given an applied voltage and specified period of time. Since the threshold field strength required for tunneling is approximately ten megavolts per centimeter, very thin tunnel oxide regions — approximately 120 angstroms thick — are required to enable operation with reasonable on-chip voltages (ie. 20 volts) Figure 4 illustrates the basic E^2PROM cell.

To tunnel electrons onto the floating gate, the drain voltage is brought to zero while raising the gate voltage. This capacitively couples the floating gate to a positive potential causing electrons to tunnel onto it. The process may be reversed to discharge the gate by applying a positive potential to the drain while grounding the gate.

The specified conditions must be maintained for a time sufficient to cause the required amount of charge to transfer. This time is influenced by factors such as the thin oxide dimension, the threshold voltage of the device, and the shape and amplitude of the high voltage pulse.

INTRINSIC FAILURE MECHANISMS

E^2PROMs and light emitting diodes differ from many other semiconductor devices in that they wear out with use. However, with a basic understanding of the intrinsic wear

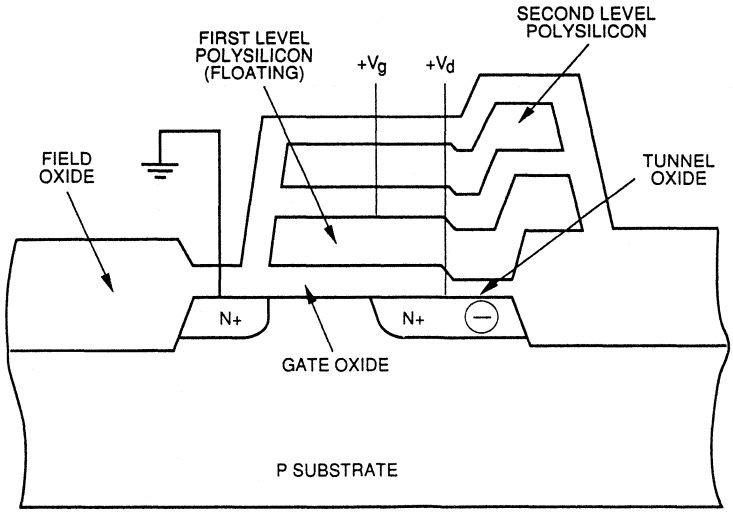

FIGURE 4. CROSS SECTION OF THE BASIC E^2PROM CELL

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out and failure mechanisms associated with E²PROMs, EXEL designers construct systems which successfully account for these limitations. The primary failure mechanisms which affect all E²PROM devices are charge trapping and voltage stress.

EXEL E²PROMs use a polysilicon floating gate structure and tend to have better endurance characteristics and superior data retention under voltage and temperature stress. Polysilicon floating gate devices also have a longer history of processing which ensures reproducibility and slow wear out as compared to nitride systems.

CHARGE TRAPPING

The major cause of endurance limitations is dielectric breakdown related to the trapping of a minute number of electrons in the tunnel dielectric during each erase/write operation. An ideal feature of a tunneling dielectric is that it should never remember the number of electrons that passed through it or the voltage that was previously applied across the film. Unfortunately, for the thermally grown silicon dioxide used as the insulator, there always exist a number of electron and hole traps. When the cell is erased or written, electrons are injected through the thin oxide and some of them will be captured by these traps, causing a buildup of negative charges in the oxide. This effect is cumulative and reduces the electric field at the injection interface, thus decreasing the tunneling current and causing the gradual reduction of the threshold margins required to differentiate logic "1's" and "0's." The trapped electrons cause an increase in the electric field across the oxide which eventually results in a partial breakdown of the oxide and leakage of the charge stored on the floating gate. This breakdown becomes a data retention failure and usually occurs before the threshold margin has been reduced to a point below the minimum acceptable level.

VOLTAGE STRESS

In an ideal E²PROM cell, the electric field across the tunneling oxide should be constant. However, because of imperfections inherent in the manufacturing process, the thickness of the oxide may not be constant, with some cells having greater variations than the average. Thinner areas are subject to a higher electric field strength, and therefore greater tunneling current during erase/write cycles. As more cycles are performed, the probability increases that a pinhole or other imperfection in the tunneling oxide will break down. Eventually a cell will fail to program correctly because of a shorted tunnel oxide layer. Endurance failures of this type usually occur early in the life of the device and are normally weeded out by the erase/write cycling performed during device testing.

EXEL engineers use the robust design principle in the conception and development of new devices. This methodology is practiced to ensure that the device circuit is capable of handling a load greater than the maximum variations which may be present in the fabrication process. Robust design provides for better circuit integrity over a wide range of application environments, and it reduces the potential for failure in test, thereby increasing yield and reliability.

Dielectric breakdown also occurs when too high a voltage is applied across the tunneling dielectric too quickly. This causes the majority of the charge transfers to occur as a breakdown rather than true tunneling. Since Fowler-Nordheim tunneling is the least stressful method for programming, EXEL designers ramp the programming voltages as shown in Figure 5 to reduce the dielectric breakdown stress.

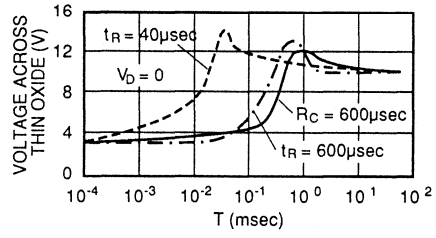

FIGURE 5. THIN OXIDE FIELD -V_{PP} PULSE SHAPE PROBLEM

ENDURANCE

E²PROM endurance is measured in the number of write and erase operations through which each bit can be cycled reliably. The amount of charge that can be stored and removed from a cell decreases as the cumulative number of program cycles rises.

Charge trapping is an intrinsic failure mechanism which tends to narrow the difference between negatively and positively charged threshold voltages (device windows) as a function of erase/write cycles. Eventually, after several million cycles, the window is collapsed completely as shown in Figure 6. This charge trapping is cumulative and increases proportionally with the magnitude and duration of the programming current.

DATA RETENTION

Data retention is the ability of the E²PROM cell to retain a charge over extended periods of time in the absence of applied gate bias. Failures are caused primarily by impurities in the structure of the storage device which cause undesired leakage paths.

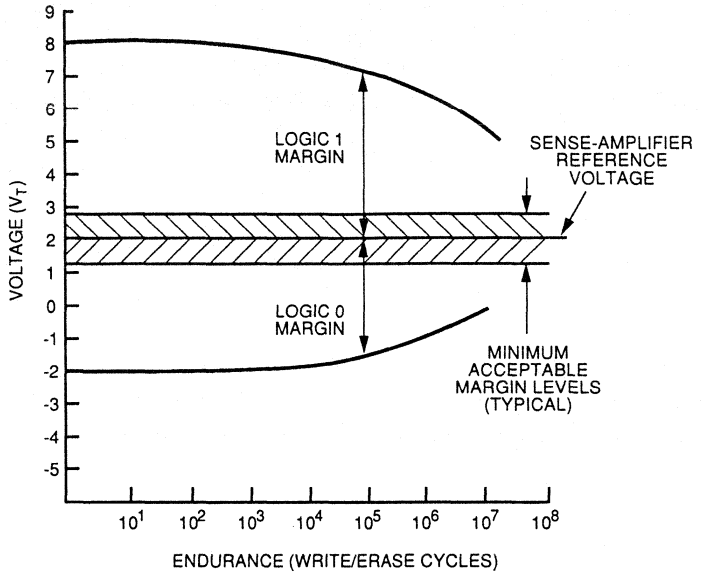

FIGURE 6. LOGIC MARGIN VS. ENDURANCE FOR FLOATING GATE E²PROM

Studies have shown that data retention cannot be increased by programming with higher voltage or for extended periods of time. Figure 7 shows that cell margin versus time approach each other asymptotically, regardless of the initial margin. Over-programming could, in fact, be detrimental to endurance characteristics.

Data retention characteristics can be predicted by measuring cell margin after baking at a high temperature. All EXEL devices are specified for a data retention of ten years minimum from the last write. In comparison, some nonvolatile alternatives such as CMOS static RAMs with integrated battery backup, specify data retention from time of manufacture, not from time of last write.

Endurance and data retention failure modes are fundamentally orthogonal in applications. A cell that is to be written 10,000 times does not require data retention of ten years between writes. Each cell in a device operates independently, therefore, any given memory location that is updated only upon rare occasions can be expected to retain information for long periods, even though adjacent cells are being worn out through extended cycling. Figure 8 plots endurance characteristics from infant mortality through random failures to eventual wear out.

Design quality begins with our state-of-the-art Computer Aided Engineering (CAE) and Computer Aided Design (CAD) systems. EXEL utilizes the advanced Cadence Design Framework environment, a fully integrated database, to store all design information in a rational and consistent manner. A single data model defines the relationship for all design data in each mode: schematic, symbol, simulation and layout. An open simulation system allows the designer to netlist the design prepare stimulus files, run a simulation and view the resulting waveforms.

The EXEL Design Center uses a Sun platform in conjunction with the Cadence software to provide efficient and reliable CAE/CAD capability. The system capabilities in-

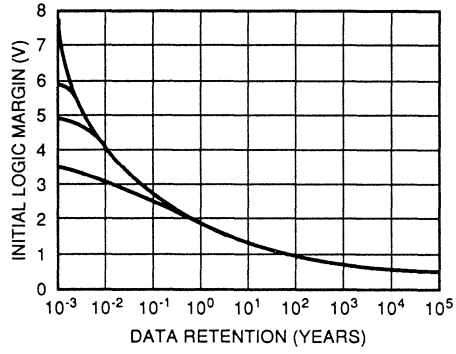

FIGURE 7. DATA RETENTION CHARACTERISTICS

	E/W < 10^5	E/W > 10^5
FAILURES	INSTANTANEOUS	GRADUAL
SCREENING	CHIP WRITE MODE	THRESHOLD BIT MAPPING

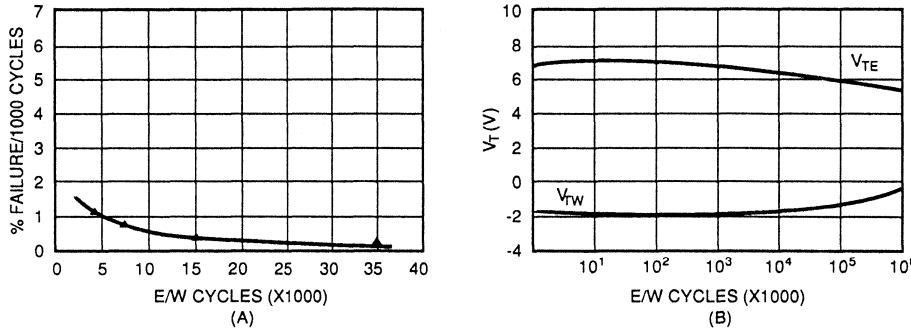

FIGURE 8. ENDURANCE TESTING

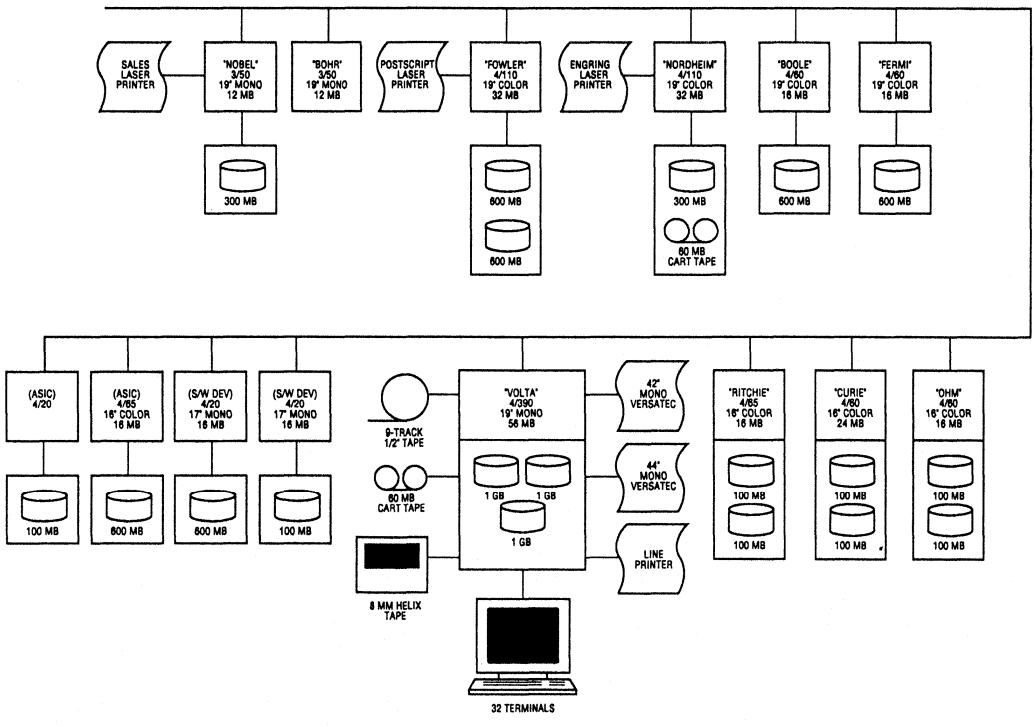

FIGURE 9. FY91 CAD/CAE NETWORK - HARDWARE

clude advanced analog design capture and simulation, statistical design, high performance layout, on-line physical design verification, and parasitic extraction, back-annotation and resimulation. The CAE/CAD network is shown in Figure 9.

An enhanced version of the University of California at Berkeley SPICE program provides interactive circuit simulation, analysis, display and modification. The statistical analysis package produces random number generation, probability density function estimation, yield calculation and sensitivity, histograms and scatterplots. The design methodology is illustrated in Figure 10.

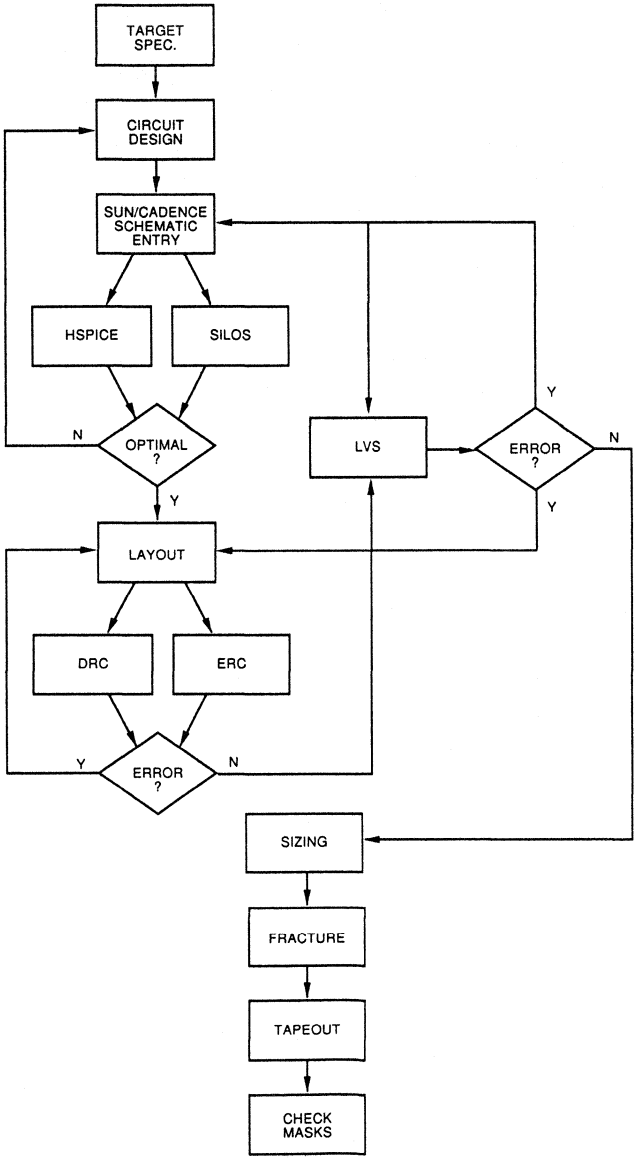

FIGURE 10. DESIGN METHODOLOGY

QUALIFICATION TESTING

Prior to formal release of the product design and ramp up for full scale unrestricted production, a sample preproduction lot is qualified in accordance with EQA-035. Qualification includes testing, inspection and acceptance of the engineering design, materials used and all processes required to produce the finished product.

Based on guidelines in MIL-M-38510, MIL-STD-883C, MIL-STD-105D, and MIL-HDBK-53-1A, a qualification level is defined and a Reliability Qualification Plan created. A control group of 100 known good devices plus a qualification test lot of devices known to be electrically good are submitted for controlled testing. The lot mix and sample size for various tests are shown in Table 3.

Testing methods and criteria for full qualification acceptance are illustrated in Table 4.

The devices under test are programmed with a control data pattern and exercised in read mode under dynamic operating conditions at 125°C. Devices are pulled at 168, 500, and 1000 hour intervals and tested electrically to ensure that units continue to function properly. An acceptable alternative test utilizes a temperature of 150°C; devices being pulled at 184 hours. This High Temperature Operating Life (HTOL) test is illustrated in Figure 11.

A temperature cycling test subjects the devices to alternating temperature extremes in a controlled chamber. The dwell time at each temperature is ten minutes, with a transition time between temperature extremes of five minutes. One complete cycle equals dwell time at each extreme plus the two one minute transition times between dwell points. This test is shown in Figure 12.

In the autoclave or Pressure Chamber Test (PCT) the devices are immersed in a pressurized bath consisting of distilled water at high temperature. After a specified test duration has been completed, the devices are electrically tested to ensure continued integrity. This PCT flow is illustrated in Figure 13.

A temperature-humidity bias (85/85 Test) subjects the devices to an ambient temperature of 85°C and a relative humidity of 85%. Devices under test are then electrically tested to ensure that performance characteristics have not degraded. The 85/85 Test is shown in Figure 14.

To determine the data retention capability of devices under test, the units are first subjected to the maximum number of erase/write cycles specified for the product. Data retention is the ability of nonvolatile memory to retain stored program data. This is determined by a High Temperature Data Retention Bake (HTDRB). Charge loss is accelerated through high temperature unbiased baking of the devices as shown in Figure 15.

When customer requirements specify additional qualifications per MIL-STD-883C, the testing and acceptance criteria are shown in Figure 16.

TABLE 3. QUALIFICATION LOT MIX AND SAMPLE SIZE REQUIREMENTS

Test	Sample size	Package
A. ESD	15/3 fab	Any package
B. LATCHUP (CMOS only)	15/3 fab	Any package
C. HTOL	228/3 fab	Both P & H
D. TEMP CYCLE OR E. THERMAL SHOCK (Solderability/lead strength/mark perm.)	120/3 assy	Both P & H
G. PRESSURE POT (Autoclave)	75/3 assy	Plastic only
H. 85/85	75/3 assy	Plastic only
I. MIL-883 group B	40/3 assy	Hermetic only
J. MIL-883 group C	75/3 assy	Hermetic only
K. MIL-883 group D	75/3 assy	Hermetic only
L. ENDURANCE CYCLING (E^2 products only)	120/3 fab	Both P & H
M. DATA RETENTION (E^2 products only)	120/3 fab	Both P & H

TABLE 4. TEST METHODS AND ACCEPTANCE CRITERIA

Test	Condition	Test Method	Sample Size	Accept/Reject
A) ESD	All pins capable of specified VDC (both polarities)		15 (3 fab runs)	15/0
B) LATCHUP	Must withstand specified MA without latching up		15 (3 fab runs)	15/0
C) HTOL	1000 hrs. @ 125°C	883-M1015	228 (3 fab lots)	3/0
D) TEMP. CYCLE	Condition C, 500 cycles -65 to 150°C	883-M1010	120 (3 ass'y lots)	2/0
E) THERMAL SHOCK	Condition B, 200 cycles -55 to 125°C	883-M1011	120 (3 ass'y lots)	2/0
F) PACKAGE TESTS				
1. Solderability	245 ± 5°C	883-M2003	15 (3 ass'y lots)	15/0
2. Mark Perm.	Four solvent solutions	883-M2015	12 (3 ass'y lots)	20/0
3. Lead Integrity	Condition B-1	883-M2004	12 (3 ass'y lots)	20/0
G) PRESSURE POT (PCT)	96 hours 15 PSI & 121°C	JEDEC-22 MA102	75 (3 ass'y lots)	3/0
H) 85/85	1000 Hours 85% RH 85°C	JEDEC-22 MA101	75 (3 ass'y lots)	3/0

TABLE 4. TEST METHODS AND ACCEPTANCE CRITERIA (Continued)

Test	Condition	Test Method	Sample Size	Accept/Reject
I) 883 GROUP B TESTS				
1. Solderability	245 ± 5°C	883-M2003	15 (3 ass'y lots)	15/0
2. Mark Perm.	Four solvent solutions	883-M2015	12 (3 ass'y lots)	20/0
3. Bond Strength	Condition C or D	883-M2011	12 (3 ass'y lots)	20/0
J) 883 GROUP C DIE RELATED TESTS (SEE HTOL)				
K) 883 GROUP D PACKAGE RELATED TESTS (ALL SUBGROUPS)				
SUBGROUP 1 1. Physical Dimensions		883-M2016	15 (3 ass'y lots)	15/0
SUBGROUP 2 1. Lead Dimensions	Condition B2	883-M2004	15 (3 ass'y lots)	15/0
2. Fine Leak	Condition A	883-M1014	15 (3 ass'y lots)	15/0
3. Gross Leak	Condition C	883-M1014	15 (3 ass'y lots)	15/0
SUBGROUP 3 1. Thermal Shock	Condition B, 15 cycles -55 to 125°C	883-M1011	120 (3 ass'y lots)	2/0
2. Temp. Cycle	Condition C, 100 cycles -65 to 150°C	883-M1010	120 (3 ass'y lots)	2/0
3. Fine Leak	Condition A	883-M1014	15 (3 ass'y lots)	15/00
4. Gross Leak	Condition C	883-M1014	15 (3 ass'y lots)	15/0
5. Visual Examination		883-M1004/M1010	15 (3 ass'y lots)	15/0
6. Electrical Endpoints Test	25°C		15 (3 ass'y lots)	15/0

TABLE 4. TEST METHODS AND ACCEPTANCE CRITERIA (Continued)

Test	Condition	Test Method	Sample Size	Accept/Reject
K) MIL 883 GROUP D TESTS (Continued)				
SUBGROUP 4				
1. Mechanical Shock	Condition B	883-M2002	15 (3 ass'y lots)	15/0
2. Vibration, Variable Frequency	Condition A	883-M2007	15 (3 ass'y lots)	15/0
3. Constant Acceleration	Condition E Y1 only	883-M2001	15 (3 ass'y lots)	15/0
4. Fine Leak	Condition A	883-M1014	15 (3 ass'y lots)	15/0
5. Gross Leak	Condition C	883-M1014	15 (3 ass'y lots)	15/0
6. Visual Examination		883-M1010/M1011	15 (3 ass'y lots)	15/0
7. Electrical Endpoints Test	25°C		15 (3 ass'y lots)	15/0
SUBGROUP 5				
1. Salt Atmosphere	Condition A	883-M1009	15 (3 ass'y lots)	15/0
2. Fine Leak	Condition A	883-M1014	15 (3 ass'y lots)	15/0
3. Gross Leak	Condition C	883-M1014	15 (3 ass'y lots)	15/0
4. Visual Examination		883-M1009	15 (3 ass'y lots)	15/0
SUBGROUP 6				
1. Internal Water Vapor Content	5000 PPM max @ 100°C	883-M1018	6 (3 ass'y lots)	50/1
SUBGROUP 7				
1. Adhesion of Lead Finish		883-M2025	15 (3 ass'y lots)	15/0
SUBGROUP 8				
1. Lid Torque		883-M2024	6	50/0
L) ERASE/WRITE CYCLING				
	10K cycles @ 25°C followed by 72 hr @ 150°C bake with all FF pattern		120 (3 fab lots)	2/0
M) HTDRB (RETENTION BAKE)				
	1 KHRS @ 150°C or 175 hrs @ 200°C pins unbiased		120 (3 fab lots)	2/0

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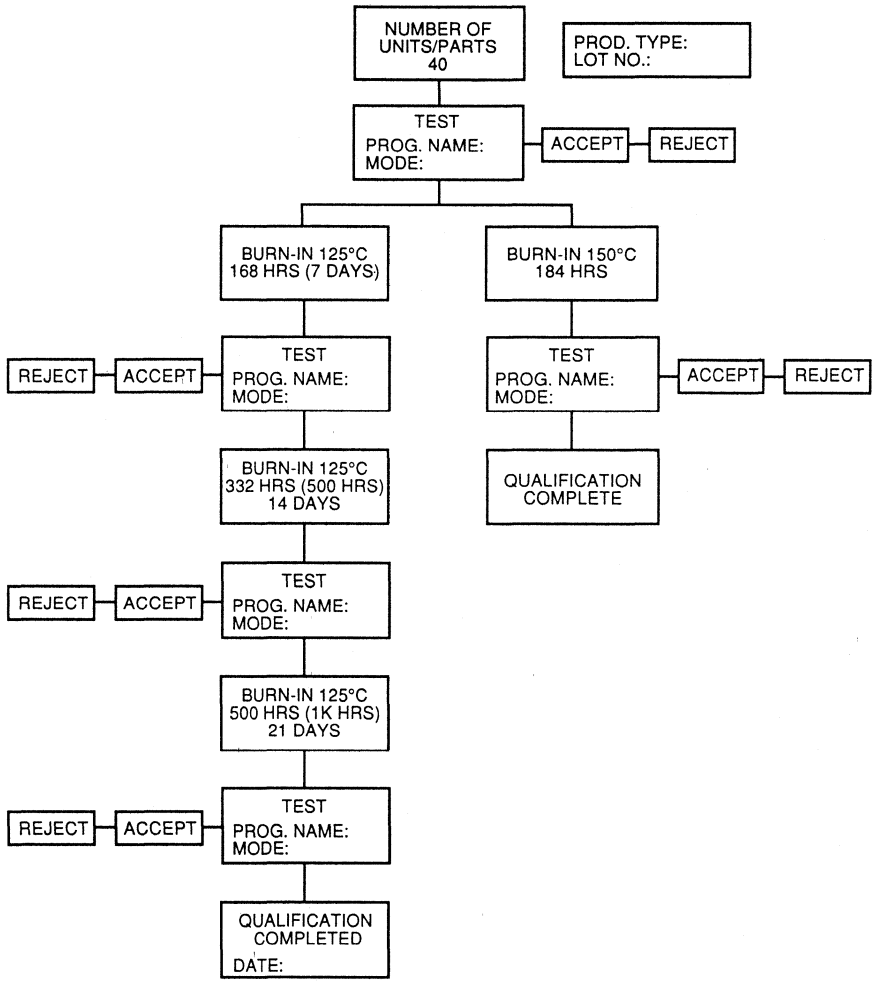

FIGURE 11. HTOL QUALIFICATION FLOWCHART

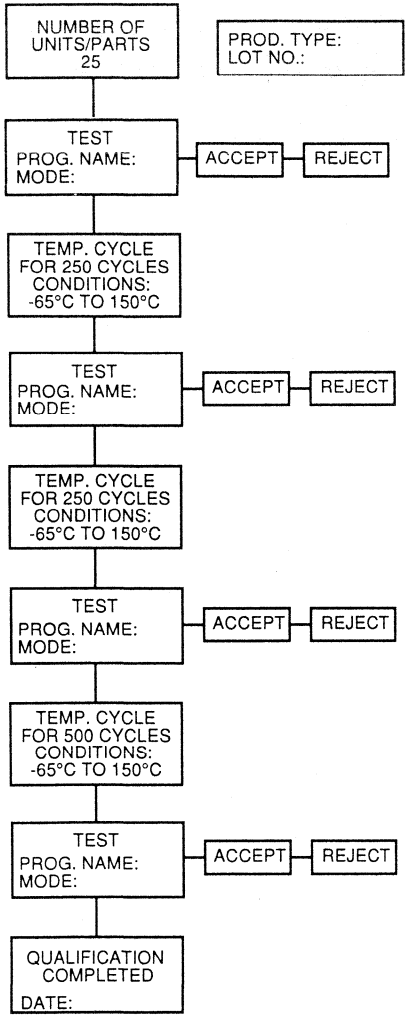

FIGURE 12. TEMPERATURE CYCLE FLOW

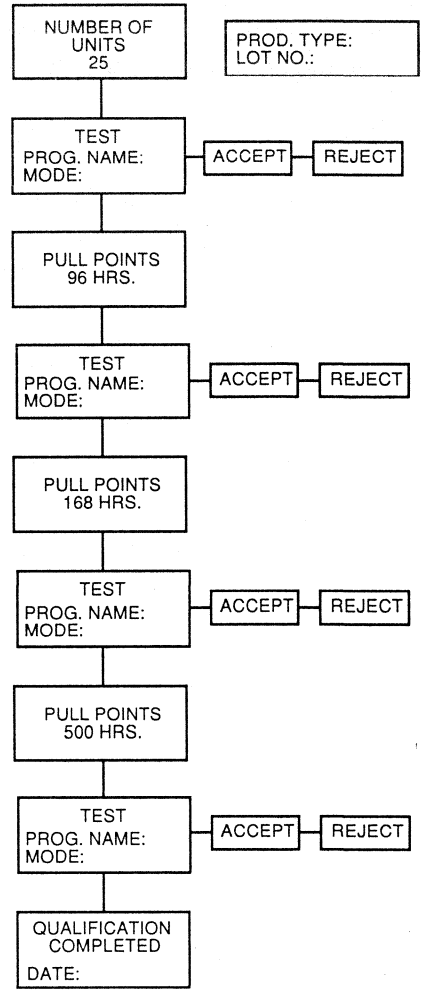

FIGURE 13. PCT FLOWCHART

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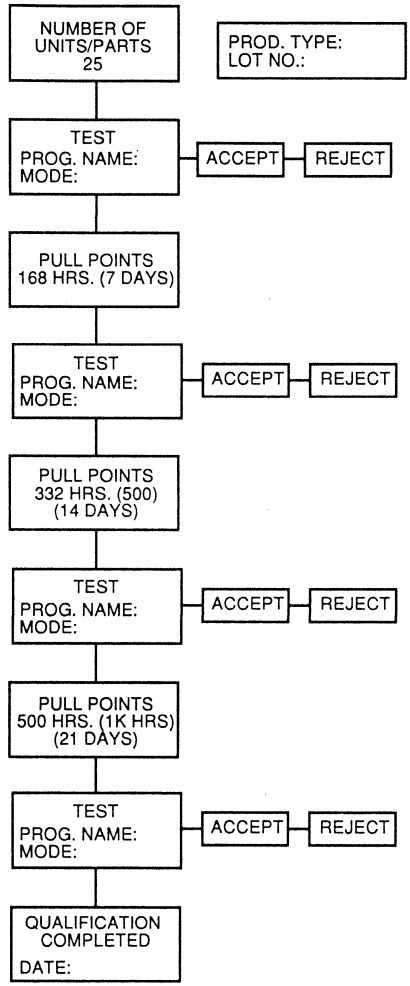


FIGURE 14. 85/85 TEST

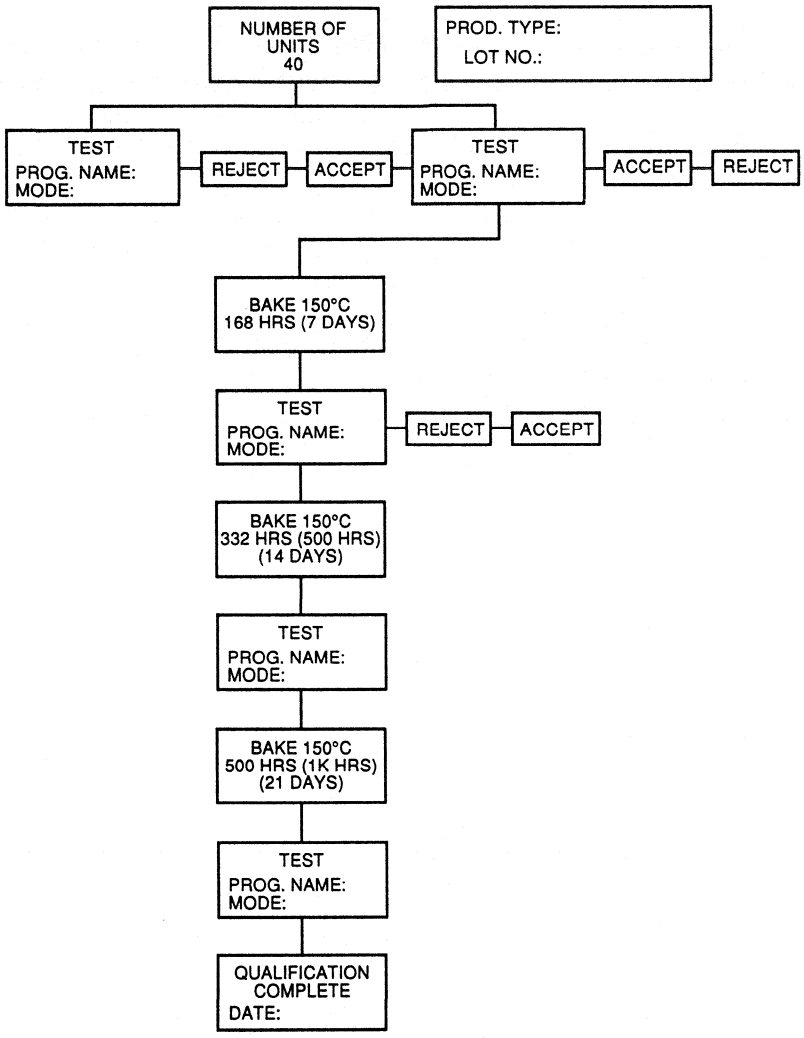


FIGURE 15. DATA RETENTION FLOW

EXEL Microelectronics Understands Rel Business

MIL-STD-105

Table I — Sample Size Code Letters

Lot or Batch Size	General Inspection Levels I	II (Normally Used)	III	Sample Size Code Letter	Sample Size
2 to 8	A	A	B	A	2
9 to 15	A	B	C	B	3
16 to 25	B	C	D	C	5
26 to 50	C	D	E	D	8
51 to 90	C	E	F	E	13
91 to 150	D	F	G	F	20
151 to 280	E	G	H	G	32
281 to 500	F	H	J	H	50
501 to 1200	G	J	K	J	80
1201 to 3200	H	K	L	K	125
3201 to 10000	J	L	M	L	200
10001 to 35000	K	M	N	M	315
35001 to 150000	L	N	P	N	500
150001 to 500000	M	P	Q	P	800
500001 and Over	N	Q	R	Q	1250
				R	2000

Table II-A — Single Sampling plans for normal inspection (Master table)

Acceptable Quality Levels (normal inspection)

Sample Size Code Letter	0.010 Ac Re	0.015 Ac Re	0.025 Ac Re	0.040 Ac Re	0.065 Ac Re	0.10 Ac Re	0.15 Ac Re	0.25 Ac Re	0.40 Ac Re	0.65 Ac Re	1.0 Ac Re	1.5 Ac Re	2.5 Ac Re	4.0 Ac Re	6.5 Ac Re	10 Ac Re	15 Ac Re	25 Ac Re
A	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 ▼ 1	0 1	↓	1 ▼ 2	1 2
B	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	2 3
C	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	↓	↓	↓	3 4
D	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	0 ▼ 1	↓	1 ▼ 2	1 ▼ 2	1 2	2 3	3 4	5 6
E	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	2 3	2 3	3 4	5 6	7 8
F	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1 2	↓	3 4	5 6	7 8	10 11
G	↓	↓	↓	↓	↓	↓	↓	↓	0 ▼ 1	1 2	1 ▼ 2	1 2	2 3	3 4	5 6	7 8	10 11	14 15
H	↓	↓	↓	↓	↓	↓	0 1	0 ▼ 1	↓	↓	2 3	2 3	3 4	5 6	7 8	10 11	14 15	21 22
J	↓	↓	↓	↓	0 1	0 1	↓	↓	1 2	2 3	3 4	3 4	5 6	7 8	10 11	14 15	21 22	↓
K	↓	↓	0 1	0 1	↓	↓	1 2	1 2	2 3	3 4	5 6	5 6	7 8	10 11	14 15	21 22	↓	↓
L	↓	0 1	↓	↓	1 2	1 2	2 3	2 3	3 4	5 6	7 8	7 8	10 11	14 15	21 22	↓	↓	↓
M	0 1	↓	1 2	1 2	2 3	2 3	3 4	3 4	5 6	7 8	10 11	10 11	14 15	21 22	↓	↓	↓	↓
N	↓	1 2	2 3	2 3	3 4	3 4	5 6	5 6	7 8	10 11	14 15	14 15	21 22	↓	↓	↓	↓	↓
P	1 2	2 3	3 4	3 4	5 6	5 6	7 8	7 8	10 11	14 15	21 22	21 22	↓	↓	↓	↓	↓	↓
Q	2 3	3 4	5 6	5 6	7 8	7 8	10 11	10 11	14 15	21 22	↓	↓	↓	↓	↓	↓	↓	↓
R	3 4	5 6	7 8	7 8	10 11	10 11	14 15	14 15	21 22	↓	↓	↓	↓	↓	↓	↓	↓	↓

AC = Acceptance number.

Re = Rejection Number.

▼ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.

▲ = Use first sampling plan above arrow.

MIL-S-19500

EXEL

TABLE C-1, LTPD sampling 1/2/
Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)											
0	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)
1	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)
2	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)
3	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)
4	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)
5	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)
6	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)
7	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)
8	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)
9	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)
10	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	551 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)

1/ Sample sizes are based upon the Poisson exponential binominal limit.

2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

FIGURE 16

IN-PROCESS QUALITY

As a part of EXEL's Total Quality Awareness, a comprehensive Statistical Process Control (SPC) program has been implemented. SPC is used for all critical processes affecting the performance, yield and quality of EXEL products.

The uniformity and repeatability of selected process parameters is an indicator of the quality and reliability of the product produced on that process. As part of the ongoing SPC implementation, multi-functional teams are identifying key process indicators (KPI) that are critical for controlling those processes. These KPI are then plotted on SPC control charts (see figure 17A) on line by the production operators to monitor and evaluate the variation in the process. In addition to the theory and fundamentals of SPC the implementation teams have training in problem solving skills. When a control chart indicates a process is out of control, a responsive action procedure (RAP) is initiated (see figure 17B). This is a proactive approach to monitor a process while it is running and empowers the operator to take immediate action. Off-line analysis is performed by engineering using historical data to study the common causes of variation and develop permanent solutions to improve process performance.

Equipment functions are periodically monitored and maintained in accordance with procedure EQR002. Quality Assurance reviews all equipment calibrations and establishes calibration intervals based on the stability, purpose, and degree of equipment usage. An independent metrology organization performs all calibrations to accepted and approved national standards. Maintenance, preventive maintenance, and calibration records are then filed for future traceability.

A comprehensive equipment operator training and certification program is documented in EQM-23.00. Also included in this program is specialized training for technicians and inspectors. All personnel performing wafer fabrication operations, electrical die sort, assembly, test, inspection, and shipping are trained and certified per procedure EQG0001.

Training concentrates on the operating methods as defined in released procedural specifications. Training includes both formal classroom instruction and on the job training. During training and upon graduation, each employee is evaluated and counseled (see Figure 18). Upon successful completion of the prescribed course an Operation Certification (Figure 19) is awarded.

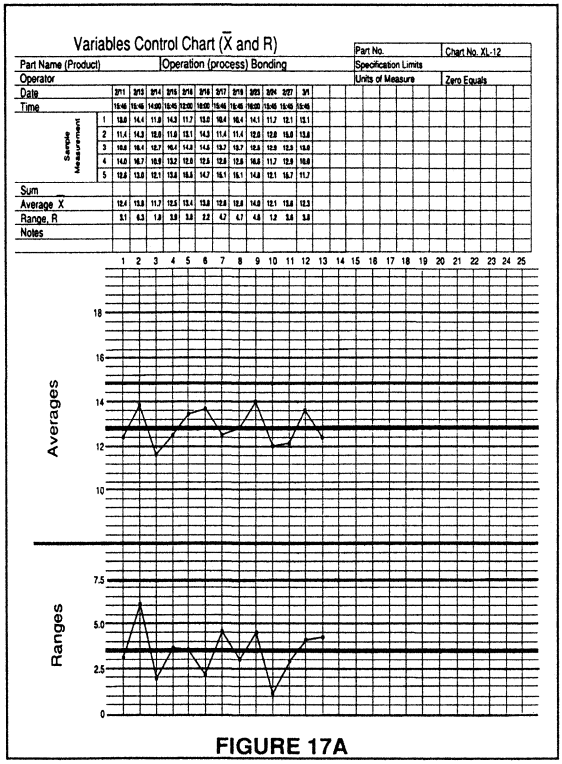


FIGURE 17A

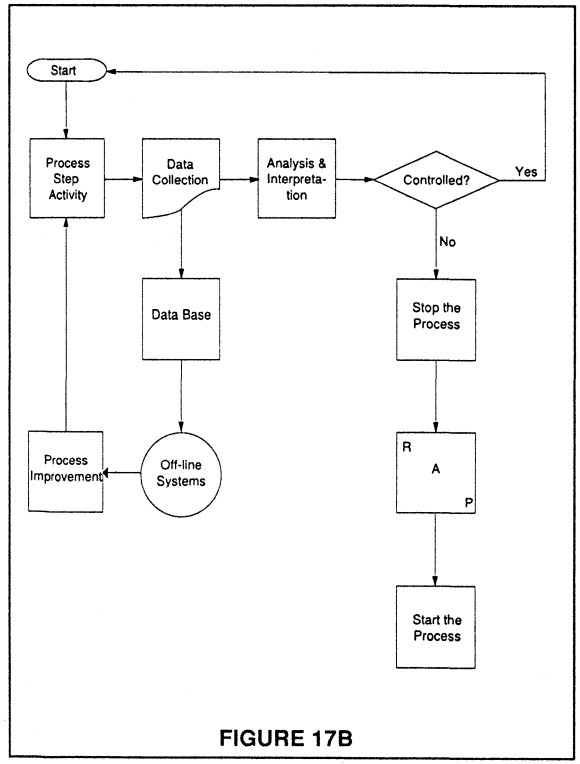


FIGURE 17B

REL & C Q.A.

EMPLOYEE TRAINING EVALUATION

EMPLOYEE BADGE #_____

EMPLOYEE:_____HIRE DATE:_____DEPT. NO.:_____SHIFT:_____

JOB TITLE:_____

TRAINING AREA

1 = FAIR
2 = GOOD
3 = ABOVE AVERAGE
4 = EXCELLENT

OVERALL PERFORMANCE
(CHECK ONE)
1 2 3 4

CRITERIA:	1	2	3	4	COMMENTS
JOB KNOWLEDGE					
ATTITUDE					
ABILITY TO COMPREHEND					
SHOWS INITIATIVE					
ATTENDANCE Q.C. ONLY					
EXAM RESULTS					

DATE OF EVALUATION _____

MAJOR STRENGTHS_____

AREA FOR IMPROVEMENT_____

EMPLOYEE COMMENTS _____

EMPLOYEE SIGNATURE _____

TRAINER/DATE MANAGER/DATE APPROVAL/DATE

FIGURE 18. TRAINING EVALUATION

EXEL
Microelectronics, Inc.

OPERATION CERTIFICATE

This is to certify that

_____

has successfully completed

_____

_____
Date

Technical Staff

_____
_____
_____

Corporate Staff

_____
_____
_____

FIGURE 19 GRADUATION CERTIFICATE

OUTGOING QUALITY

The quality of devices shipped is continually monitored in order to predict the rate of defectives that a customer is likely to observe in electrical testing or application. Predictions are based on the following definitions:

p — Process average Parts Per Million (PPM) defective. The PPM defective observed in the electrical test sample; the number defective divided by the number sampled.

pa(p) — Probability of acceptance for a given lot sample based on the lot sample plan. EXEL sampling includes selecting a sample of 125 parts from a lot and performing an electrical test. If one or more parts fail, the lot from which the samples were obtained is rejected and a complete screening is initiated to sort out all defectives.

AQL — Acceptable Quality Level. That value of p for which we have Pa(p) = 0.95; the PPM defective for which we have a 95 percent chance of passing the electrical sample test for a given lot.

LTPD — Lot Tolerance Percent Defective. The value of p for which we have Pa(p)=0.10; the PPM defective for which we have a 10 percent chance of passing the electrical sample test for a given lot.

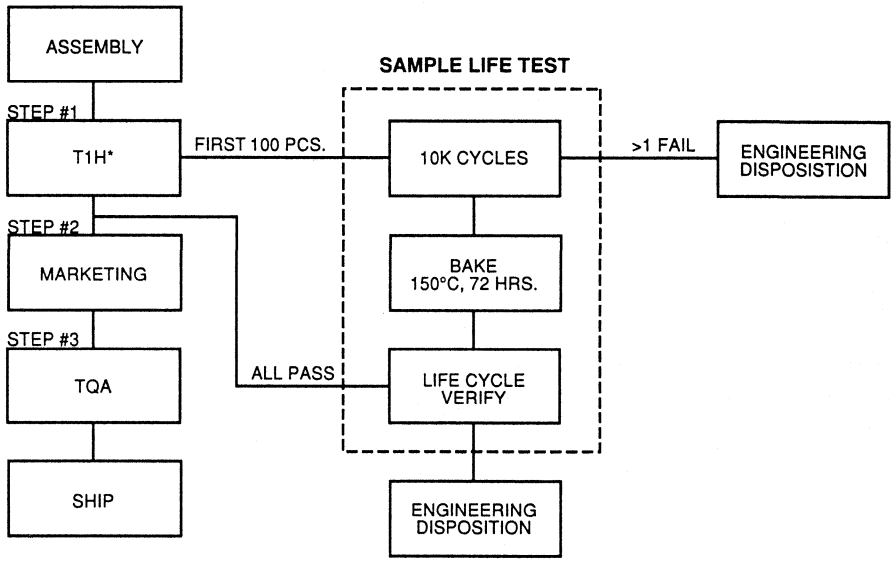
AOQ — Average Outgoing Quality. The average PPM defective being shipped when using rectifying sample inspection.

AOQL — Average Outgoing Quality Limit. The absolute maximum level of PPM defective that can be shipped based on the rectifying sample inspection plan.

RECTIFYING SAMPLE INSPECTION PLAN — A sample plan for which a lot failing to pass the sample acceptance criteria is screened to sort out all defectives.

Outgoing lots are sampled, inspected and tested by Quality Assurance using released and controlled test programs to estimate outgoing electrical quality. The program tests all critical parameters and functions as required by the product data sheet or specification. Parts are 100 percent functionally and parametrically tested prior to the sample electrical test. In this way the sample test ensures that devices have not failed in the process of testing. The electrical sample is run at room temperature; visual inspection performed in accordance with the requirements of EXEL inspection instructions. A post assembly final test is illustrated in Figure 20.

EXEL guarantees an AQL of less than 0.1 percent - 1000 PPM - for electrical parameters. With the current electrical sample plan of 125 devices tested per lot, the sample AQL is actually 0.04 percent - 400 PPM defective - for large production runs.



*T1H = FIRST HIGH TEMPERATURE ELECTRICAL TEST

FIGURE 20. POST ASSEMBLY FINAL TEST

DOCUMENTATION

Documentation intended to define product requirements and support production is formally released and subject to coordinated change control by the Document Control department. Documentation maintained by Document Control is shown in Table 5.

TABLE 5. CONTROLLED DOCUMENTS

Standard and General Operating Procedures
Assembly Flows, Specifications, and Procedures
Assembly/Bonding Diagrams
Burn-in Configuration/Schematics
Equipment Drawings and Schematics
Offshore Assembly Flows, Specifications and Procedures
Equipment Operating and Setup Specifications and Procedures
Package Drawings and Material Specifications
Material Procurement Specifications and Procedures
Production Control Specifications and Procedures
Military and Government Specifications and Standards
Product Design Specifications and Procedures
Product Flows and Schematics
Test Programs and Flows
Test Specifications and Procedures
Quality Specifications and Procedures
Wafer Fab Flows, Specifications, and Procedures
Mask Overlays/Digitizing Tapes
Released Product Binders
20X Metal Layer Film
Process Specifications
Manufacturing Instructions

When revisions are initiated by Engineering or required by Manufacturing, an Engineering Change Notice (ECN) is prepared and processed per procedure ED0001. This procedure is also used for the initial release of new documentation (see Figure 21).

Upon completion of the ECN form, Document Control assigns and logs an unique ECN number to ensure traceability throughout all production and quality assurance operations. The ECN identifies work centers directly affected by the change, provides justification for the revision, and includes a disposition on all material in process.

The ECN is reviewed by all cognizant department representatives who indicate their approval (or disapproval) on the form. The ECN is released and reproduced for a standard distribution list.

Documentation Control is also chartered with the responsibility of reviewing customer specifications and generating any internal documents necessary to meet customer requirements.

Process runcards are also generated, released, and controlled by this department. The production runcard serves as a listing of all work center operations and inspection instructions and directs the flow of materials through the various fabrication departments. Upon completion of each operation, test and inspection, the runcard is annotated to serve as an historical record for each production lot. Using this procedure, device traceability is possible through each step in the manufacturing process.

AUDITS

Quality audits are periodically performed to ensure that all personnel, systems, procedures, processes and equipment are operating in accordance with company goals. At a minimum, audits are scheduled semi-annually per Section 19.01 of the EXEL Quality Manual (EQM).

All manufacturing and production support departments are subject to this quality audit. In the event discrepancies are found, a Corrective Action Request (CAR) is initiated and processed per Section 04.01 of the EQM.

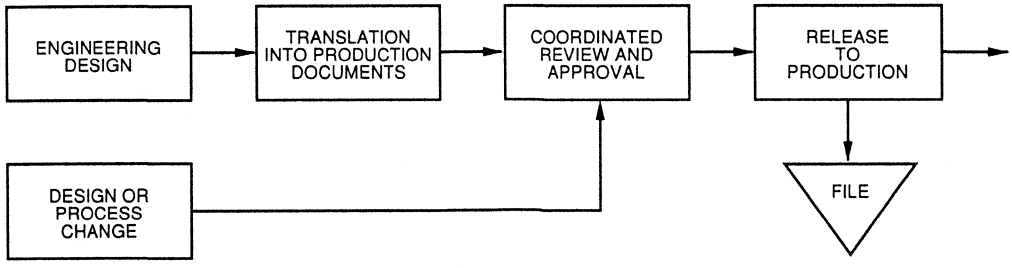


FIGURE 21. ENGINEERING CHANGE NOTICE PROCEDURE

System type audits are held every 90 days to ensure the adequacy of those operations that directly affect product quality. Per procedure EQA-016, the purpose of the audit is to sample the quality of an operation, quality controls, and the environment in which the operation takes place. Inspection points include the following:

- Accuracy of documentation used within the operation.
- Evidence of operator training and certification.
- Proper identification and segregation of all materials.
- Maintenance of operational records to ensure traceability.
- In-process and final inspection and test activities.
- Monitoring of temperature, humidity, particle count, and DI water.

Fabrication operations are audited in accordance with procedure EQA-038. This auditing and monitoring program includes the following additional inspection points:

- Verification of document and ECN control for each process step.
- Status of processing equipment calibration.
- Evidence of operator compliance to specifications and work instructions.
- Review of logs, charts and run cards for accuracy and completeness.

An example of a recent production audit is illustrated in Figure 22. At this fabrication work center, individual operating instructions and processing specification requirements were compared with actual workcenter practices to determine the percentage of compliance. The specific audit points are identified on the left side of the form; the quality index illustrated in chart format. Refer to Figure 22.

CUSTOMER INTERFACE

In pursuit of our goal of Total Customer Satisfaction, EXEL has developed a number of quality programs. The most visible of these programs is our distribution of Application Notes.

In a competitive marketplace, the supplier who provides that extra level of service invariably wins long term customer support. EXEL application notes are developed to provide customers - and future customers - with unique and cost-effective solutions to everyday design problems. Utilizing the App. Note format, EXEL engineers and designers offer suggestions for new products and services, innovative methods and procedures, inventive circuit designs and layout applications. Many times an App. Note has been credited with creating a new and different use for a standard off the shelf device.

SHIFT	YEAR 7/16-7/21 1990	WEEK 29 NO. AUDIT	NO. PASS	NO. %
DAYS	SPIN OPER.	90	86	96%
	BATCH DEVELOP	90	90	100%
SWING				
GRAVE	SPIN OPER.	90	86	96%
	BATCH DEVELOP	90	90	100%
MONITOR	RUNCARD	5	4	80%
	MAINT.PM/ CALIB.	20	16	80%
	TEMP. & REL. HUM.	13	13	100%
	SMOCK RM. SUIT-UP	40	30	75%
	TOTAL	418	385	93%

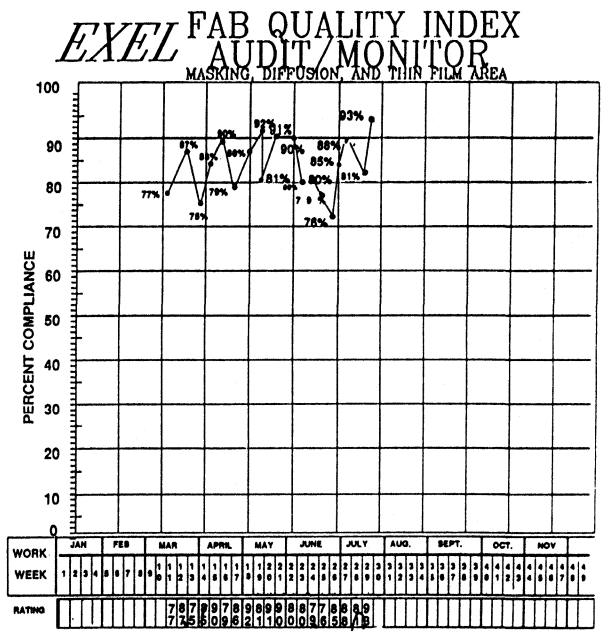


FIGURE 22.

Total satisfaction means anticipating a customer's needs well in advance of final shipment. This includes dedicated attention to quality in the earliest design stages, during material selection and review, and throughout each phase of fabrication and assembly. Total satisfaction includes follow-up after delivery and support throughout all field applications.

Customer support operations are outlined in EQM sections 04.00, 14.00, and 29.00. These sections include detailed procedures for processing customer returned materials, failure analysis and corrective action.

In the event of an application failure, a customer may request an analysis to determine if the defect was a random occurrence or an indication of potential reliability concerns. When a failure is detected, EXEL field personnel gather all necessary data concerning the problem and relay the information directly to the factory for analysis. Figure 23 shows the overall procedure for returned material and failure analysis.

Each returned device, or lot of devices, is assigned an unique RMA number for tracking and traceability. Failure analysis is performed per procedure EQA012 and may include any of the following operations:

- Duplicating the final quality test program
- Performing bench tests
- Performing reliability stress testing
- Internal visual inspection
- SEM inspection
- X-Ray inspection

Necessary corrective action - both in-plant and at the customer site - is outlined in procedure EQA006. An expanded detail of the RMA flow is shown in Figure 24.

SUPPLIER QUALITY ASSURANCE

Vendor control is detailed in the following Product Assurance documents:

- EQM 12.01, Vendor Control/Receiving Inspection
- EQA006, Corrective Action Systems
- EQA007, Material Review Board Procedure
- EQA009, Receiving Inspection for Assembled MIL-STD-883 Military/Hi-Rel Devices
- EQA010, Incoming Inspection for Assembled Plastic Devices
- EQA020, Approved Vendors List
- EQA022, QA Incoming Piece Part Lot Inspection
- EQA024, QA Review of Outgoing Purchase Orders for Raw Materials
- EQA025, Vendor Quality Rating Procedure
- Applicable SEMI standard specifications

In accordance with these documents, incoming material is categorized into three classes:

- Direct Material-A: material which is directly used to fabricate product. Included in this category are photomasks, wafers, package piece parts, and assembled materials.
- Direct Material-B: materials indirectly used to fabricate product, such as quartzware, chemicals, solvents, gases.
- Indirect Material: materials not used in production.

Direct material used by subcontractors and supplied to EXEL in semifinished form is subject to vendor control criteria including qualification, vendor quality surveys, subcontractor inspection and special requirements called out by contract.

Material Procurement Specifications (MPS) are developed to provide specific requirements for various direct materials. For commodity materials, the Semiconductor Equipment and Materials Institute (SEMI) standards are used.

All suppliers of direct materials are qualified by Quality Assurance. Qualification requires that samples of the material be used on a minimum of three engineering or production lots and that finished products be electrically tested and subject to quality analyses and stresses per EXEL specifications. Suppliers are surveyed periodically and it is the responsibility of each supplier to prove by documented evidence that he is in control of these processes. Qualified suppliers are listed on the Approved Vendor List (AVL).

Vendors of standard wafer fabrication and assembly commodities must meet SEMI standards and prove with documented evidence that they continually meet these institute requirements.

For all direct materials, suppliers and EXEL develop documented evidence of material conformance for tracking and traceability. Evidence of acceptability includes: receiving inspection reports, lab tests, certificates of conformance, vendor SPC charts, vendor quality surveys and source inspection reports.

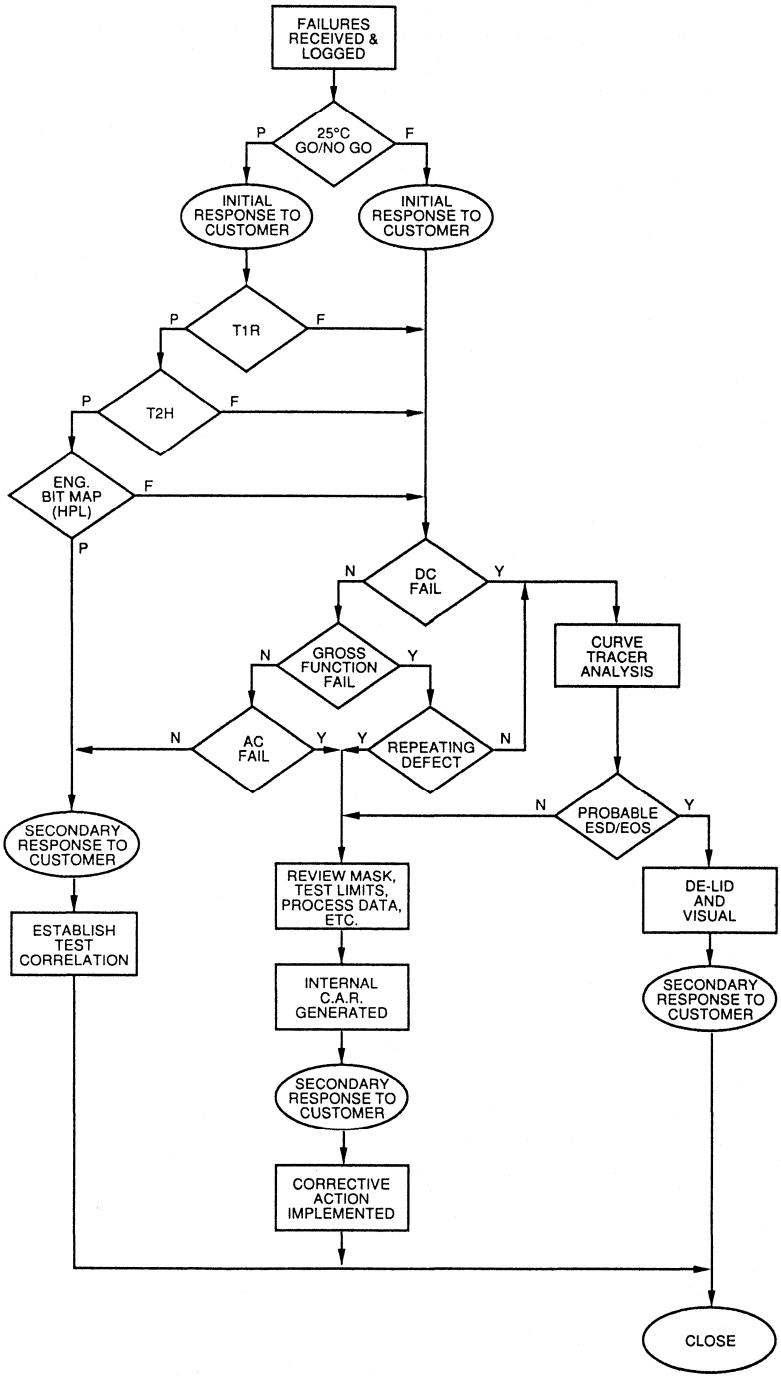


FIGURE 23. RETURNED MATERIAL FAILURE ANALYSIS

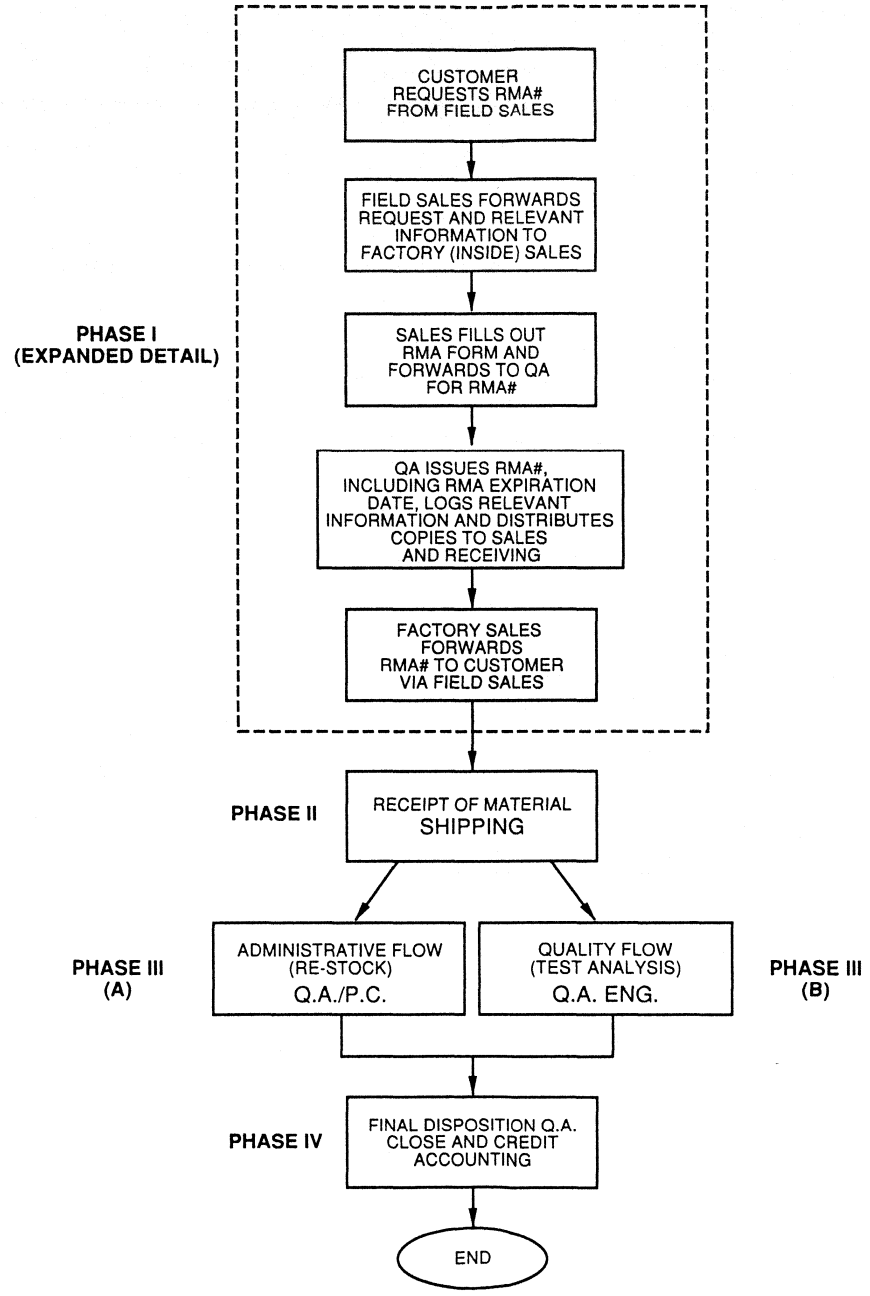


FIGURE 24. RMA FLOW

REL & C Q.A.

MILITARY APPLICATIONS

EXEL has produced devices in compliance with the requirements of MIL-STD-883C since 1987. Military products are processed in accordance with MIL-STD-883C, Class -B screening, as shown in Figure 12A.

A unique part Identification is used for ordering military product. It consists of the following alphanumeric code:

AABCCCCCD-EEEFGGGG

AA: identifies the manufacturer with a two-character Manufacturer's Prefix

XL = EXEL Microelectronics

B: identifies the Temperature Range

M = Military (T_A = -55°C to +125°C)

C...C: identifies the basic Device Type. This code, which varies in length, is common to both the standard/commercial and military versions of the product. (See examples below.)

D: identifies the Case Outline (package type)

- L = 24-lead, 300mil (width), ceramic DIP (D-9)
- Y = 28-lead, 600mil (width), ceramic DIP (D-10)
- Z = 32-lead, 450mil x 500mil, rectangular LCC (C-12)
- J = 24-lead, 600mil (width), ceramic DIP (D-3)
- 3 = 28-lead, 450mil x 450mil, square LCC (C-4)

(The hyphen, used as field separator, is part of the code.)

E...E: identifies the device Access Speed. This code, which varies in length, is given in units compatible with the product.

F: identifies the lead finish

- A = hot solder dip
- C = gold plate (used for LCC packages only)

GGGG: identifies the Screening used on the part

883C = 883C-compliant

AWARD WINNING QUALITY

At EXEL, Total Quality Management begins at the executive level with defined goals and interactive action plans. Managers at all levels champion the cause of quality throughout their organization. Defined objectives are set and employees are motivated to perform to their fullest potential. Progress is continually monitored and reported in a closed loop feedback system.

Total Productive Maintenance includes a commitment to continuing product improvement of every process. EXEL has a commitment to world-class manufacturing, engineering, and business management to ensure that products are designed and produced to the highest quality standards.

Our Total Quality Culture starts in the automated integrated CAE/CAD Design Center and continues through design verification, prototype, and preproduction evaluation. Qualification testing ensures both design and process reliability and in-process quality control monitors adherence to reliability standards. Ongoing product and process auditing provide data for quality and reliability reporting; controlled production documentation guarantees process repeatability.

Throughout each stage of design, production, and application our total quality commitment has but one goal...complete customer satisfaction.

Inspired by the numerous quality achievement awards received by ROHM Company, Ltd, our parent organization, we are striving for a total quality culture at EXEL. When all policies and procedures are in place and performing at peak efficiency, it is our intention to pursue the coveted Malcolm Baldrige Quality Achievement award.

APPENDIX D Table of Contents

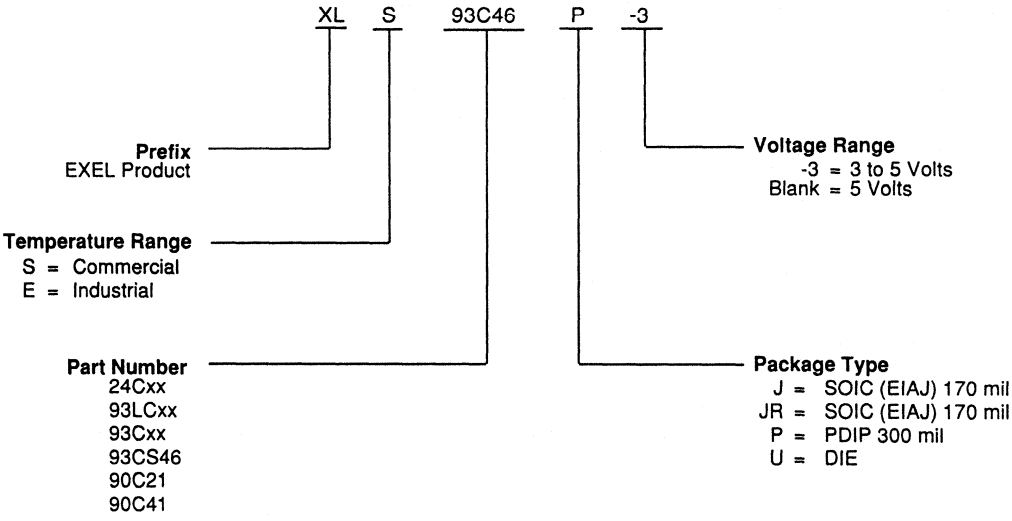
ORDER D INFO

ORDERING INFORMATION
Standard Configurations

Prefix	Temperature Range*	Part Type	Package Type*	Voltage Range
XL	S, E	XXXXXX	J, JR, P, U	3 Volts, 5 Volts

*Contact EXEL for your special temperature and packaging requirements.

Part Numbers:



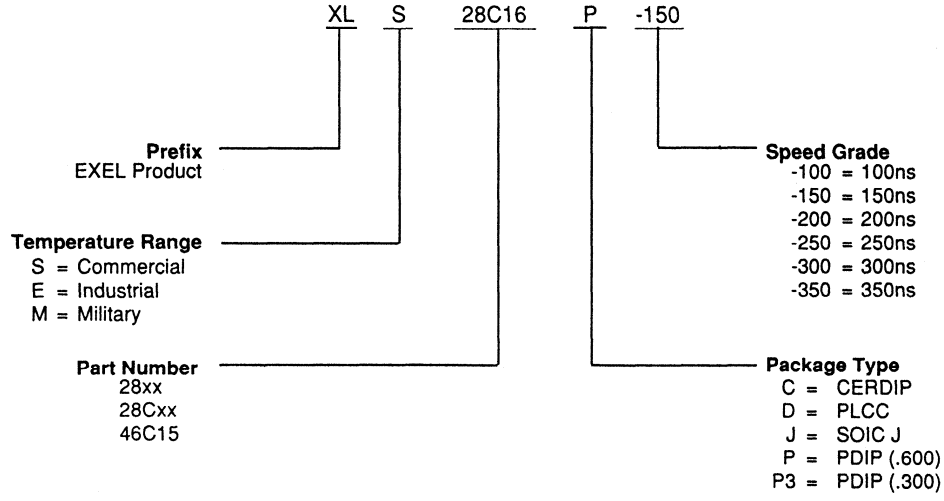
ORDER D INFO

ORDERING INFORMATION
Standard Configurations

Prefix	Temperature Range*	Part Type	Package Type*	Access Time
XL	S, E, M	XXXXXX	C, D, J, P, P3	100, 150, 200, 250, 300, 350

*Contact EXEL for your special temperature and packaging requirements.

Part Numbers:



LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

EXEL Microelectronics products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WARRANTY

Devices sold by EXEL Microelectronics are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. EXEL Microelectronics makes no warranty, express, statutory, implied, or by description, regarding the information set forth herein or regarding the freedom of the described devices from patent infringement.

EXEL Microelectronics makes no warranty of merchantability or fitness for any purpose. EXEL Microelectronics reserves the right to discontinue production and change specifications and prices at any time and without notice. EXEL Microelectronics assumes no responsibility for the use of any circuitry other than circuitry embodied in EXEL Microelectronics product. No other circuits, patents or licenses are implied.

APPENDIX F Table of Contents

EXEL North American Sales Representatives

ALABAMA
STRATEGIC MARKETING
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